DATA SHEET

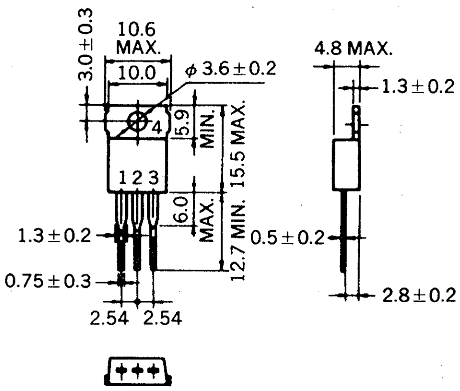
NEC

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS
2SK1495, 2SK1495-Z/2SK1496, 2SK1496-Z

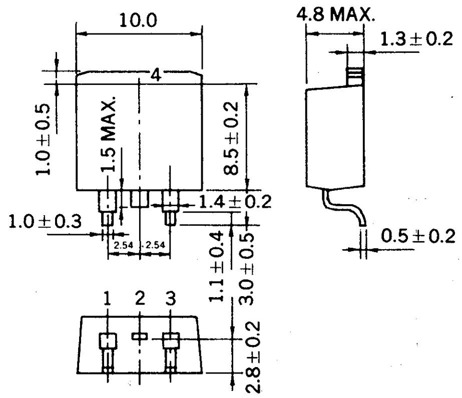
SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

PACKAGE DIMENSIONS
(Unit: mm)

2SK1495, 2SK1496

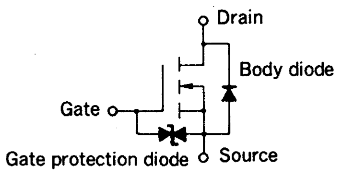


2SK1495-Z, 2SK1496-Z



PIN CONNECTIONS

1. Gate
2. Drain
3. Source
4. Fin (Drain)



DESCRIPTION

The 2SK1495/2SK1496 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.9 Ω MAX./1.0 Ω MAX. (V_{GS} = 10 V, I_D = 4 A)
- Low C_{iss} C_{iss} = 1 060 pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Storage Temperature	T_{stg}	−55 to +150	°C
Channel Temperature	T_{ch}	150	°C MAX.
Maximum Power Dissipation			
Total Power Dissipation (T_A = 25 °C)	P_T	70	W
Maximum Voltages and Currents (T_A = 25 °C)			
Drain to Source Voltage	V_{DSS}	450/500 (2SK1495/2SK1496)	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±7	A
Drain Current (pulse)	$I_{D(pulse)}$*	±28	A

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

Maximum Avalanche Capability Ratings**			
Single Avalanche Current	I_{AS}	10.5	A
Single Avalanche Energy	E_{AS}	206	mJ

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

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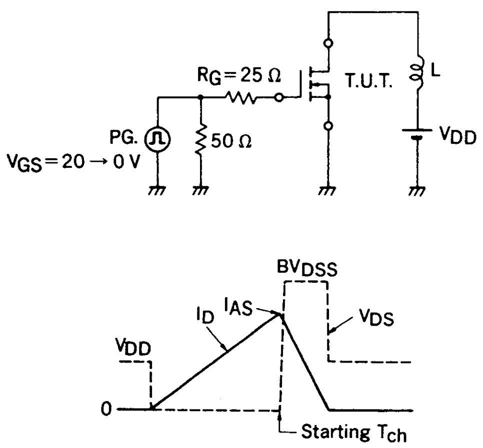
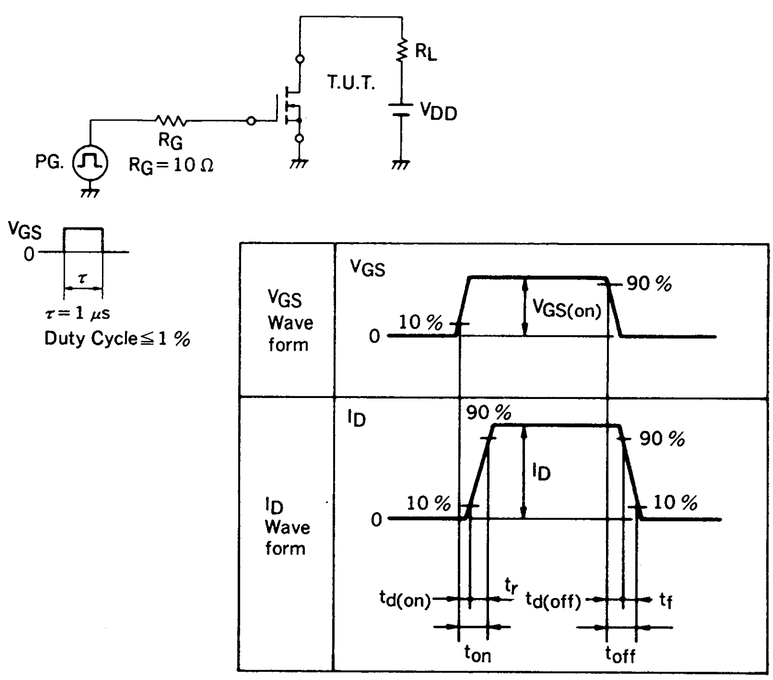
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1493/2SK1494)	$R_{DS(on)}$		0.7/0.8	0.9/1.0	Ω	V_{GS} = 10 V, I_D = 4 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	3.0			S	V_{DS} = 10 V, I_D = 4 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 450V/500V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1 060		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		340		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		150		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		20		ns	V_{GS} = 10 V
Rise Time	t_r		30		ns	V_{DD} = 150 V
Turn-Off Delay Time	$t_{d(off)}$		70		ns	I_D = 4 A, R_G = 10 Ω
Fall Time	t_f		20		ns	R_L = 37.5 Ω
Total Gate Charge	Q_G		36		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		7		nC	I_D = 7 A
Gate to Drain Charge	Q_{GD}		21		nC	V_{DD} = 400 V
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 7 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		420		ns	I_F = 7 A
Reverse Recovery Charge	Q_{rr}		2.1		μC	di/dt = 50 A/μs

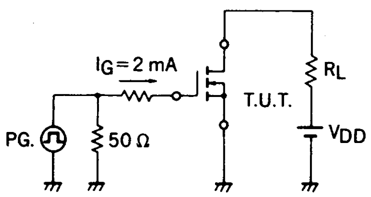
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

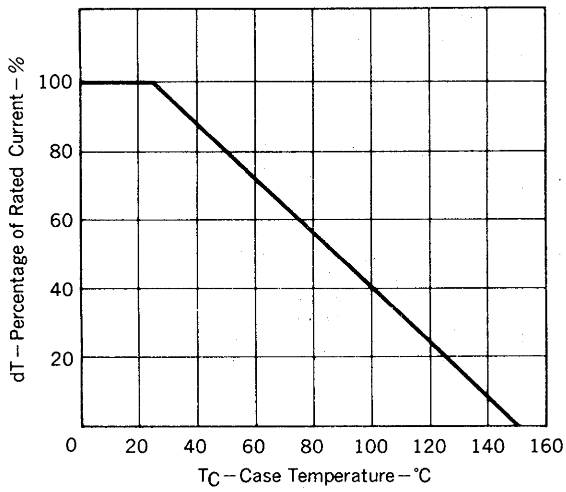


Test Circuit 3: Gate Charge

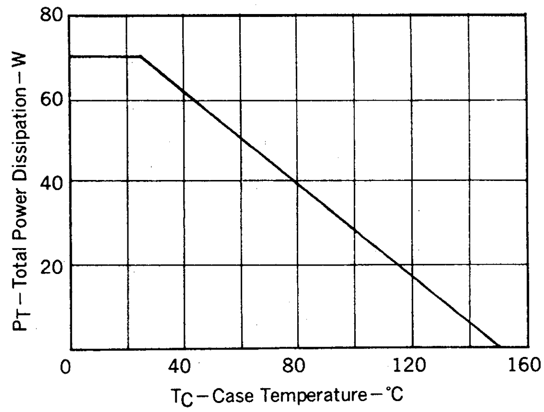


TYPICAL CHARACTERISTICS (T_A = 25 °C)

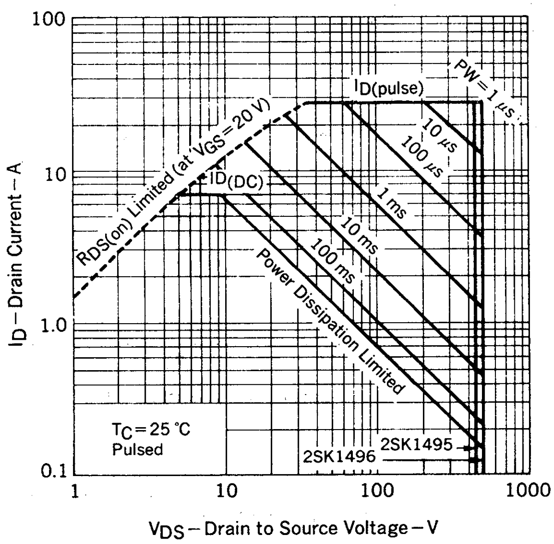
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



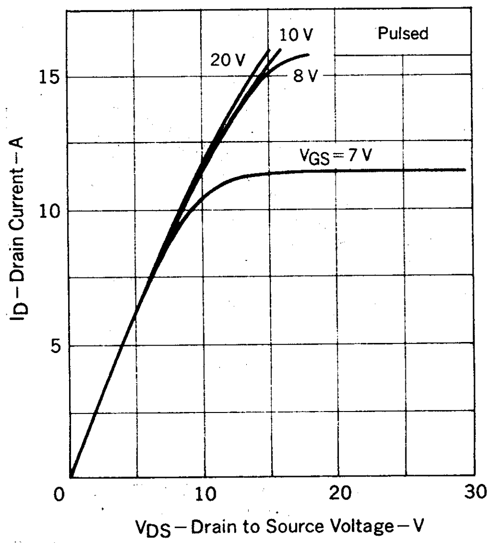
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



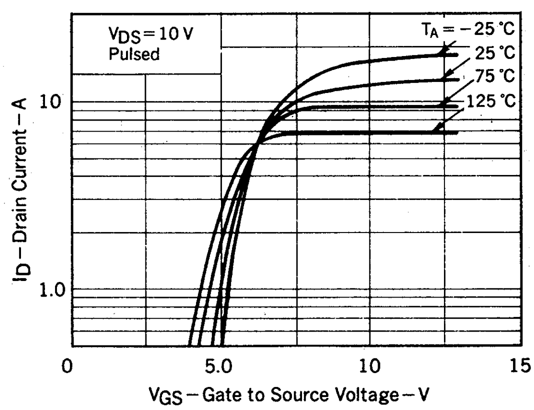
FORWARD BIAS SAFE OPERATING AREA



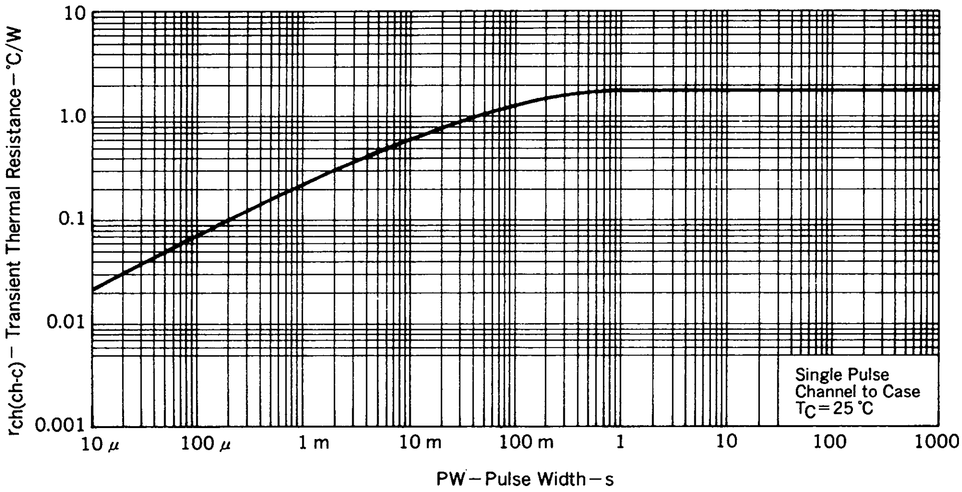
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



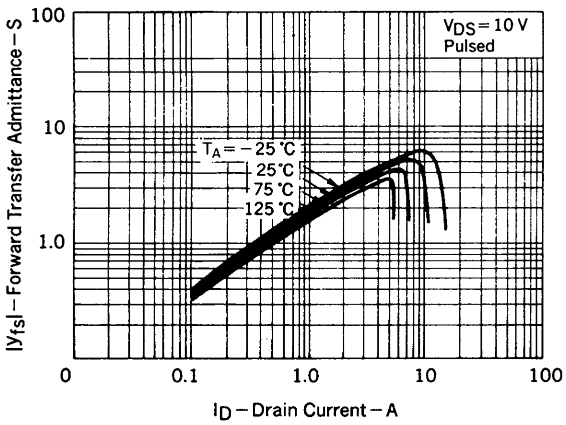
TRANSFER CHARACTERISTICS



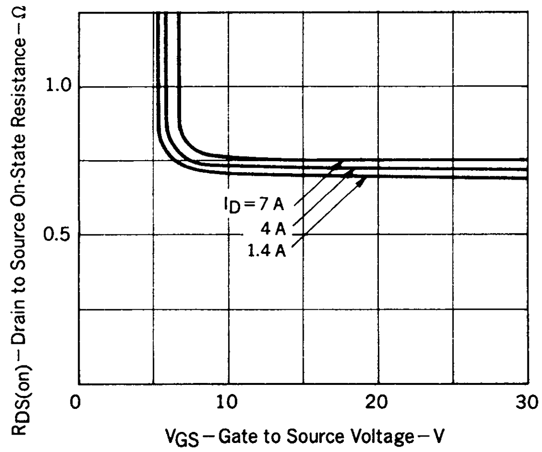
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



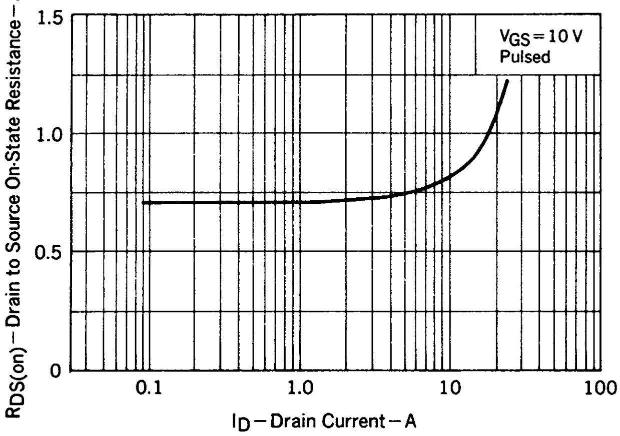
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



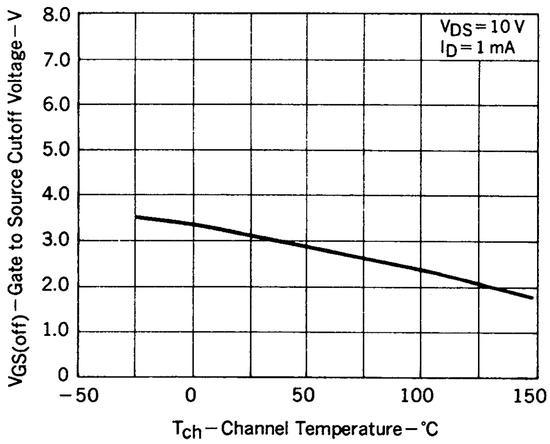
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



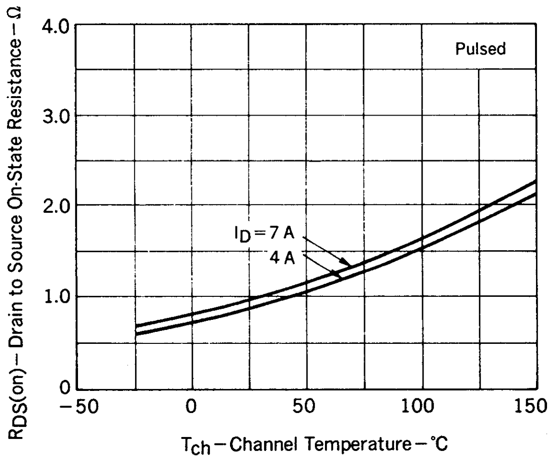
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



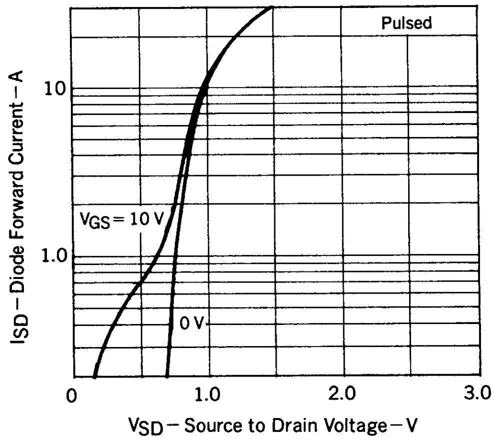
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



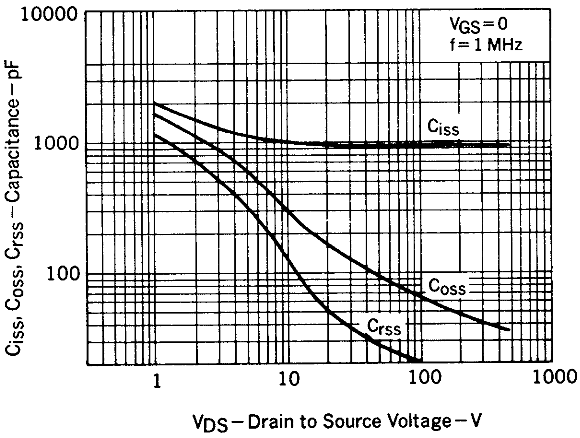
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



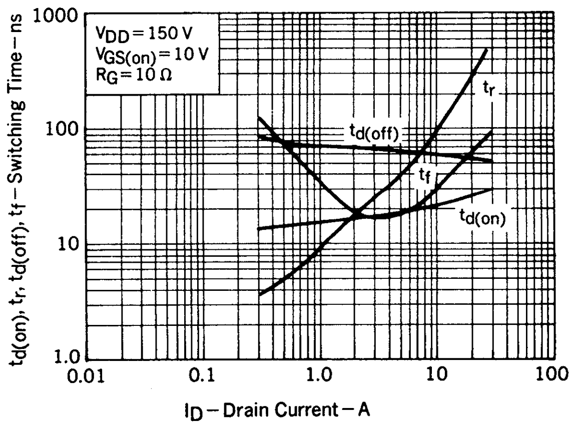
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



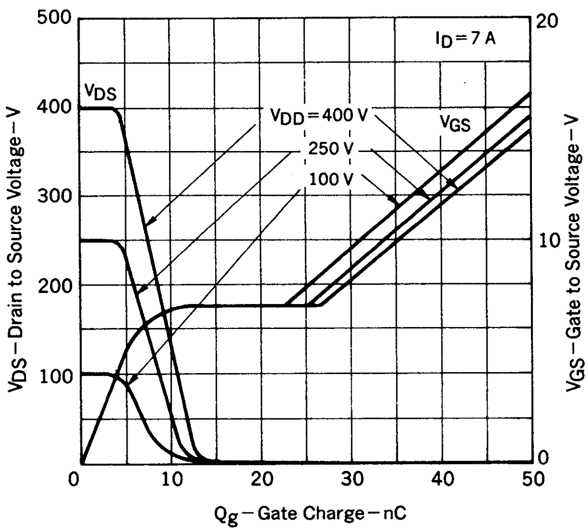
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



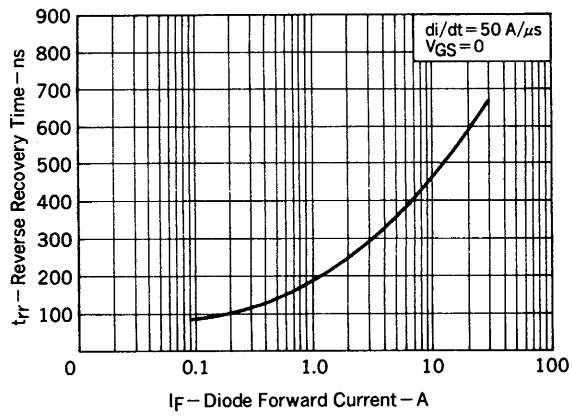
SWITCHING CHARACTERISTICS



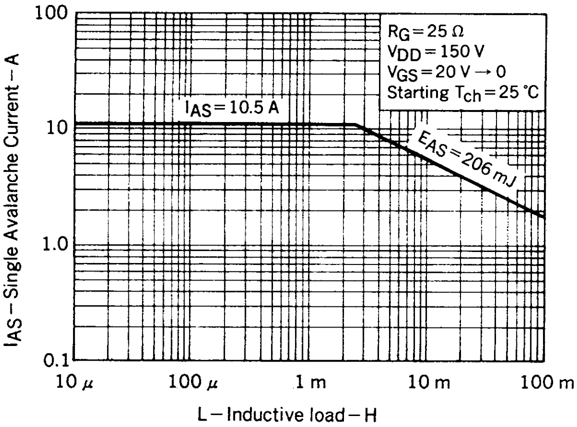
DYNAMIC INPUT CHARACTERISTICS



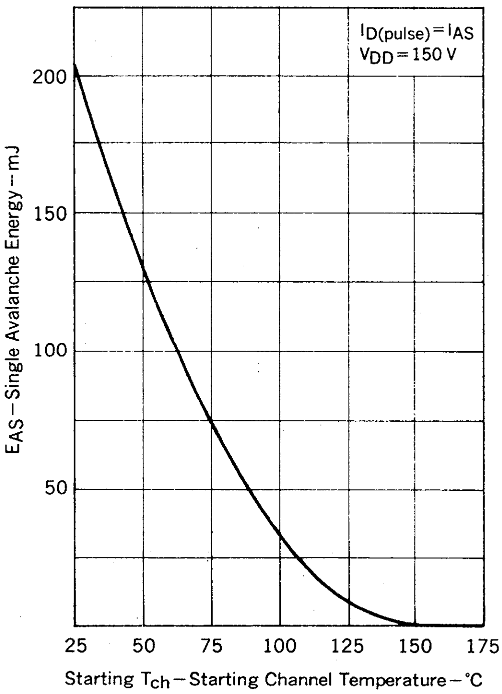
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



REFERENCE

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1037
Application circuit using Power MOS FET.	TEA-1035
Guide to quality assurance for semiconductor device.	MEI-1202
Power MOS FET features and application switching power supply	TEA-1034

[MEMO]