DATA SHEET

NEC

MOS FIELD EFFECT POWER TRANSISTORS
2SK1748, 1748-Z

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1748 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.11 Ω (V_{GS} = 10 V, I_D = 4 A)
  $R_{DS(on)}$ = 0.16 Ω (V_{GS} = 4 V, I_D = 4 A)
- Low C_{iss} C_{iss} = 850 pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semi-conductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

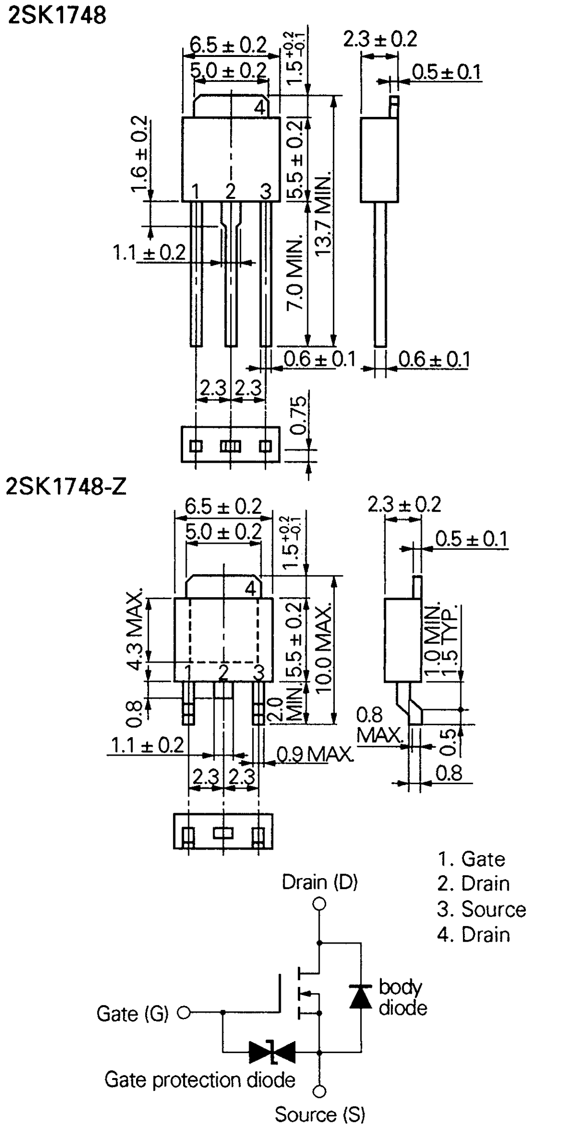
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±8.0	A
Drain Current (pulse)	$I_{D(pulse)}$*	±24	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	20	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSIONS

in millimeters

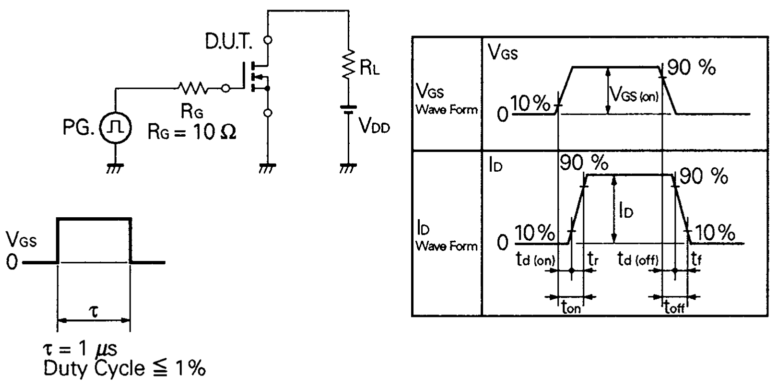


Document No. TC-2424
Date Published August 1993 M
Printed in Japan

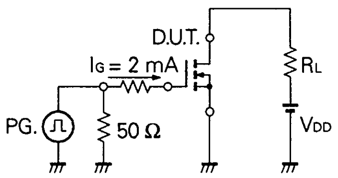
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.08	0.11	Ω	V_{GS} = 10 V, I_D = 4 A
Drain to Source On-state Resistance	$R_{DS(on)}$		0.11	0.16	Ω	V_{GS} = 4 V, I_D = 4 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	5.0			S	V_{DS} = 10 V, I_D = 4 A
Drain Leakage Current	I_{DSS}			10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	µA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		850		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		350		pF	
Reverse Transfer Capacitance	C_{rss}		100		pF	
Turn-On Delay Time	$t_{d(on)}$		15		ns	$V_{GS(on)}$ = 10 V V_{DD} = 30 V I_D = 4 A, R_G = 10 Ω R_L = 7.5 Ω
Rise Time	t_r		60		ns	
Turn-Off Delay Time	$t_{d(off)}$		100		ns	
Fall Time	t_f		45		ns	
Total Gate Charge	Q_G		3		nC	V_{GS} = 10 V I_D = 8 A V_{DD} = 48 V
Gate to Source Charge	Q_{GS}		7		nC	
Gate to Drain Charge	Q_{GD}		25		nC	
Reverse Recovery Time	t_{rr}		120		ns	I_F = 8 A, V_{GS} = 0 di/dt = 50 A/µs
Reverse Recovery Charge	Q_{rr}		200		nC	

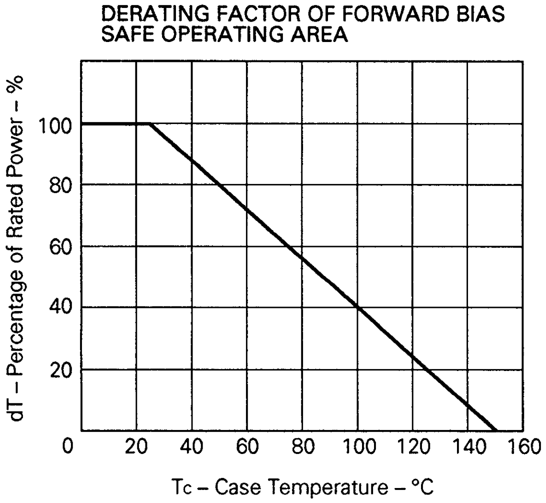
Test Circuit 1: Switching Time

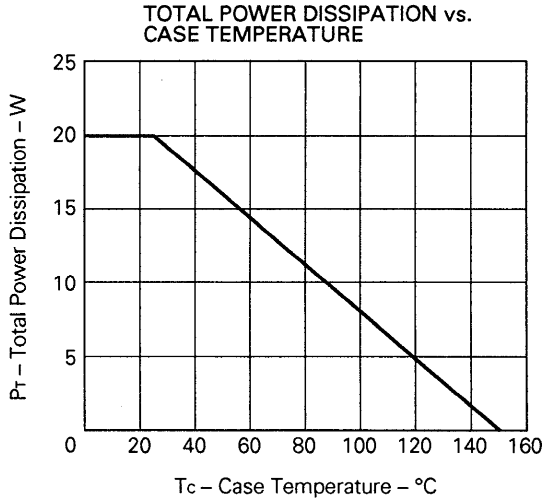


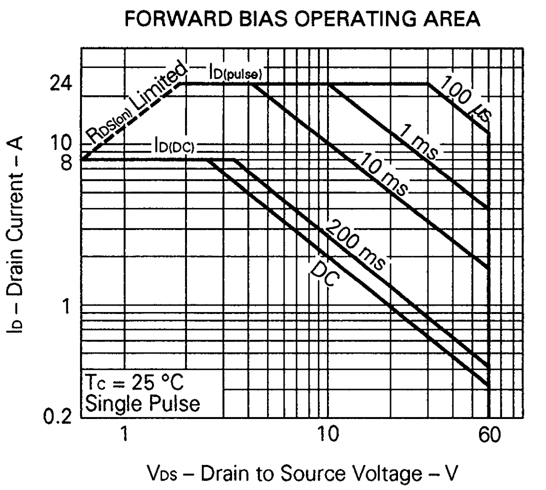
Test Circuit 2: Gate Charge

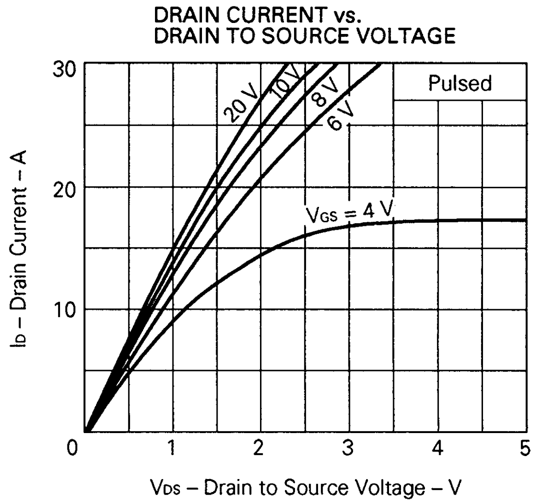


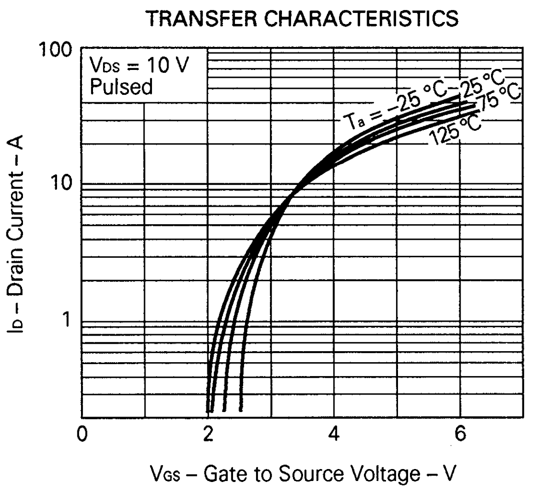
TYPICAL CHARACTERISTICS (T_a = 25 °C)



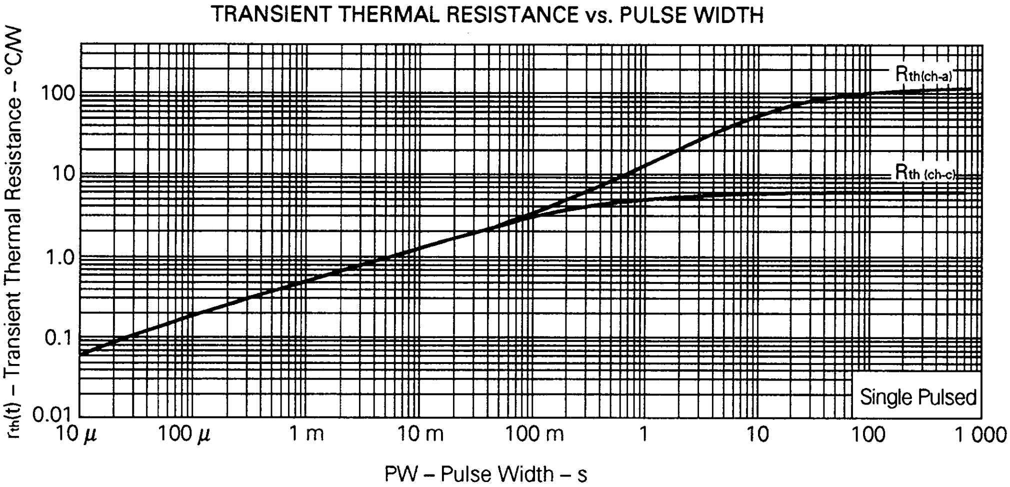




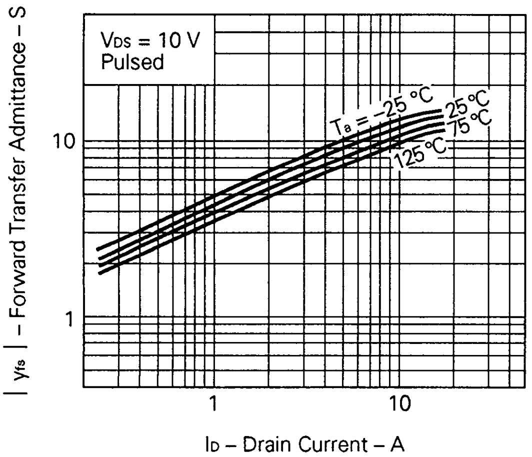




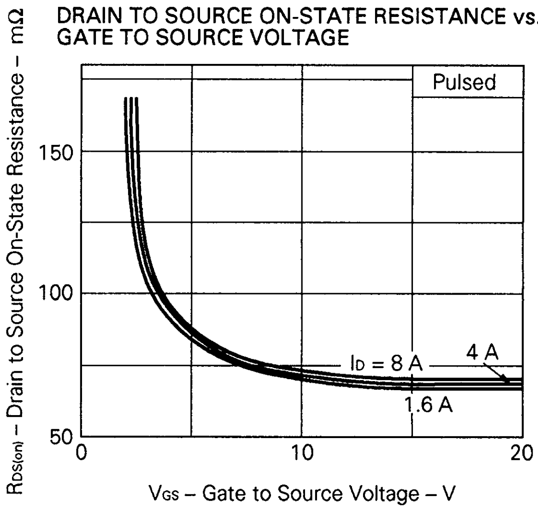
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



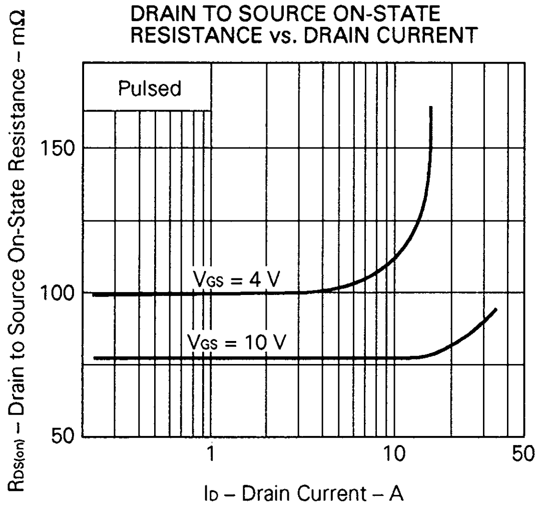
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



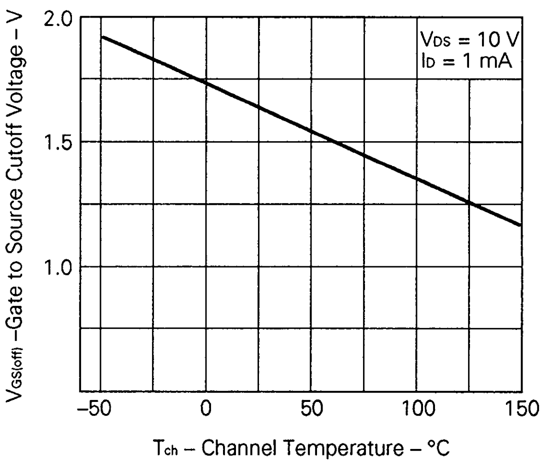
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



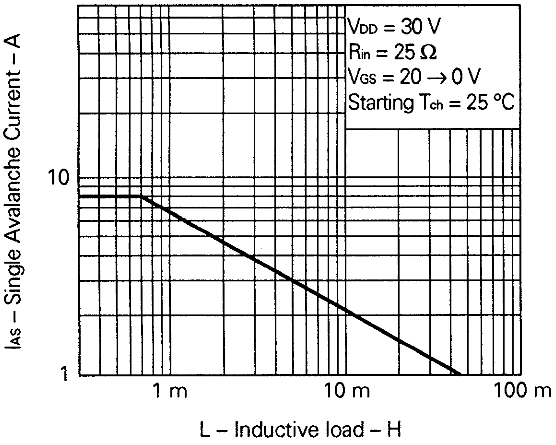
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



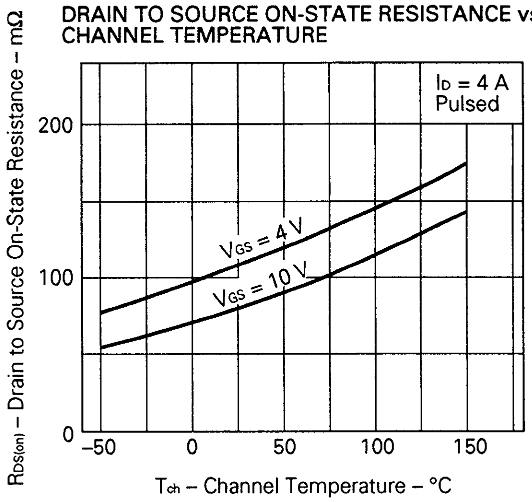
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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