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NEC

# MOS FIELD EFFECT POWER TRANSISTOR

# 2SK1995

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK1995 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

### FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 4.0 Ω ($V_{GS}$ = 10 V, $I_D$ = 2.0 A)
- Low $C_{iss}$ $C_{iss}$ = 790 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

### QUALITY GRADE

Standard

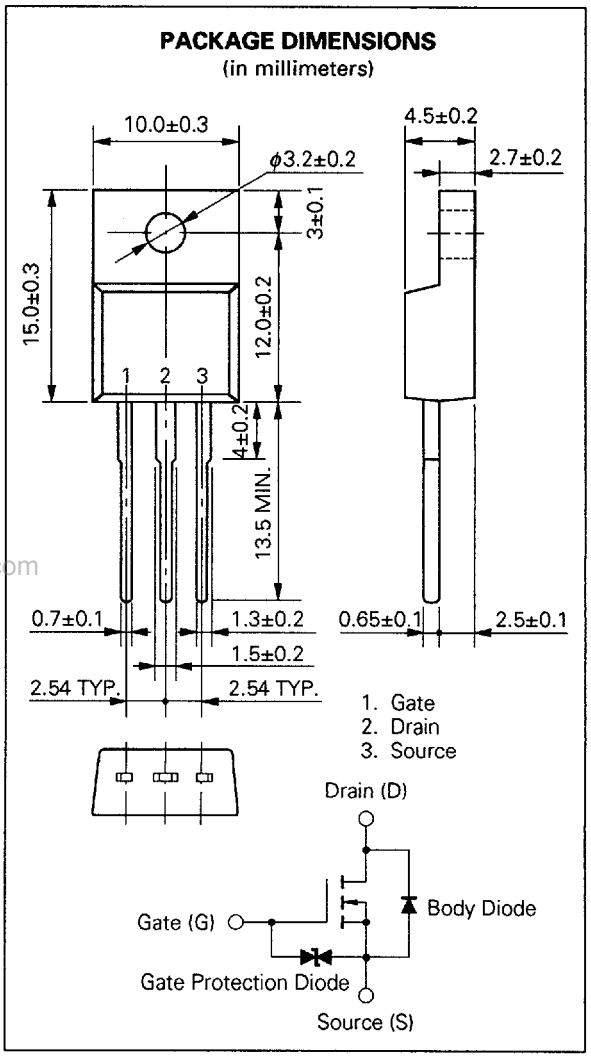
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### ABSOLUTE MAXIMUM RATINGS ($T_a$ = 25 °C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | 900 | V |
| Gate to Source Voltage | $V_{GSS}$ | ±30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±3.0 | A |
| Drain Current (pulse) | $I_{D(pulse)}$* | ±6.0 | A |
| Total Power Dissipation ($T_C$ = 25 °C) | $P_{T1}$ | 35 | W |
| Total Power Dissipation ($T_a$ = 25 °C) | $P_{T2}$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |
| Single Avalanche Current | $I_{AS}$** | 3.0 | A |
| Single Avalanche Energy | $E_{AS}$** | 16.2 | mJ |

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0

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## ELECTRICAL CHARACTERISTICS ($T_a$ = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)}$ | | 3.0 | 4.0 | Ω | $V_{GS}$ = 10 V, $I_D$ = 2 A |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | 2.5 | | 3.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Forward Transfer Admittance | $\|y_{fs}\|$ | 1.0 | | | S | $V_{DS}$ = 20 V, $I_D$ = 2 A |
| Drain Leakage Current | $I_{DSS}$ | | | 100 | μA | $V_{DS}$ = 900 V, $V_{GS}$ = 0 |
| Gate to Source Leakage Current | $I_{GSS}$ | | | ±10 | μA | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 |
| Input Capacitance | $C_{iss}$ | | 790 | | pF | $V_{DS}$ = 10 V<br>$V_{GS}$ = 0<br>f = 1 MHz |
| Output Capacitance | $C_{oss}$ | | 150 | | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 55 | | pF | |
| Turn-On Delay Time | $t_{d(on)}$ | | 17 | | ns | $V_{GS}$ = 10 V<br>$V_{DD}$ = 150 V<br>$I_D$ = 2.0 A, $R_G$ = 10 Ω<br>$R_L$ = 75 Ω |
| Rise Time | $t_r$ | | 12 | | ns | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 104 | | ns | |
| Fall Time | $t_f$ | | 24 | | ns | |
| Total Gate Charge | $Q_G$ | | 28 | | nC | $V_{GS}$ = 10 V<br>$I_D$ = 3 A<br>$V_{DD}$ = 450 V |
| Gate to Source Charge | $Q_{GS}$ | | 4 | | nC | |
| Gate to Drain Charge | $Q_{GD}$ | | 15 | | nC | |
| Diode Forward Voltage | $V_{F(S-D)}$ | | 0.9 | | V | $I_F$ = 3 A, $V_{GS}$ = 0 |
| Reverse Recovery Time | $t_{rr}$ | | 530 | | ns | $I_F$ = 3 A<br>di/dt = 50 A/μs |
| Reverse Recovery Charge | $Q_{rr}$ | | 1.9 | | μC | |

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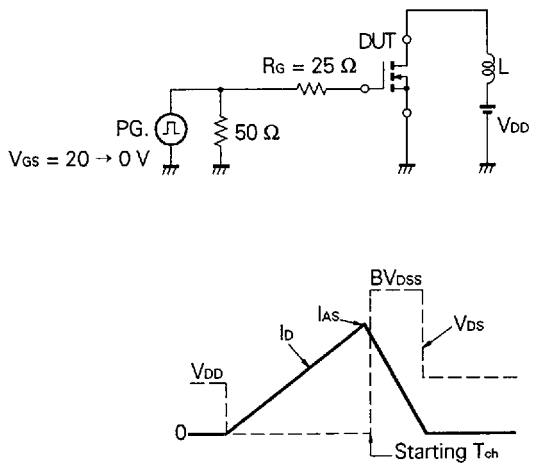
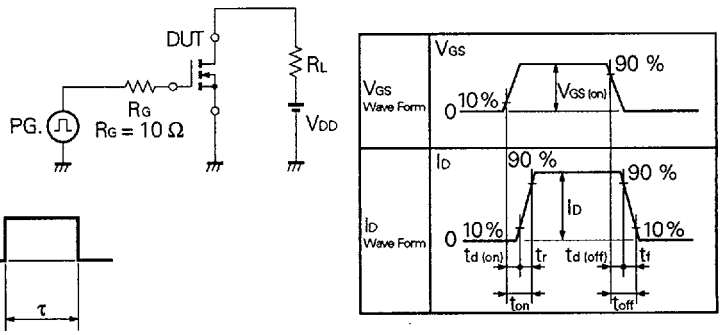
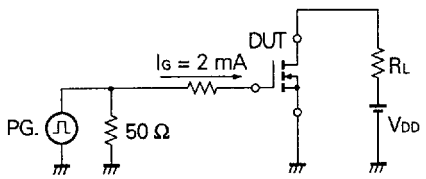
### Test Circuit 1: Avalanche Capability




### Test Circuit 2: Switching Time




### Test Circuit 3: Gate Charge



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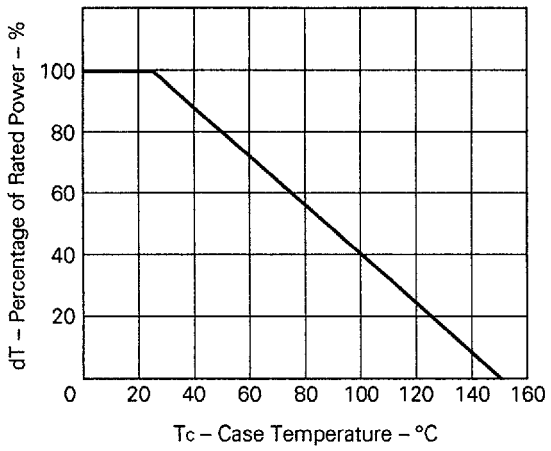
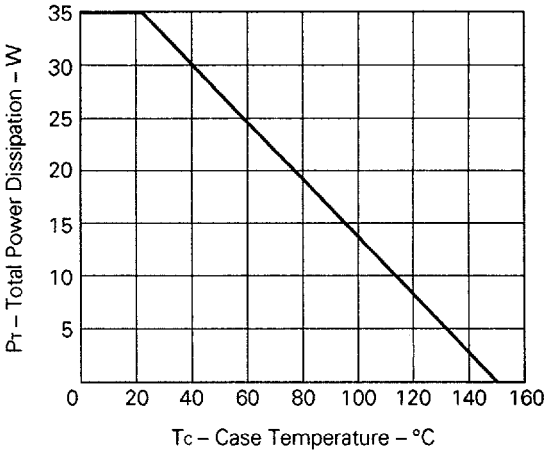
## TYPICAL CHARACTERISTICS ($T_a$ = 25 °C)

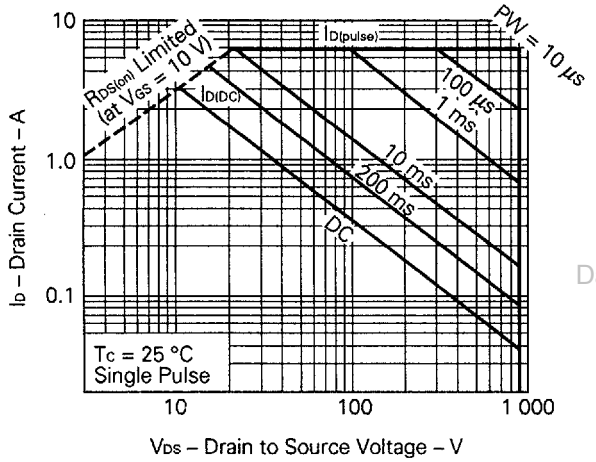
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



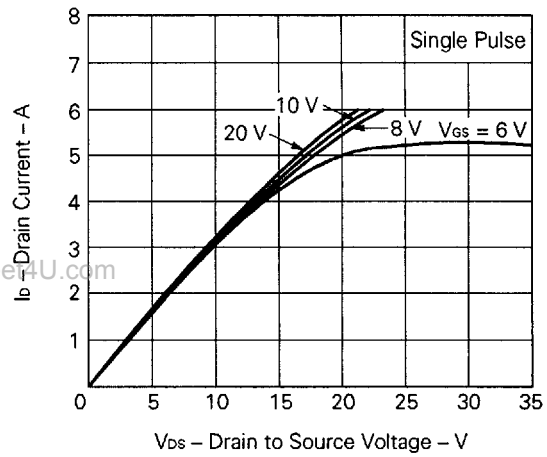

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



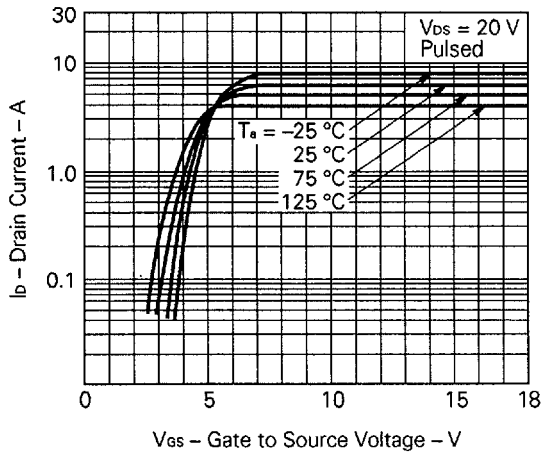

FORWARD BIAS SAFE OPERATING AREA




DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE




TRANSFER CHARACTERISTICS



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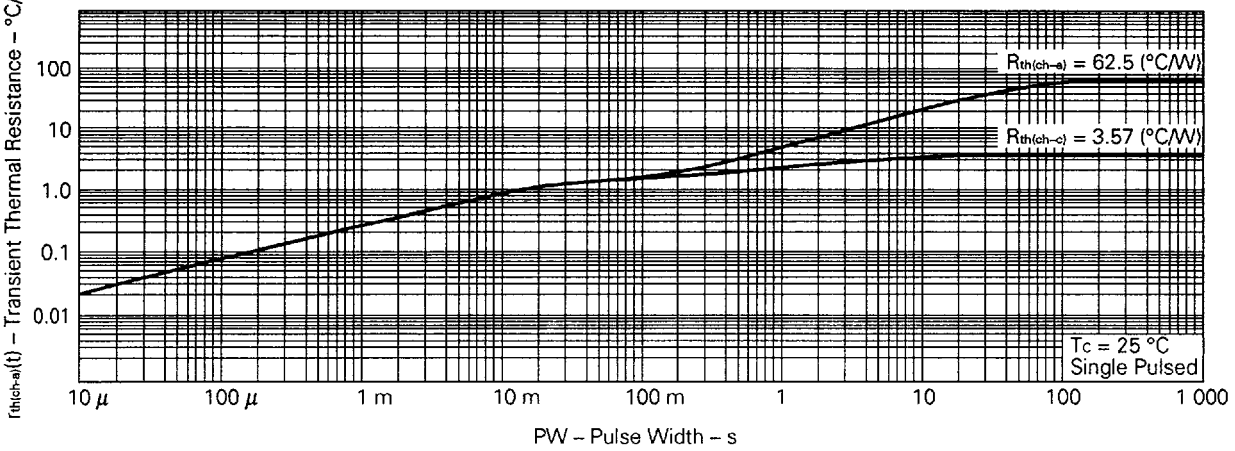
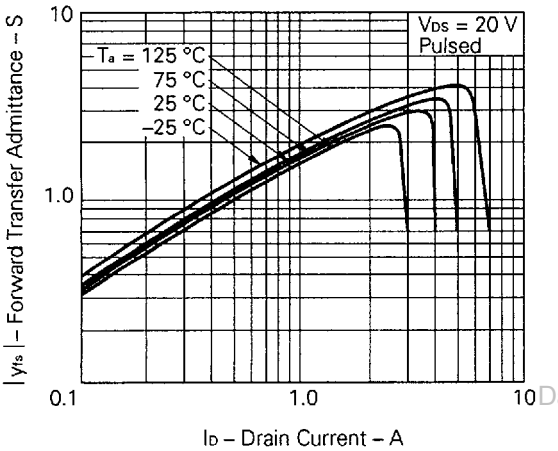
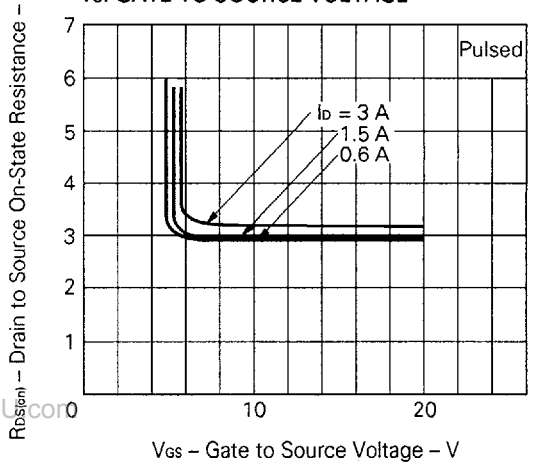
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



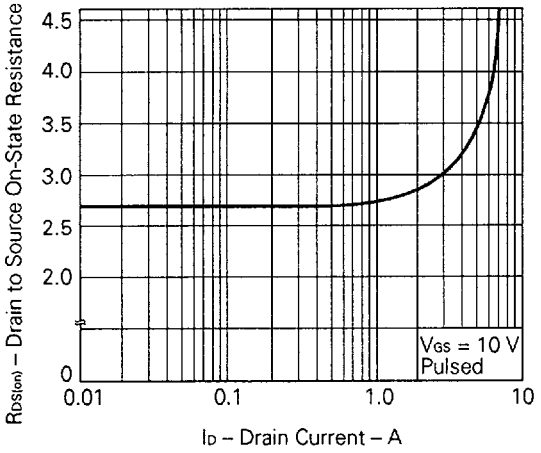

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



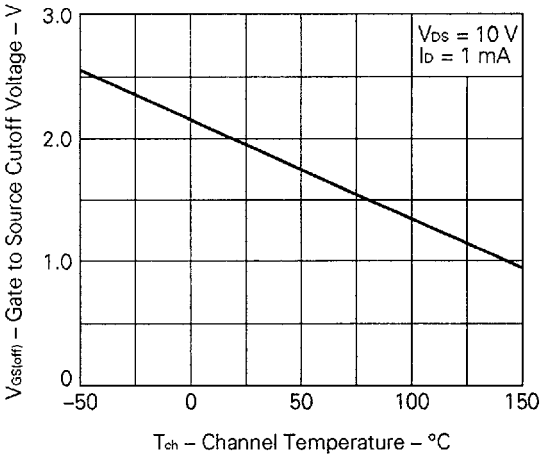

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE




DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT




GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



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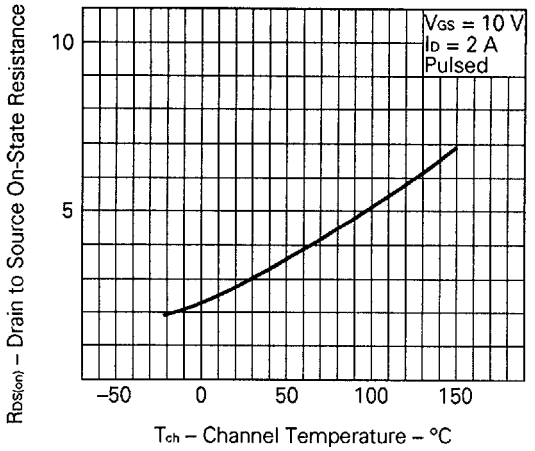
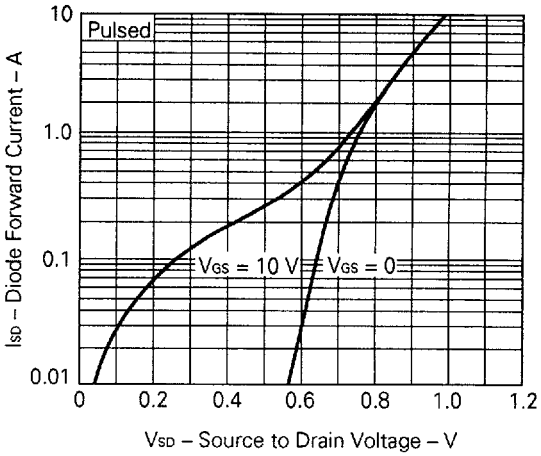
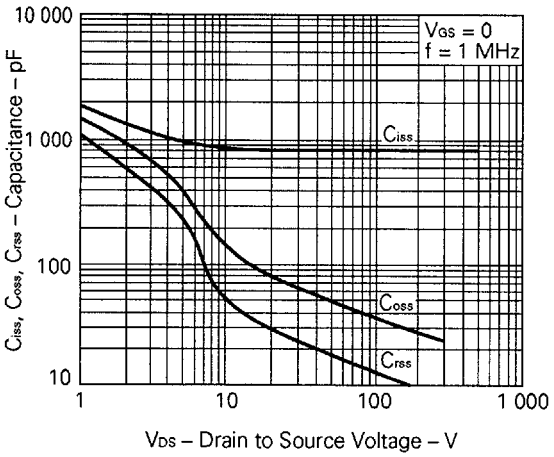
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



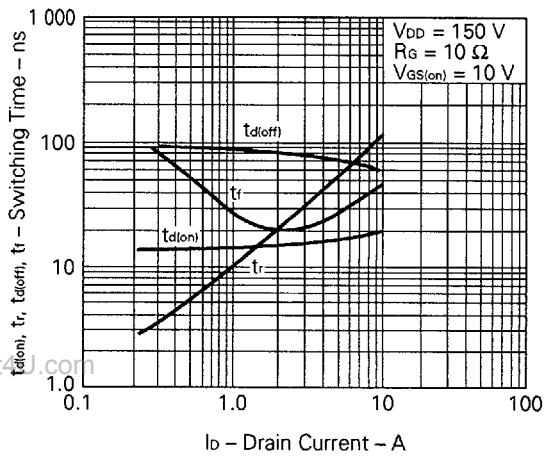

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



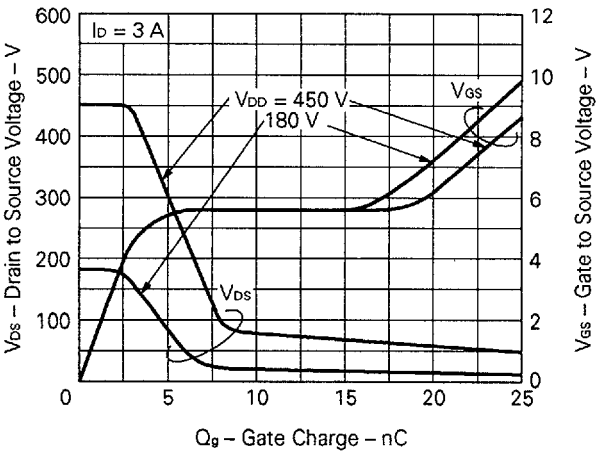

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



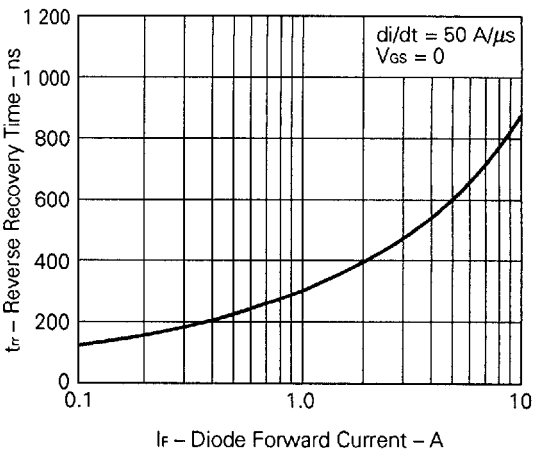

SWITCHING CHARACTERISTICS




DYNAMIC INPUT CHARACTERISTICS




REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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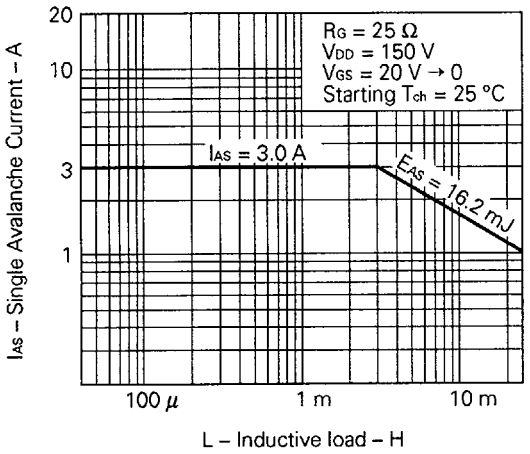
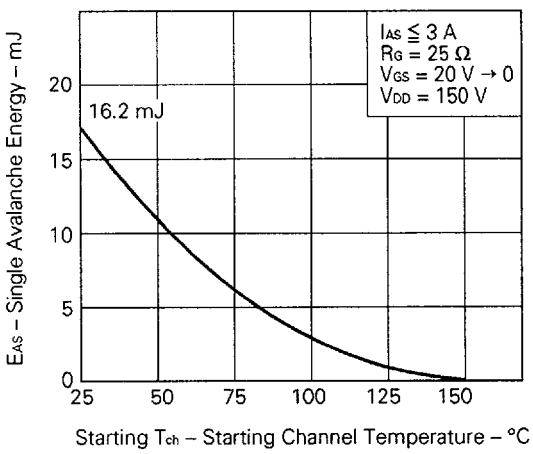
SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD




SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE

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## Reference

| Application note name | No. |
|---|---|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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