Ordering number:ENN4871

N-Channel Junction Silicon FET

2SK2171

High-Frequency, Low-Frequency Amplifier Analog Switch Applications

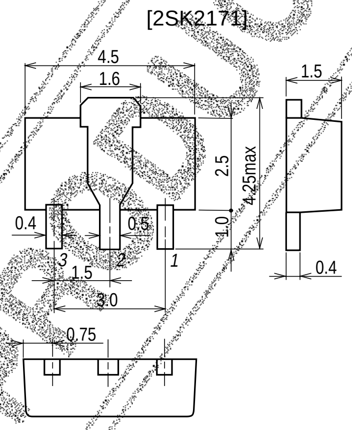
Features

- Adoption of FBET process.
- Large | y_{fs} |.
- Small Ciss.
- High P_D allowable power dissipation.

Package Dimensions

unit:mm

2125



1 : Source
2 : Gate
3 : Drain
SANYO : PCP
(Bottom View)

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSX}		40	V
Gate-to-Drain Voltage	V_{GDS}		–40	V
Gate Current	I_G		10	mA
Drain Current	I_D		100	mA
Allowable Power Dissipation	P_D		400	mW
		Mounted on ceramic board (250mm²×0.8mm)	800	mW
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gate-to-Drain Breakdown Voltage	$V_{(BR)GDS}$	I_G=–10μA, V_{DS}=0	–40			V
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=–20V, V_{DS}=0			–1.0	nA
Zero-Gate Voltage Drain Current	I_{DSS}**	V_{DS}=10V, V_{GS}=0	40*		75*	mA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=100μA	–2.0	–3.0	–5.0	V
Forward Transfer Admittance	| yfs |1	V_{DS}=10V, I_D=10mA, f=1kHz	10	15		mS
	| yfs |2	V_{DS}=10V, V_{GS}=0, f=1kHz	22	30		mS

** : Pulse Test Pulse Width≤2mS

Continued on next page.

* : The 2SK2171 is classified by I_{DSS} as follows : (unit : mA)

40	3	52	48	4	63	57	5	75

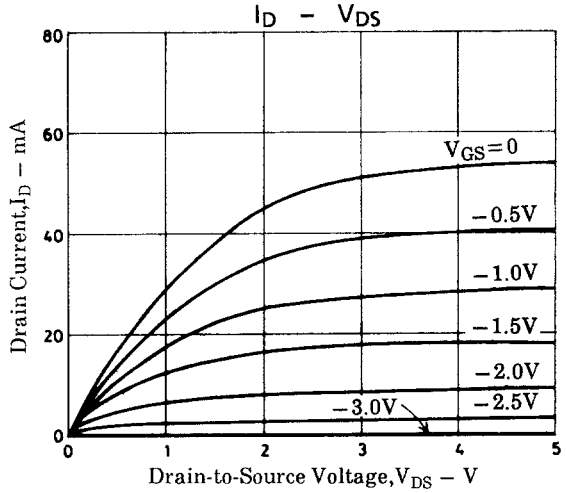
Marking : KM

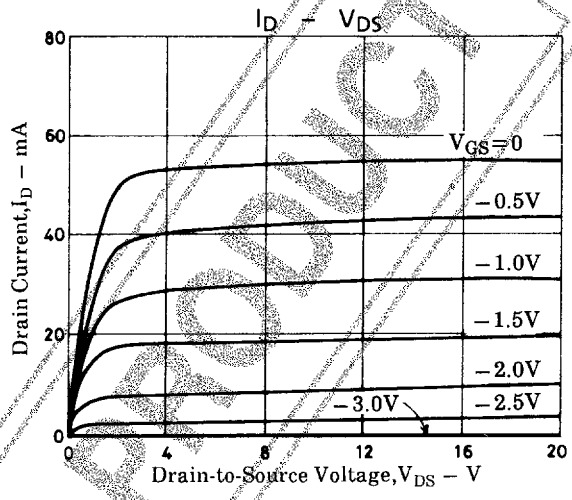
I_{DSS} rank : 3, 4, 5

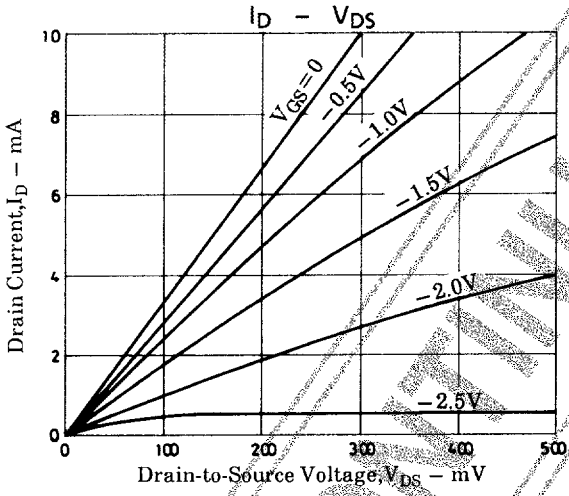
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

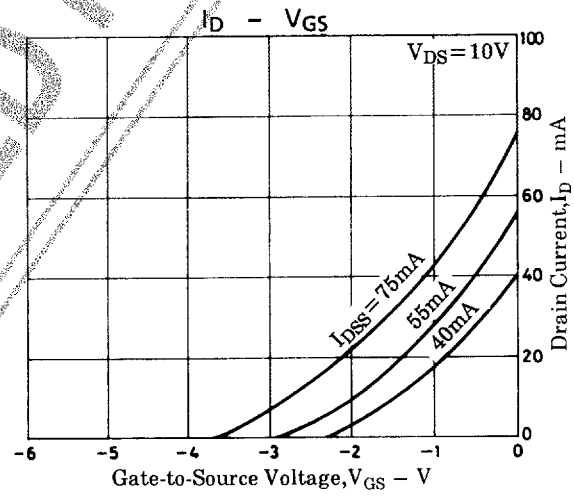
Continued from preceding page.

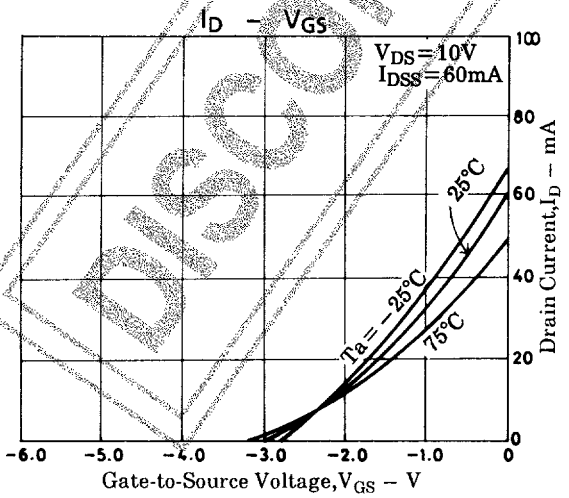
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz		11		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, V_{GS}=0, f=1MHz		2.5		pF
Noise Figure	NF	V_{DS}=10V, Rg=1kΩ, I_D=1mA, f=1kHz		1.5		dB
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	V_{DS}=10mV, V_{GS}=0		30		Ω

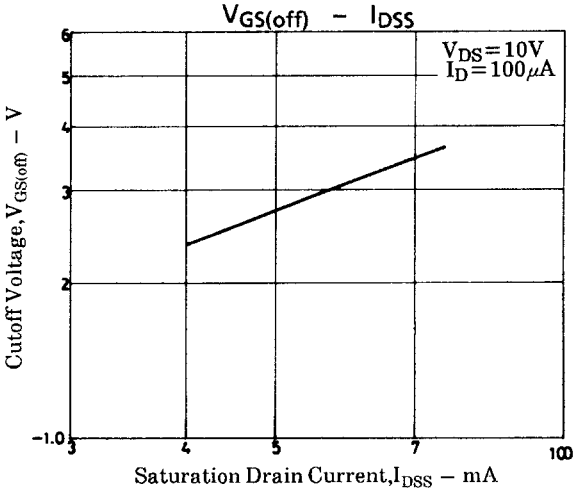




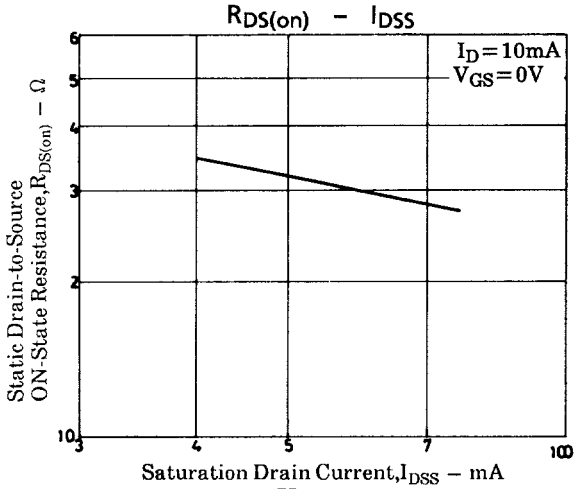




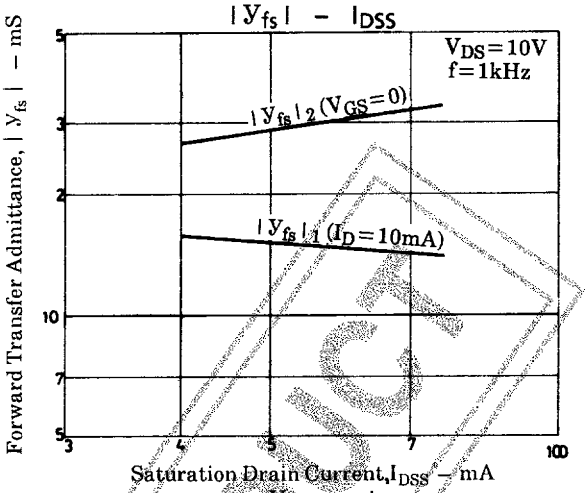




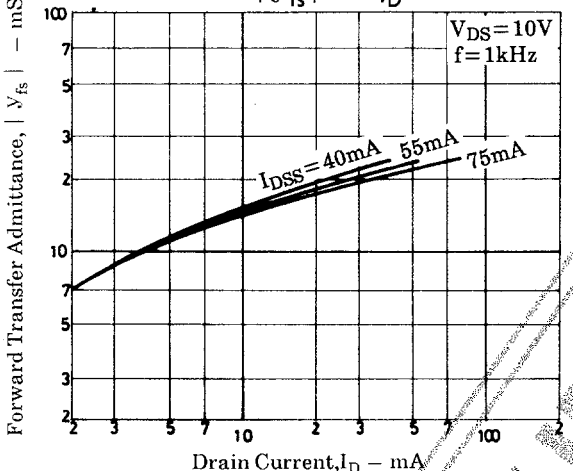
$R_{DS(on)}$ – I_{DSS}



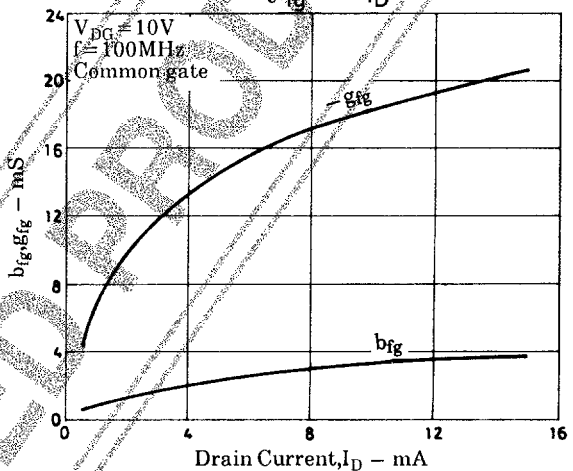
$|y_{fs}|$ – I_{DSS}



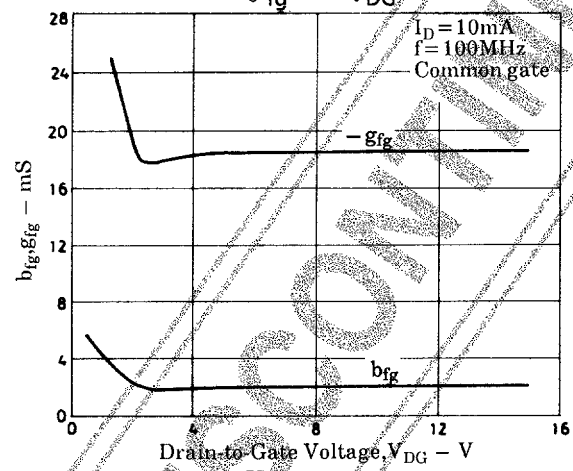
$|y_{fs}|$ – I_D



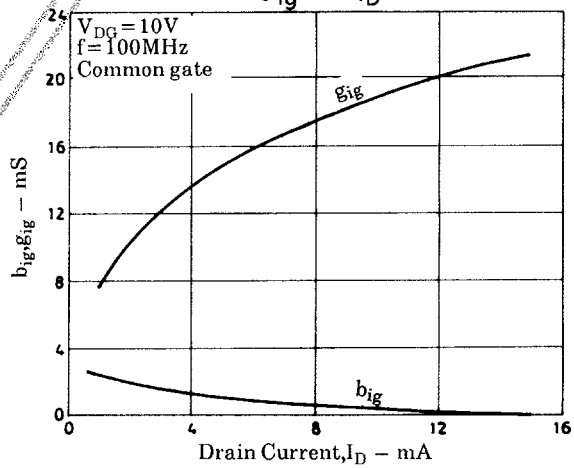
y_{fg} – I_D



y_{fg} – V_{DG}



y_{ig} – I_D



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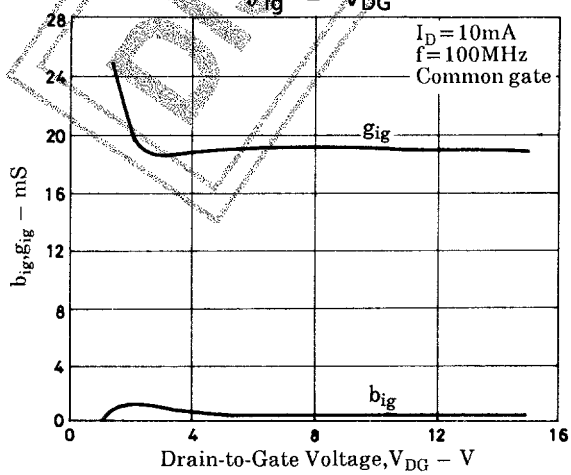
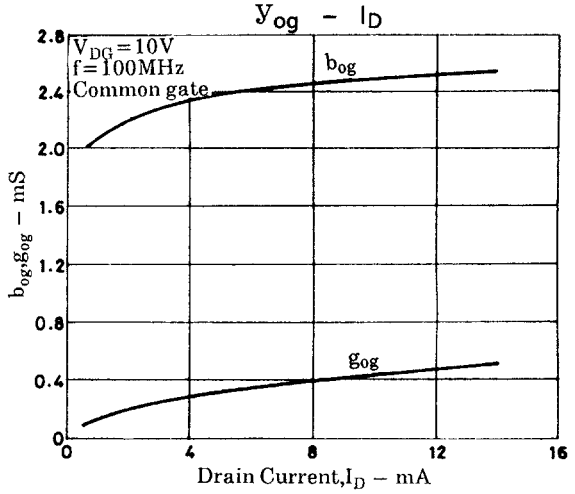
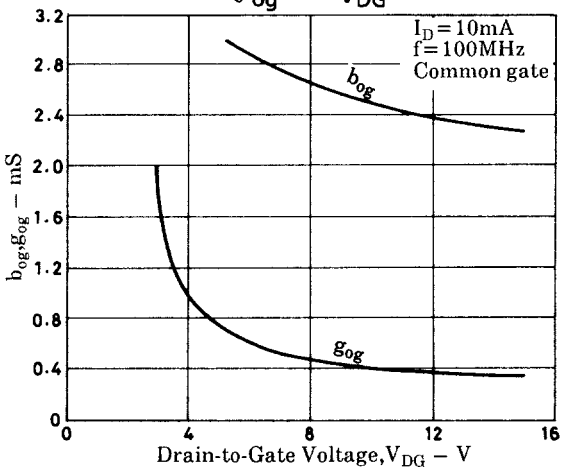


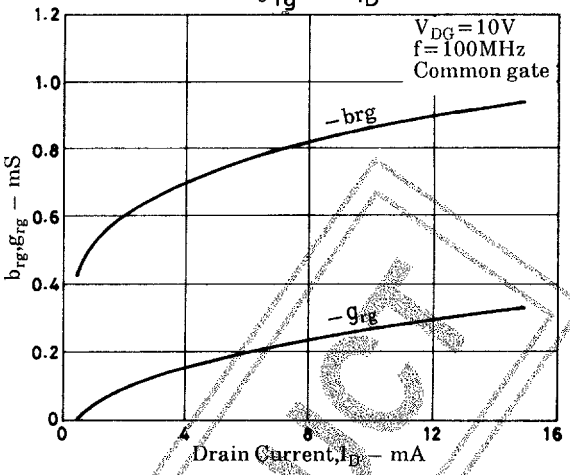
y_{og} – I_D



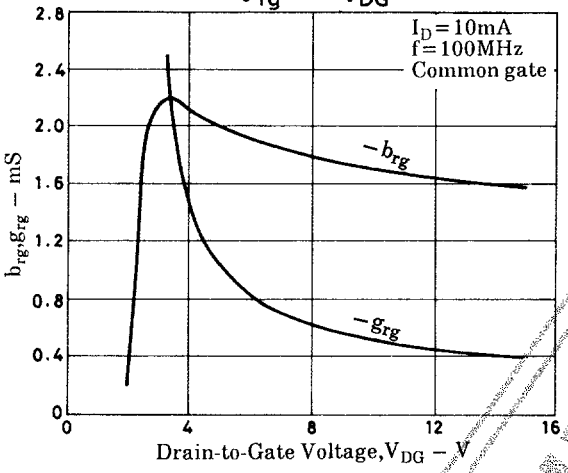
y_{og} – V_{DG}



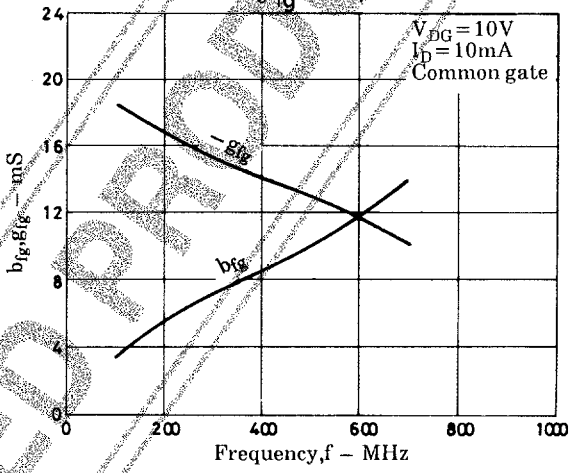
y_{rg} – I_D



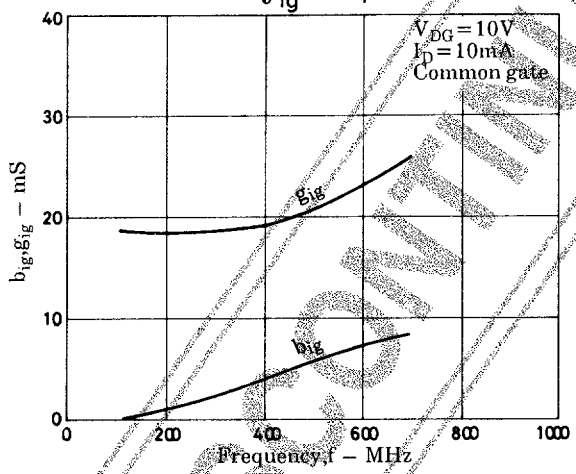
y_{rg} – V_{DG}



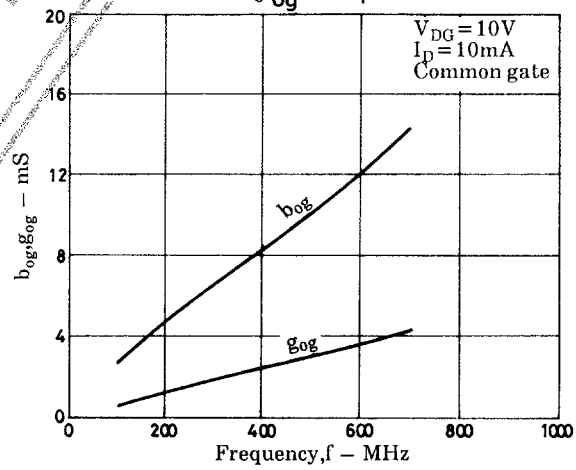
y_{fg} – f



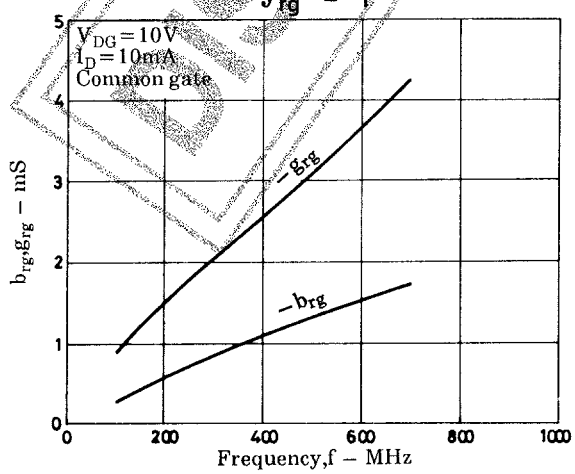
y_{ig} – f



y_{og} – f



y_{rg} – f



Ciss – V_{DS}