Ordering number:EN695G

N-Channel Junction Silicon FET

2SK242

Low-Frequency General-Purpose Amplifier Applications

Features

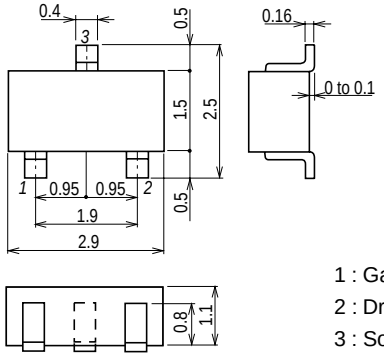
- Ultrasmall-sized package permitting 2SK242-applied sets to be made small and slim.
- Small Crss (Crss=0.04pF typ).

Package Dimensions

unit:mm

2024B

[2SK242]



1 : Gate
2 : Drain
3 : Source
SANYO : CP

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Gate-to-Drain Voltage	V_{GDO}		–20	V
Gate Current	I_G		10	mA
Drain Current	I_D		20	mA
Allowable Power Dissipation	P_D		150	mW
Junction Temperature	Tj		125	˚C
Storage Temperature	Tstg		–55 to +125	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gate-to-Drain Breakdown Voltage	$V_{(BR)GDO}$	I_G=–10μA	–20			V
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=–0.5V, V_{DS}=0			–10	nA
Zero-Gate Voltage Drain Current	I_{DSS}*	V_{DS}=5V, V_{GS}=0	0.6*		12.0*	mA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=5V, I_D=10μA			–2.5	V
Forward Transfer Admittance	| yfs |1	V_{DS}=5V, V_{GS}=0, f=1kHz	2.0	6.0		mS
	| yfs |2	V_{DS}=5V, V_{GS}=0, f=100MHz	2.0	6.0		mS
Input Capacitance	Ciss	V_{DS}=5V, V_{GS}=0, f=1MHz		4.0		pF
Output Capacitance	Coss	V_{DS}=5V, V_{GS}=0, f=1MHz		4.0		pF
Reverse Transfer Capacitance	Crss	V_{DS}=5V, V_{GS}=0, f=1MHz		0.04	0.15	pF

* : The 2SK242 is classified by I_{DSS} as follows : (unit : mA).

Continued on next page.

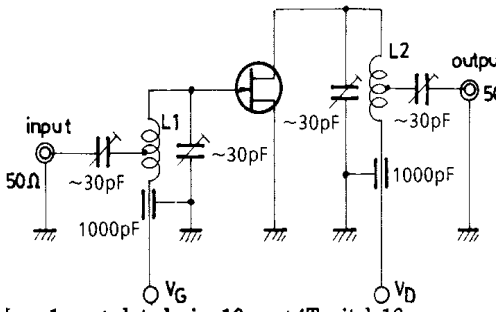
0.6	2	1.5	1.2	3	3.0	2.5	4	6.0	5.0	5	12.0

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

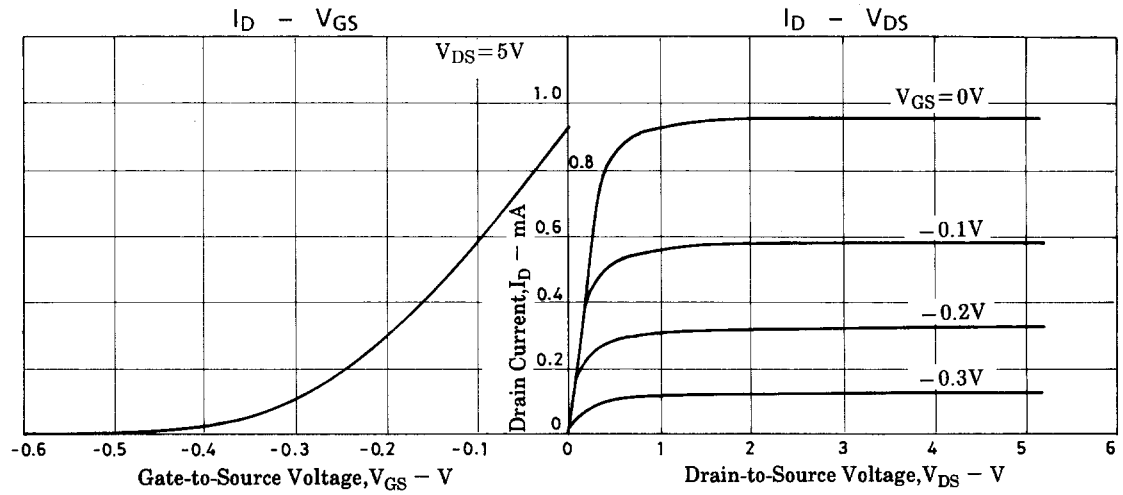
Parameter	Symbol	Conditions	Ratings			Unit
Power Gain	PG	V_{DS}=5V, V_{GS}=0, f=100MHz, See specified Test Circuit		24		dB
Noise Figure	NF	See specified Test Circuit		3.5	6.0	dB

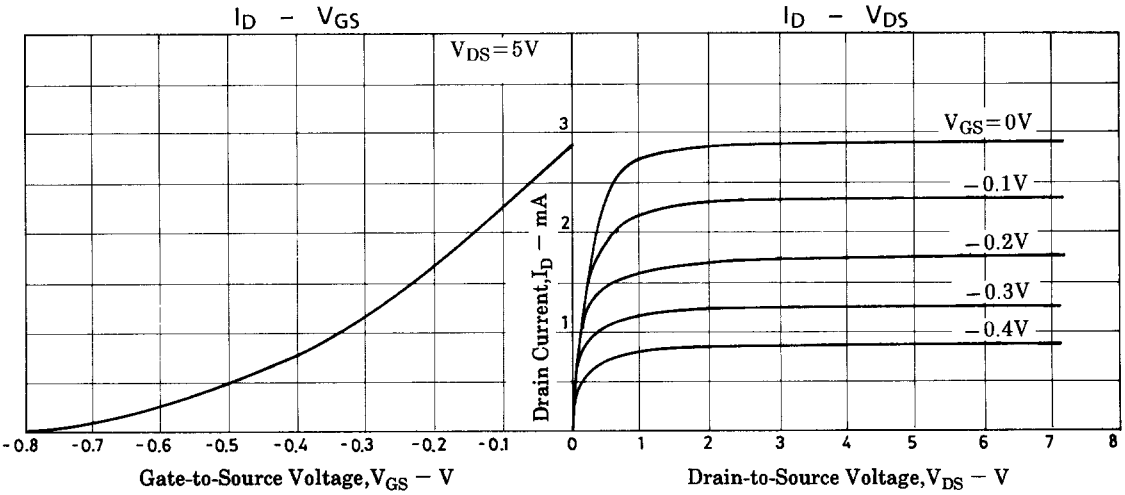
PG, NF Specified Test Circuit



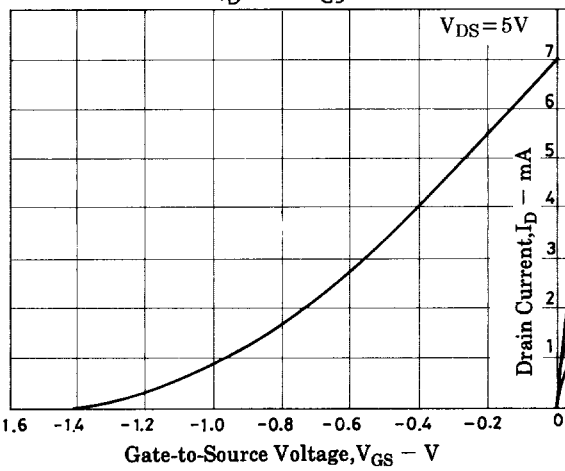
L_1 : 1mmø plated wire 10mmø 4T, pitch 18mm, tap : 1T from gate side

L_2 : 1mmø plated wire 10mmø 6T, pitch 10mm, tap : 1T from drain side

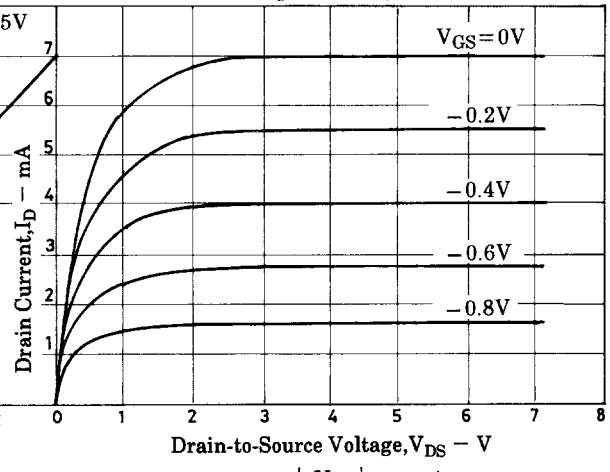




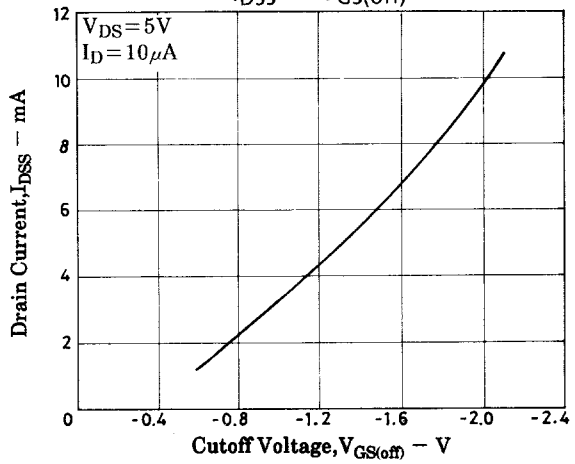
I_D – V_{GS}



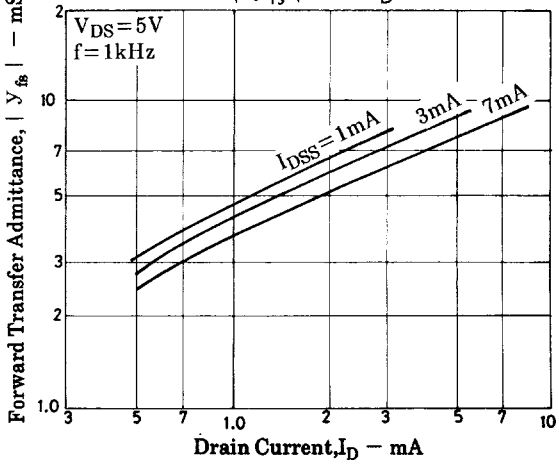
I_D – V_{DS}



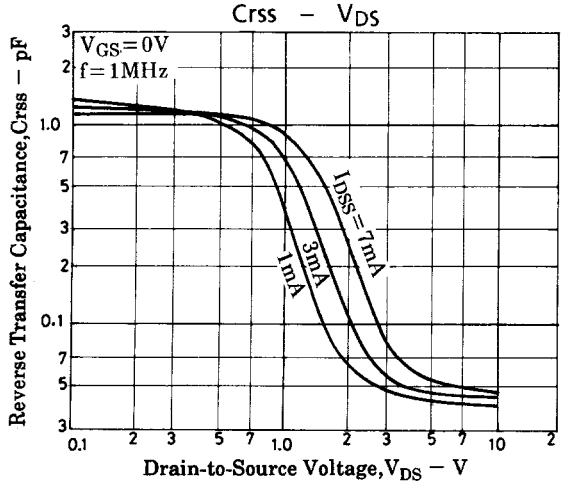
I_{DSS} – $V_{GS(off)}$



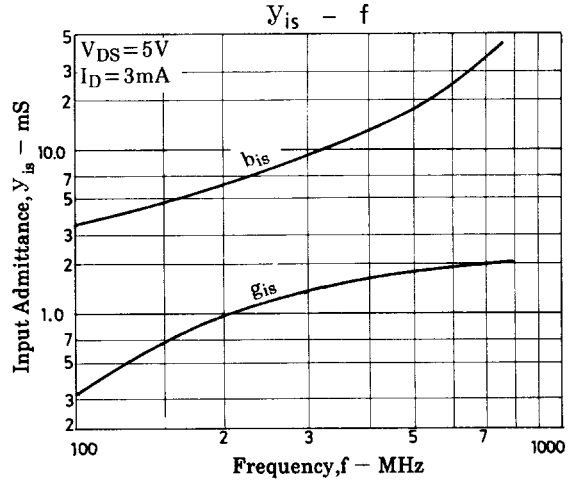
$|y_{fs}|$ – I_D



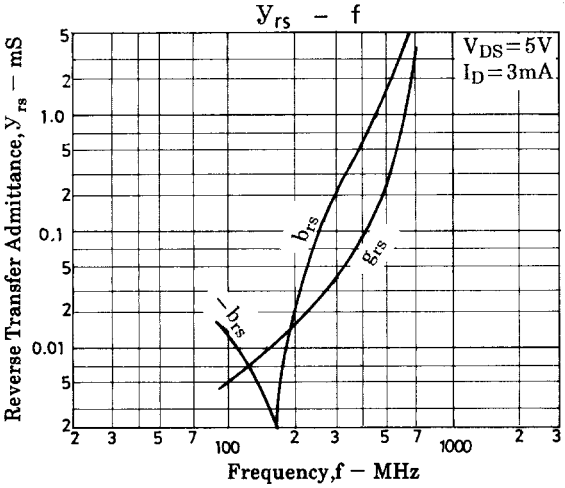
Crss – V_{DS}



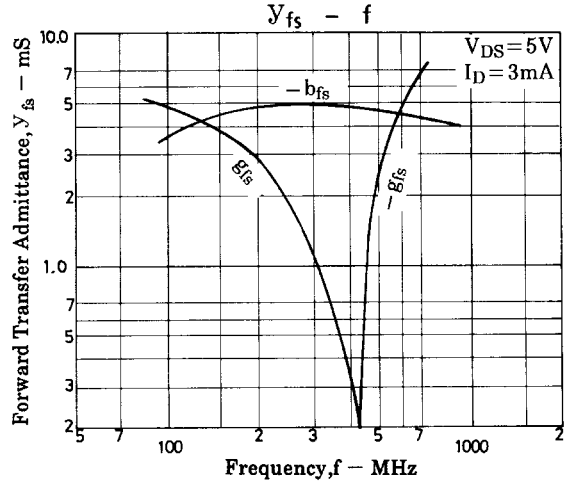
y_{is} – f



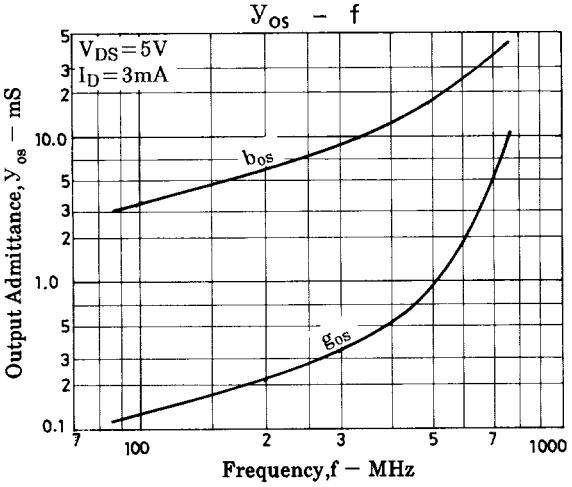
y_{rs} – f



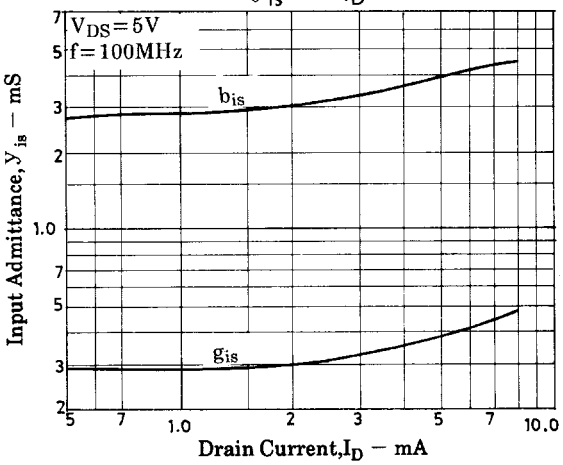
y_{fs} – f



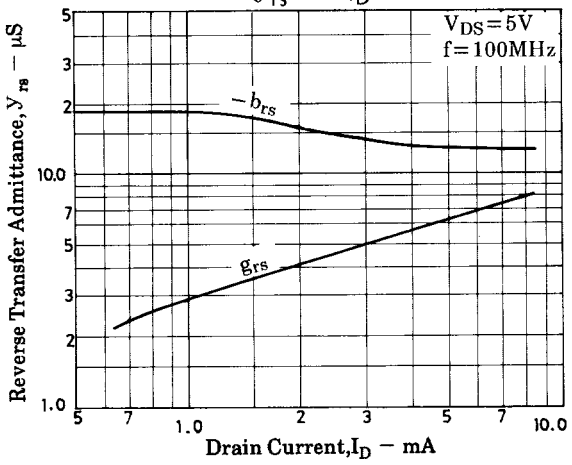
y_{os} – f



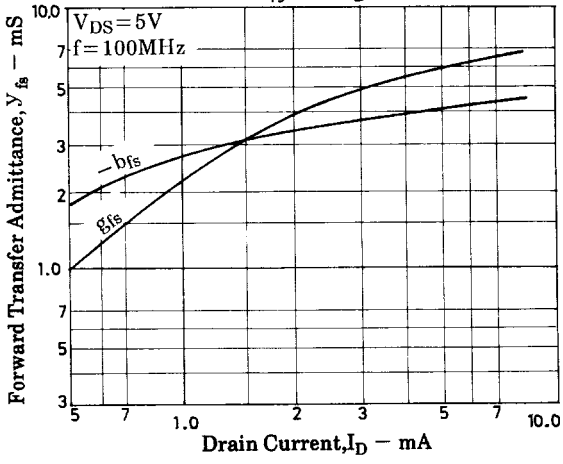
y_{is} – I_D



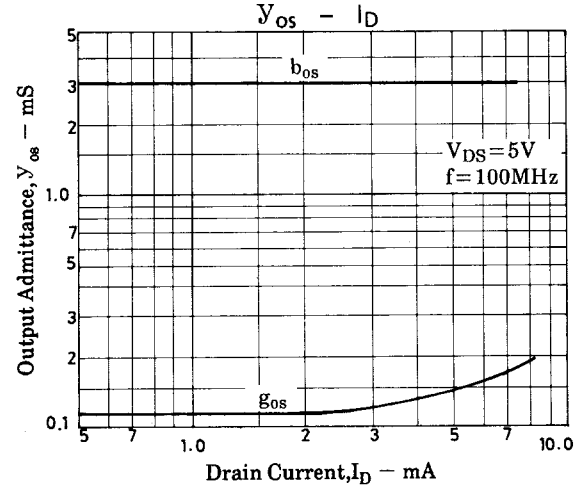
y_{rs} – I_D



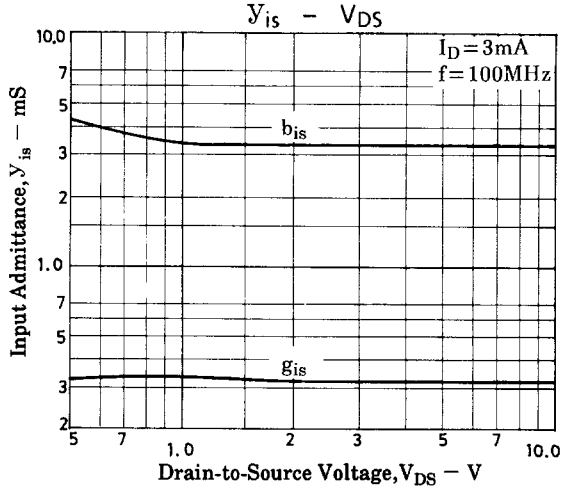
y_{fs} – I_D



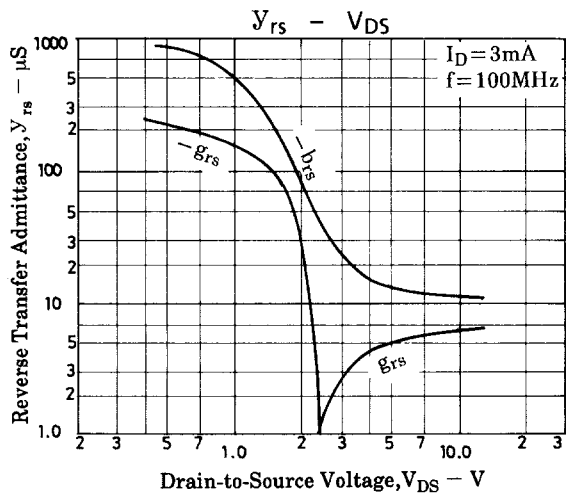
y_{os} – I_D



y_{is} – V_{DS}



y_{rs} – V_{DS}



y_{fs} – V_{DS}