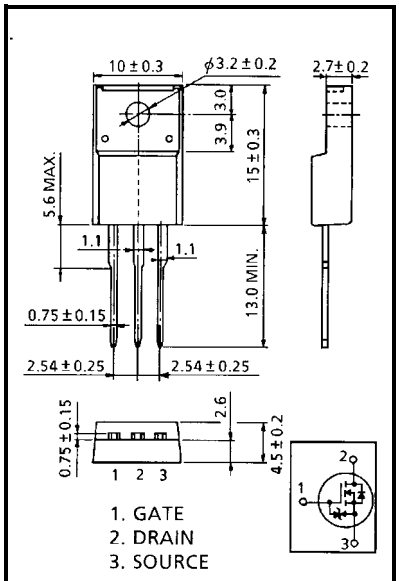
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U−MOS)

2SK2466

Chopper Regulator, DC−DC Converter and Motor Drive Applications

- 4 V gate drive
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 34 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 30 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement−mode : V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10R1B

Weight: 1.9 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	100	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	30	A
	Pulse (Note 1)	I_{DP}	120	
Drain power dissipation (Tc = 25°C)		P_D	40	W
Single pulse avalanche energy (Note 2)		E_{AS}	293	mJ
Avalanche current		I_{AR}	30	A
Repetitive avalanche energy (Note 3)		E_{AR}	4	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

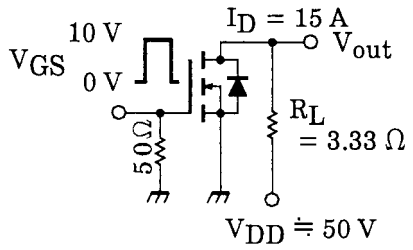
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	3.125	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W

Note 1: Please use devices on condition that the channel temperature is below 150°C.
Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 525 μH, R_G = 25 Ω, I_{AR} = 30 A
Note 3: Repetitive rating; Pulse width limited by maximum channel temperature.

This transistor is an electrostatic sensitive device.
Please handle with caution.

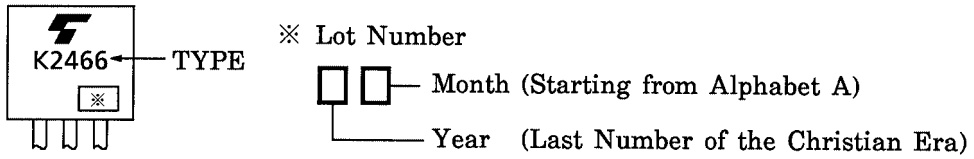
Electrical Characteristics (Ta = 25°C)

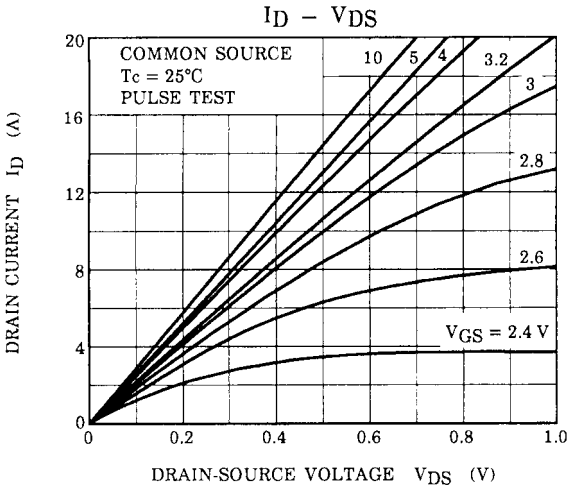
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 15 A	—	40	70	mΩ
			V_{GS} = 10 V, I_D = 15 A	—	34	46	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 15 A	13	30	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	3250	—	pF
Reverse transfer capacitance		C_{rss}		—	230	—	
Output capacitance		C_{oss}		—	520	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	33	—	ns
	Turn−on time	t_{on}		—	60	—	
	Fall time	t_f		—	95	—	
	Turn−off time	t_{off}		—	230	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 30 A	—	68	—	nC
Gate−source charge		Q_{gs}		—	46	—	
Gate−drain (“miller”) charge		Q_{gd}		—	22	—	

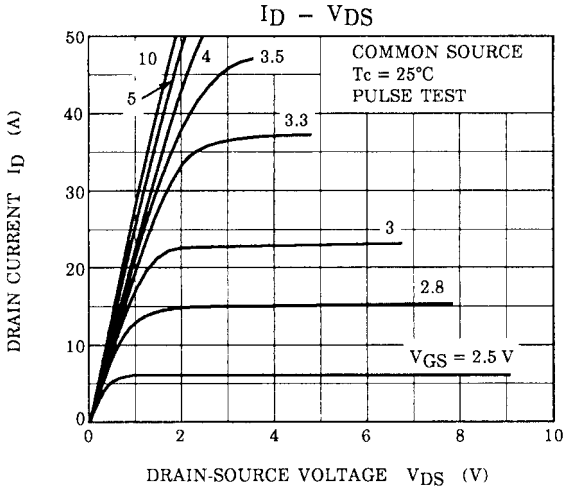
Source−Drain Ratings and Characteristics (Ta = 25°C)

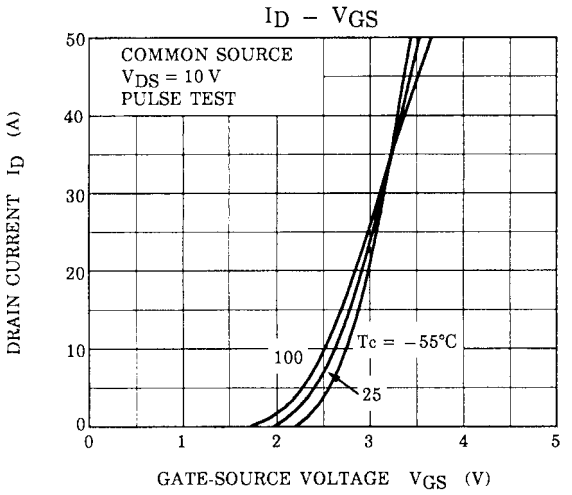
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	30	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	120	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 30 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 30 A, V_{GS} = 0 V dI_{DR} / dt = 50 A / μs	—	120	—	ns
Reverse recovery charge	Q_{rr}		—	280	—	μC

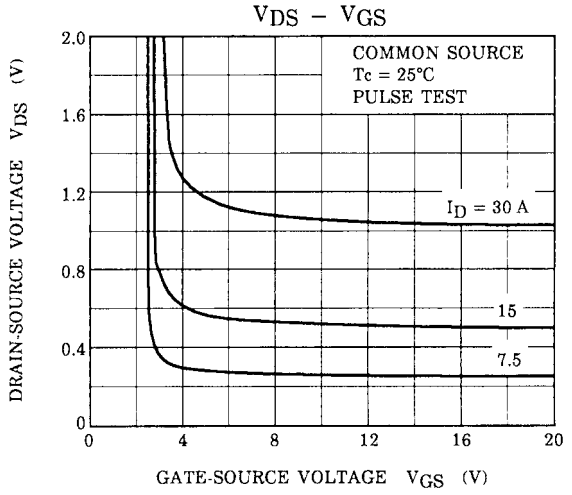
Marking

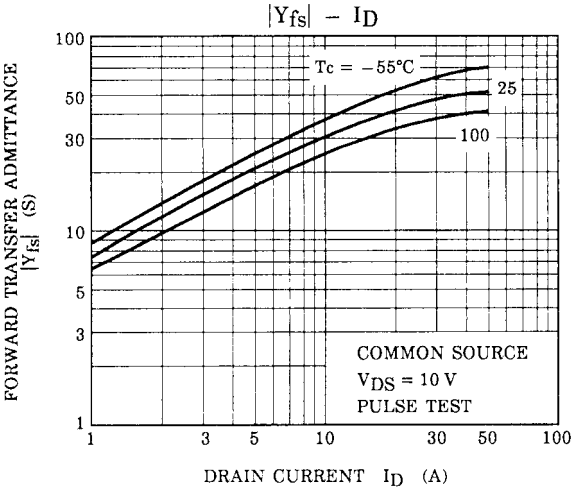


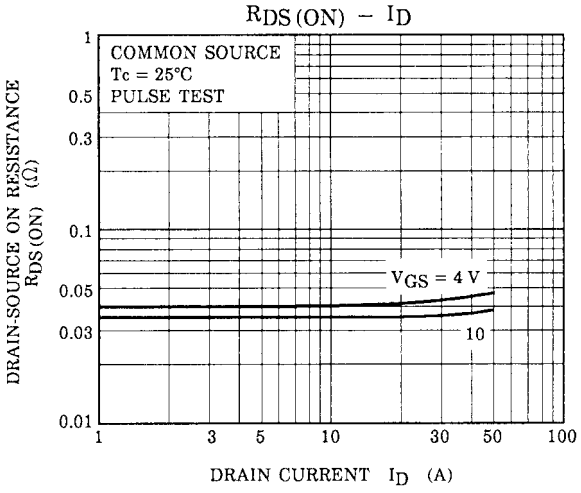

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
5
4
3.2
3
2.8
2.6
V_{GS} = 2.4 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
5
4
3.5
3.3
3
2.8
V_{GS} = 2.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)

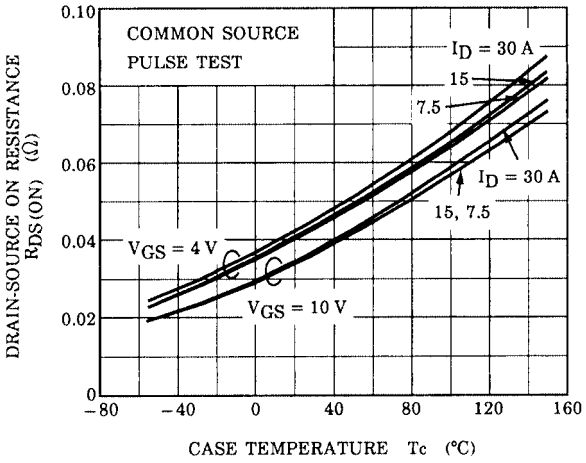

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
100
Tc = −55°C
25
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)


V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 30 A
15
7.5
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)

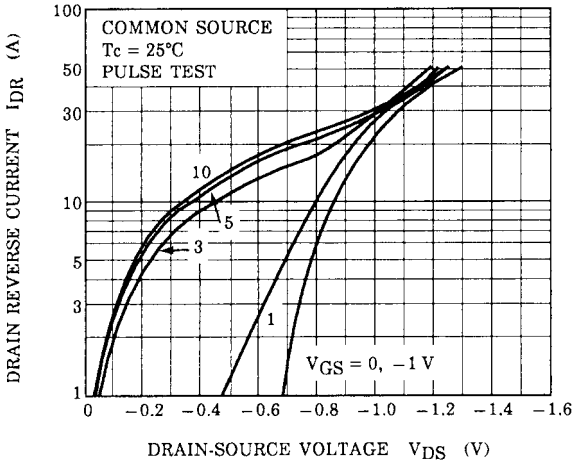

$|Y_{fs}|$ – I_D
Tc = −55°C
25
100
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS(ON)}$ – I_D
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = 4 V
10
DRAIN-SOURCE ON RESISTANCE $R_{DS(ON)}$ (Ω)
DRAIN CURRENT I_D (A)

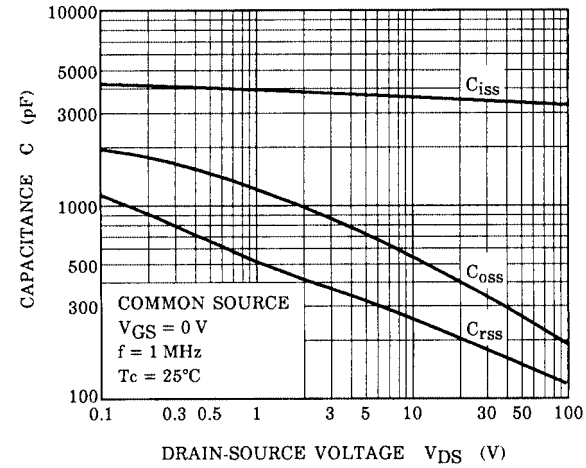
$R_{DS(ON)}$ – Tc



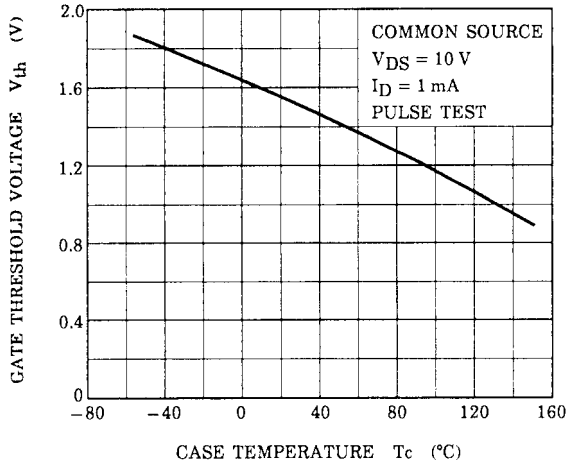
I_{DR} – V_{DS}



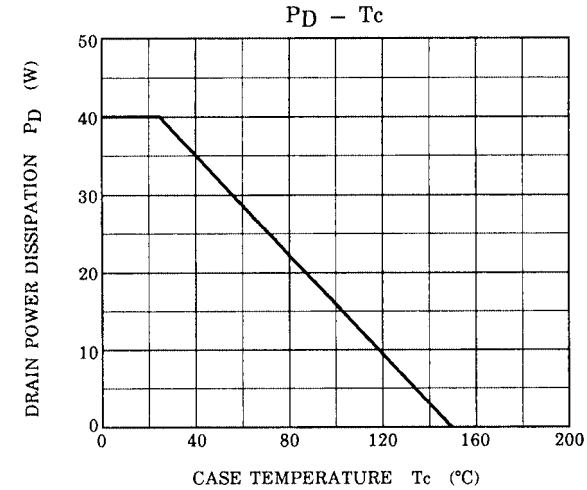
CAPACITANCE – V_{DS}



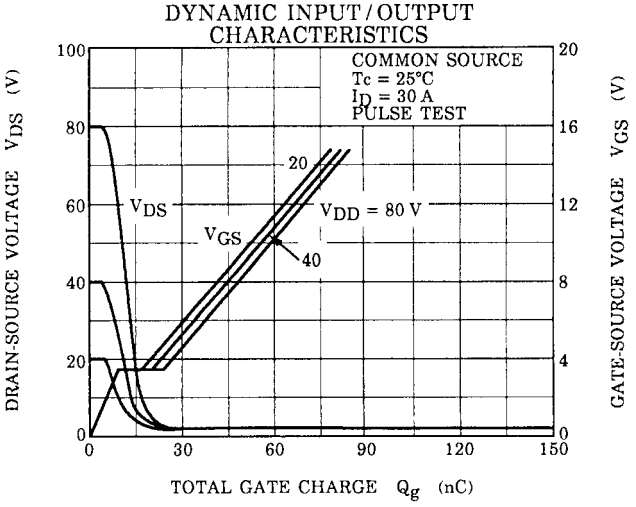
V_{th} – Tc

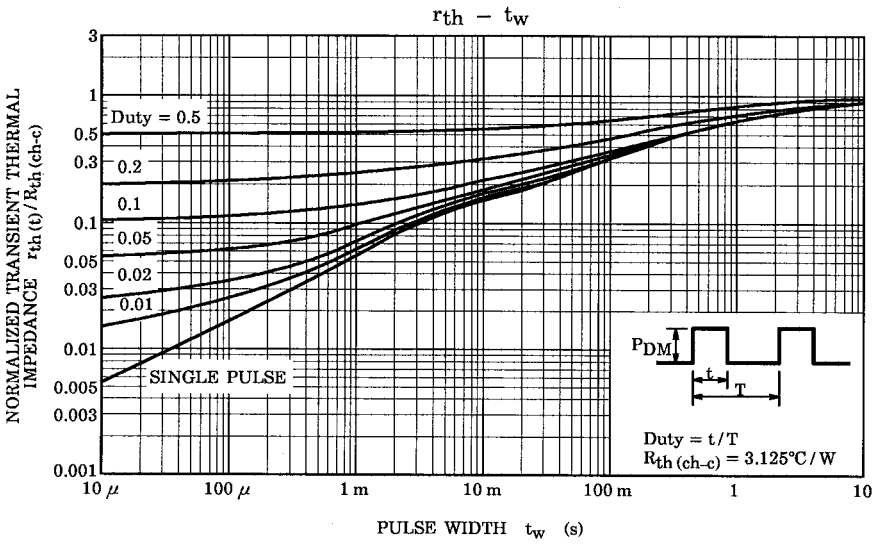


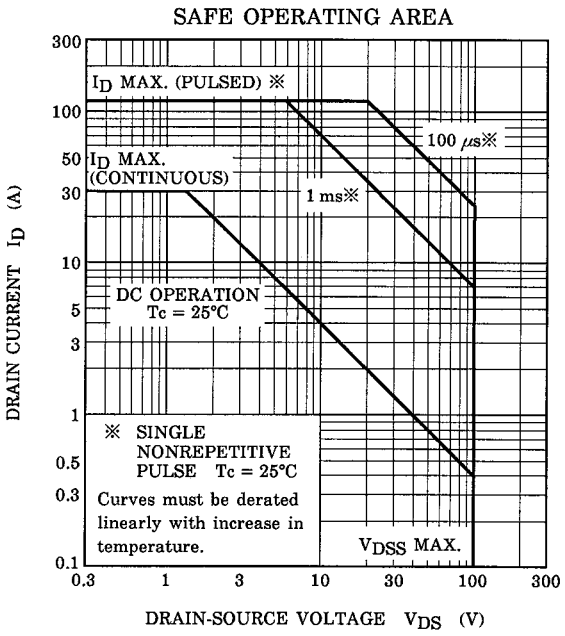
P_D – Tc

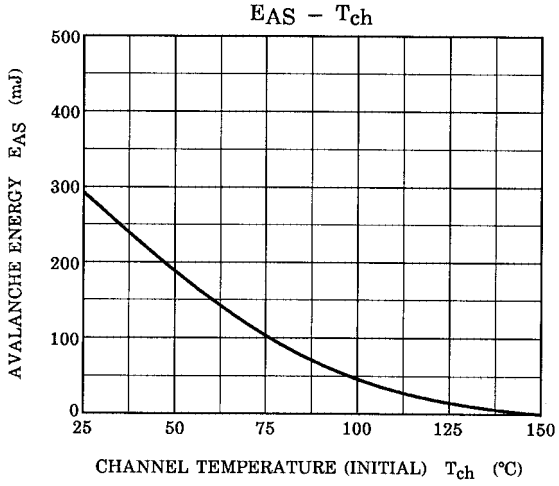


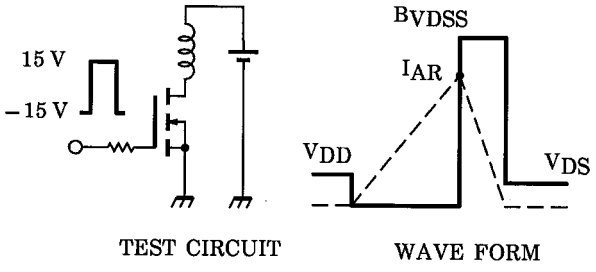
DYNAMIC INPUT / OUTPUT CHARACTERISTICS











$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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