

# 2SK2932

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

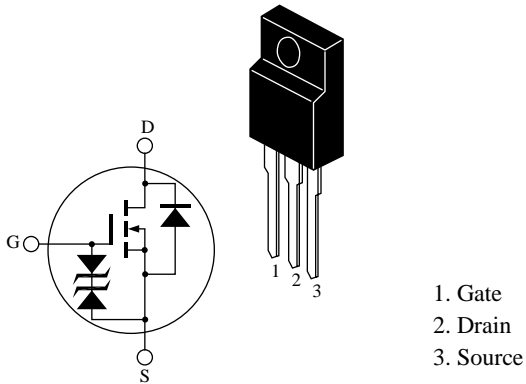
ADE-208-555B (Z)  
3rd. Edition  
Jun 1998

## Features

- Low on-resistance  
 $R_{DS} = 0.055 \Omega$  typ.
- High speed switching
- 4V gate drive device can be driven from 5V source

## Outline

TO-220CFM



**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	10	A
Drain peak current	$I_{D(pulse)}^{Note1}$	40	A
Body-drain diode reverse drain current	$I_{DR}$	10	A
Avalanche current	$I_{AP}^{Note3}$	10	A
Avalanche energy	$E_{AR}^{Note3}$	8.5	mJ
Channel dissipation	$P_{ch}^{Note2}$	20	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

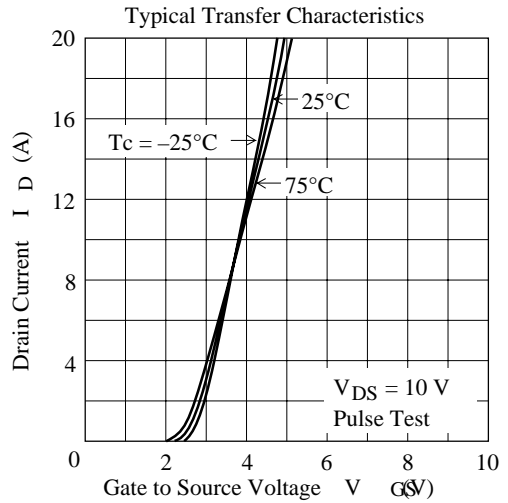
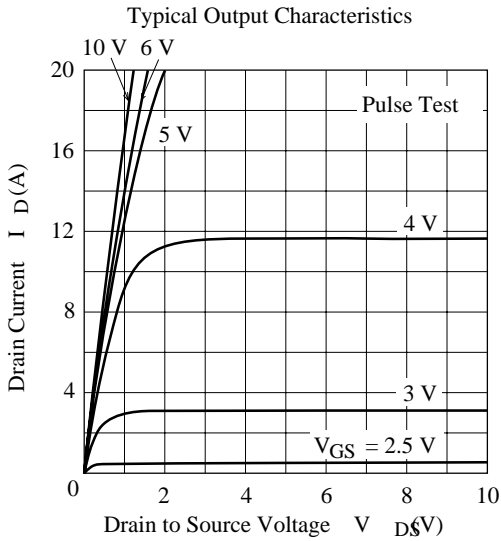
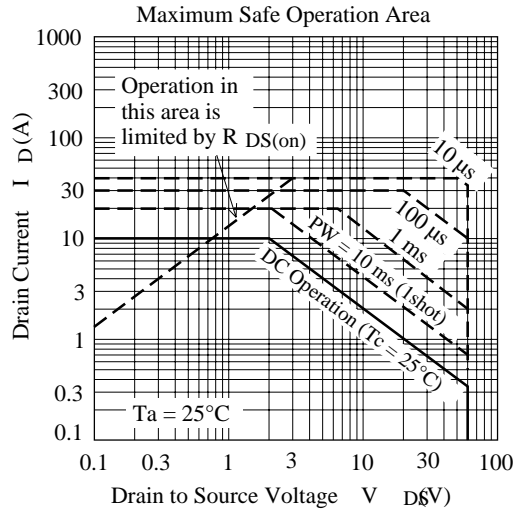
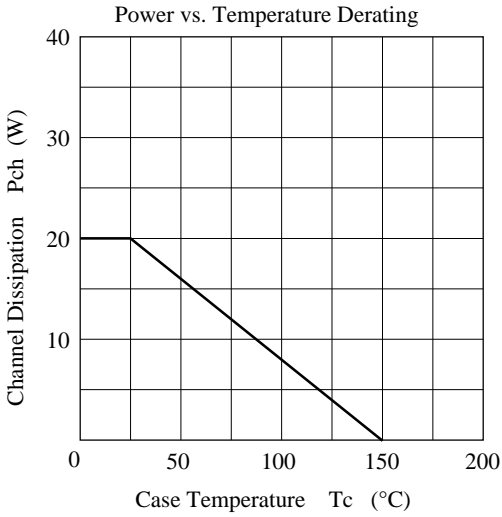
Note: 1.  $PW \leq 10\mu\text{s}$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ\text{C}$   
3. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50\Omega$

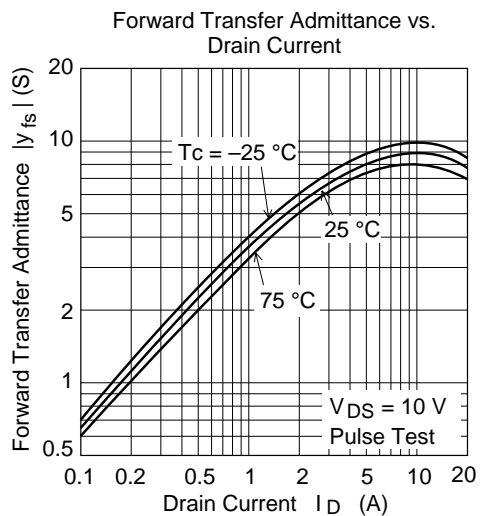
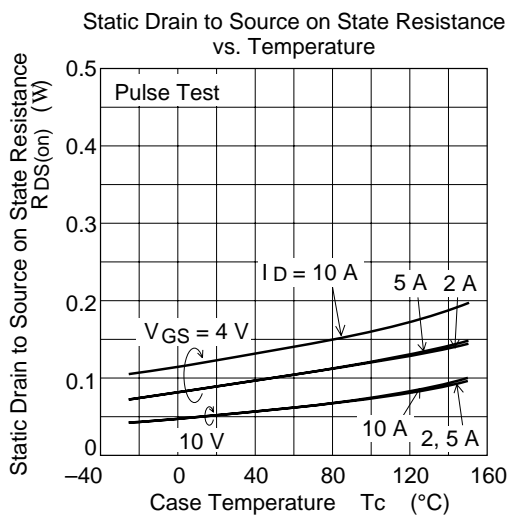
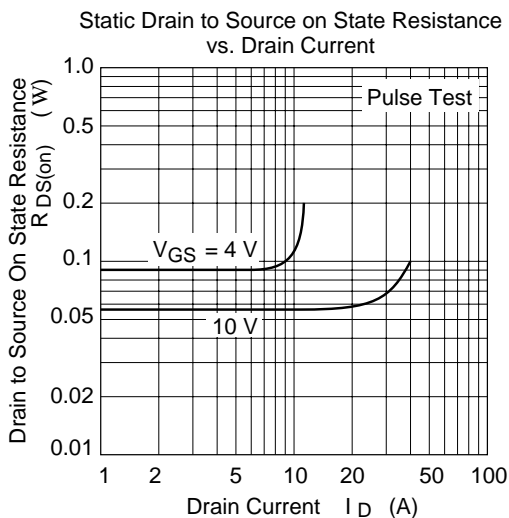
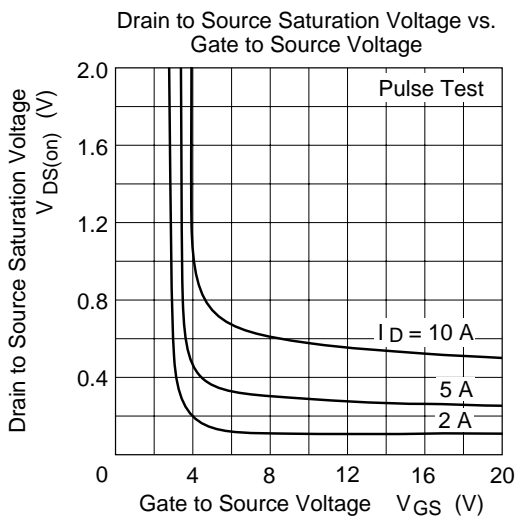
## Electrical Characteristics (Ta = 25°C)

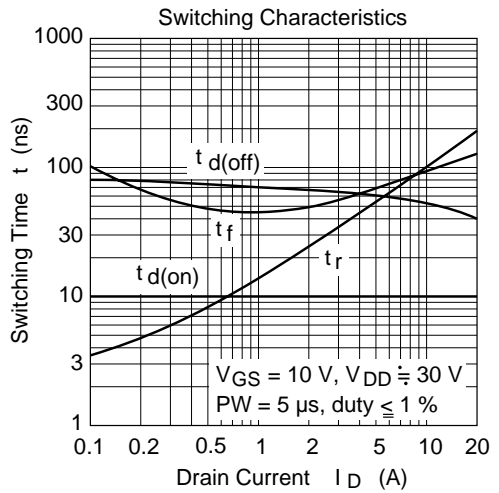
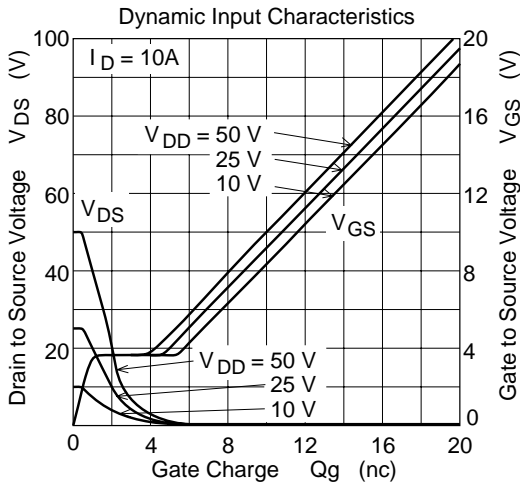
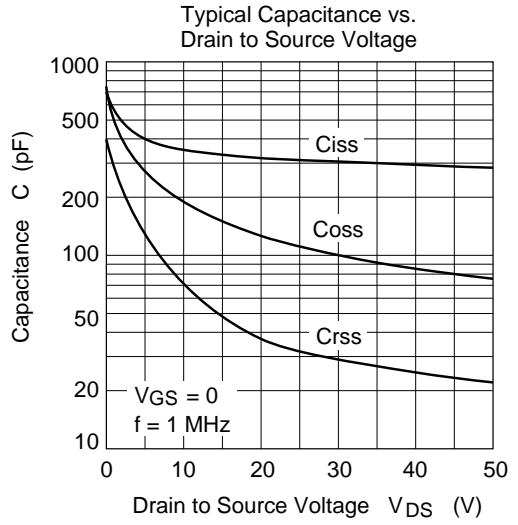
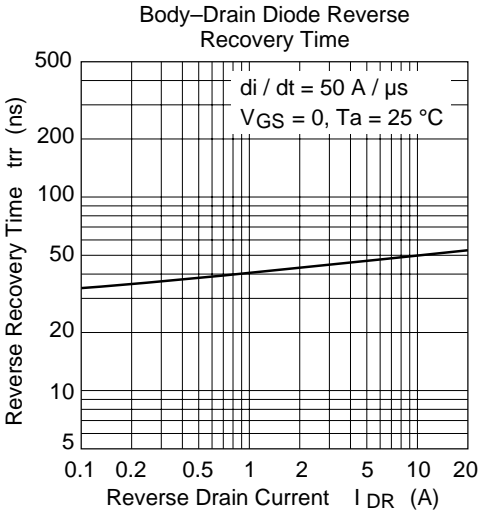
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1\text{mA}$ , $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.075	$\Omega$	$I_D = 5\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.090	0.150	$\Omega$	$I_D = 5\text{A}$ , $V_{GS} = 4\text{V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	5	8	—	S	$I_D = 5\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	350	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	$C_{oss}$	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	70	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = 5\text{A}$ , $V_{GS} = 10\text{V}$
Rise time	$t_r$	—	55	—	ns	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	
Fall time	$t_f$	—	70	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	—	V	$I_F = 10\text{A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = 10\text{A}$ , $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

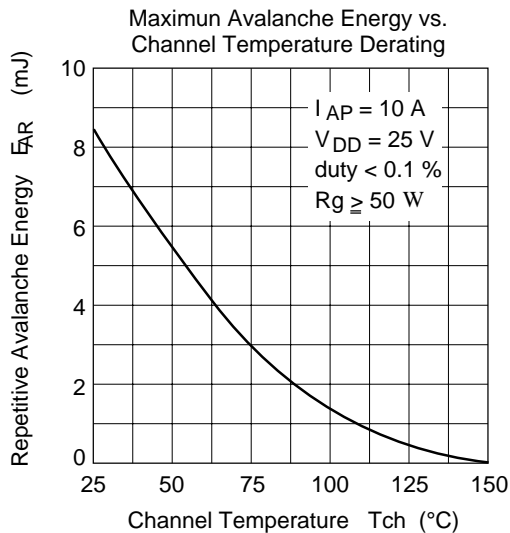
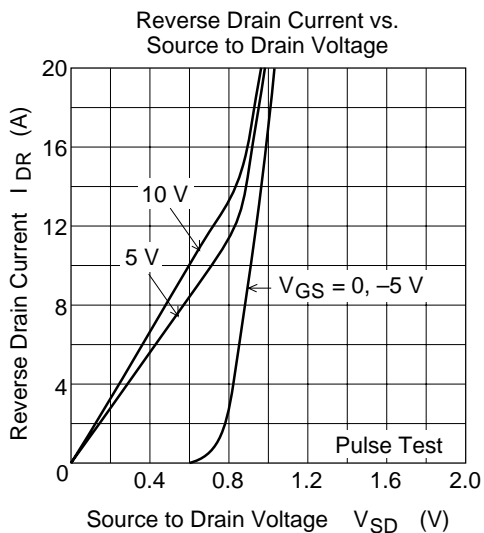
Note: 4. Pulse test

Main Characteristics

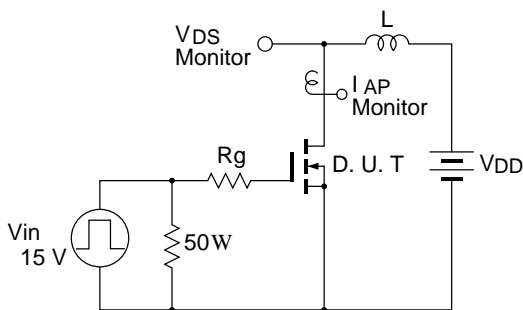






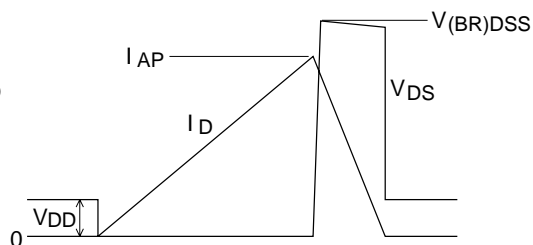


Avalanche Test Circuit

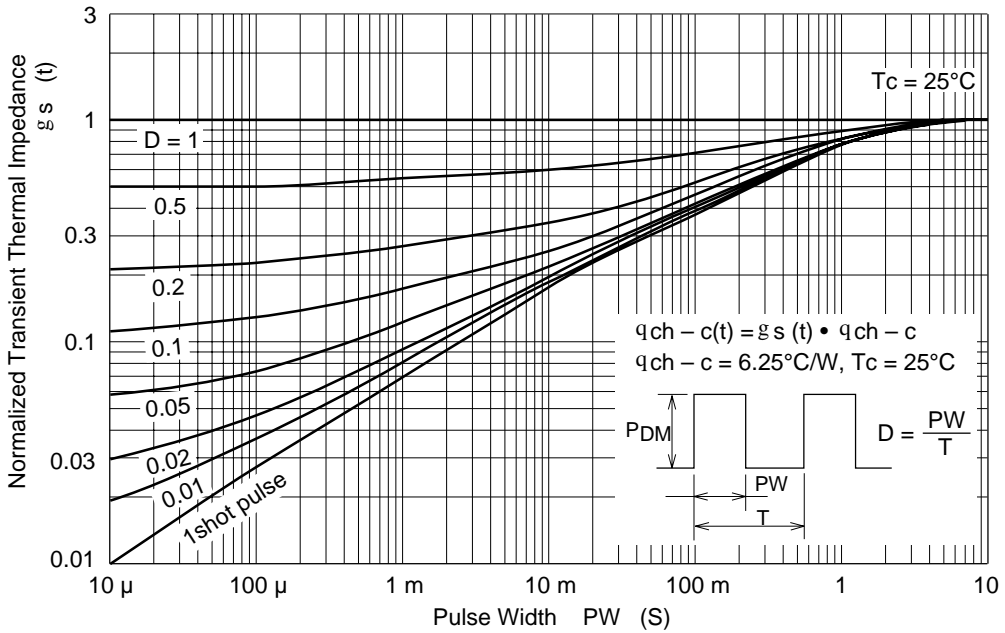


Avalanche Waveform

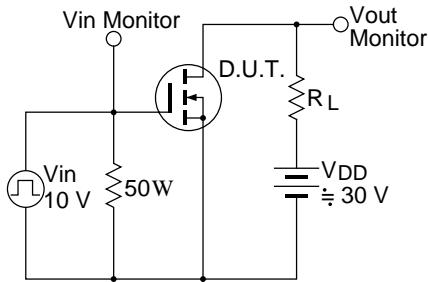
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



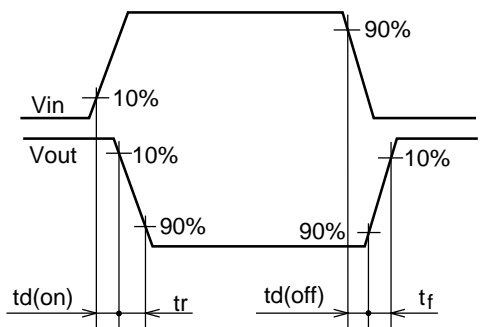
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



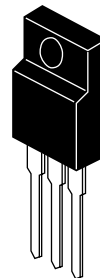
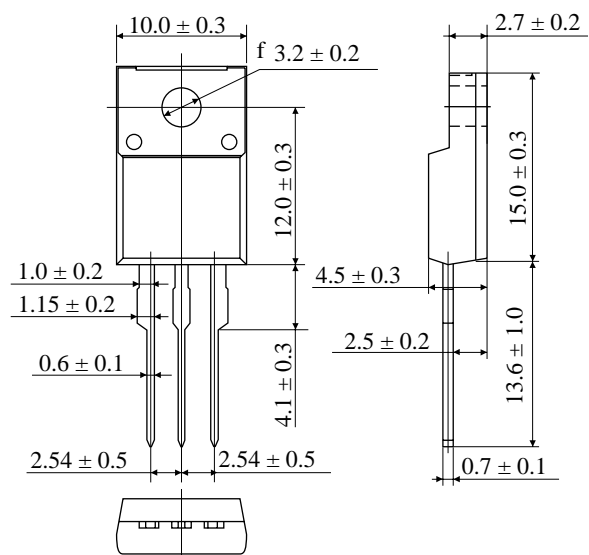
Waveform





## Package Dimensions

Unit: mm



Hitachi Code	TO-220CFM
EIAJ	—
JEDEC	—

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