

SANYO**2SK3255LS**N-Channel MOS Silicon FET
Very High-Speed Switching Applications

TENTATIVE

Features and Applications

- ¥ Low ON-state resistance.
- ¥ Low Qg.

Absolute Maximum Ratings / Ta=25°C

			unit
Drain to Source Voltage	V _{DSS}	900	V
Gate to Source Voltage	V _{GSS}	-30	V
Drain Current(DC)	I _D *	5	A
Drain Current(Pulse)	I _{DP}	15	A
Allowable power Dissipation	PD (TC=25°C)	35	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

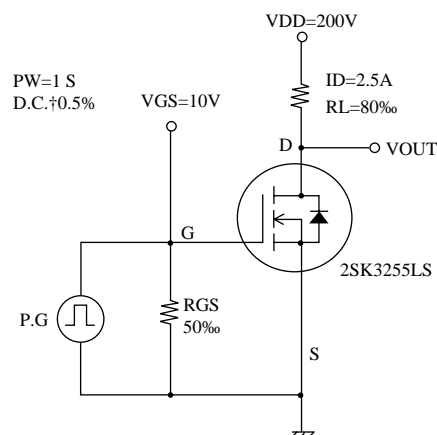
*) : Chip Performance Shown

Electrical Characteristics / Ta=25°C

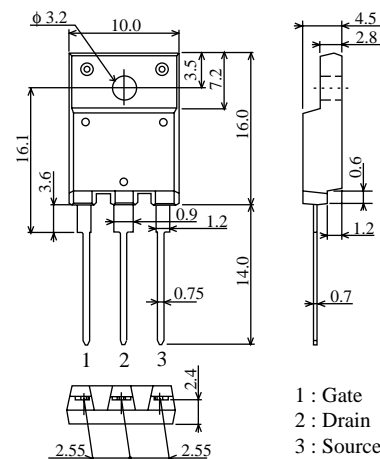
			min	typ	max	unit
Drain to Source Breakdown Voltage	V(BR) _{DSS}	I _D =1mA , V _{GS} =0	900			V
Zero Gate Voltage Drain Current	I _{DSS}	V _D =900V , V _{GS} =0			250	A
Gate to Source Leakage Current	I _{GSS}	V _{GS} =-30V , V _D =0			-100	nA
Cutoff Voltage	V _{GS(off)}	V _D =10V , I _D =1mA	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	V _D =10V , I _D =2.5A	2.4	4.0		S
Static Drain to Source On State Resistance	R _{DS(on)}	I _D =2.5A , V _{GS} =10V		2.1	2.8	Ω
Input Capacitance	C _{iss}	V _D =20V , f=1MHz		1100		pF
Output Capacitance	C _{oss}	V _D =20V , f=1MHz		115		pF
Reverse Transfer Capacitance	C _{rss}	V _D =20V , f=1MHz		28		pF
Total Gate Charge	Q _g	V _D =200V , I _D =2.5A V _{GS} =20V		44		nC
Turn-ON Delay Time	t _{d(on)}	See Specified Test Circuit		21		ns
Rise Time	t _r			43		ns
Turn-OFF Delay Time	t _{d(off)}			160		ns
Fall Time	t _f			47		ns
Diode Forward Voltage	V _{SD}	I _S =2.5A , V _{GS} =0			1.5	V

(Note) Be careful in handling the 2SK3255LS because it has no protection diode between gate and source.

Switching Time Test Circuit



Package Dimensions TO-220FI(LS) (unit:mm)



1 : Gate
2 : Drain
3 : Source

Specifications and information herein are subject to change without notice.

SANYO Electric Co., Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, taito-ku, 110 JAPAN

HD-010711

