

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3638 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

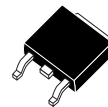
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3638-ZK	TO-252 (MP-3ZK)

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 8.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 32 \text{ A)}$
 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 18 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1100 \text{ pF TYP.}$
- Built-in gate protection diode

(TO-252)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	20	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 64	A
Drain Current (pulse) ^{Note}	$I_{D(pulse)}$	± 220	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	36	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

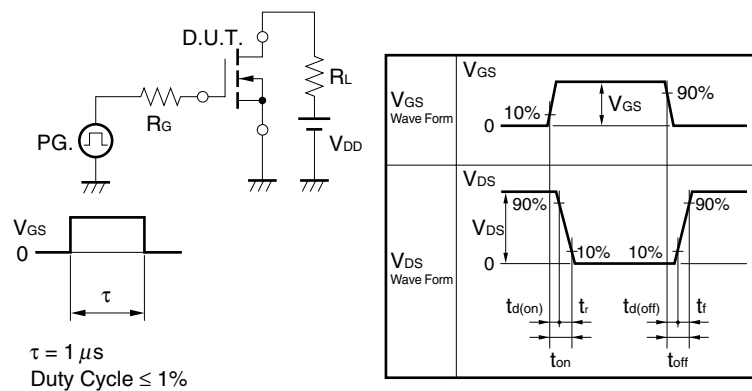
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

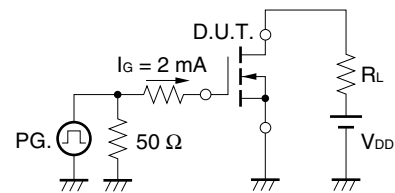
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 32 A	12	25		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 32 A		6.8	8.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 18 A		10	15	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1100		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		450		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		170		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 10 V, I _D = 32 A		10		ns
Rise Time	t _r	V _{GS} = 10 V		4.3		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		35		ns
Fall Time	t _f			9.7		ns
Total Gate Charge	Q _G	V _{DD} = 16 V		22		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		4.3		nC
Gate to Drain Charge	Q _{GD}	I _D = 64 A		5.1		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 64 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 64 A, V _{GS} = 0 V		31		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		23		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT 1 SWITCHING TIME

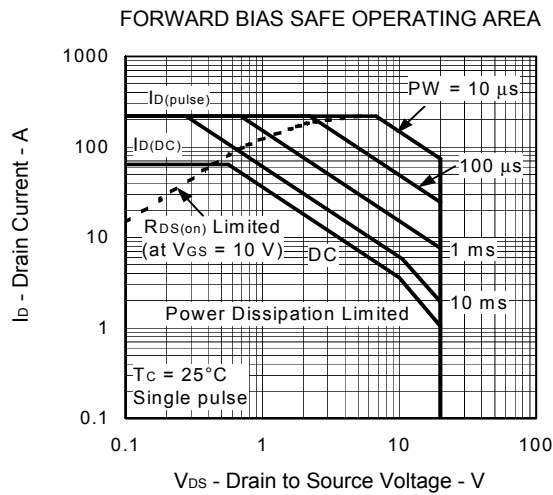
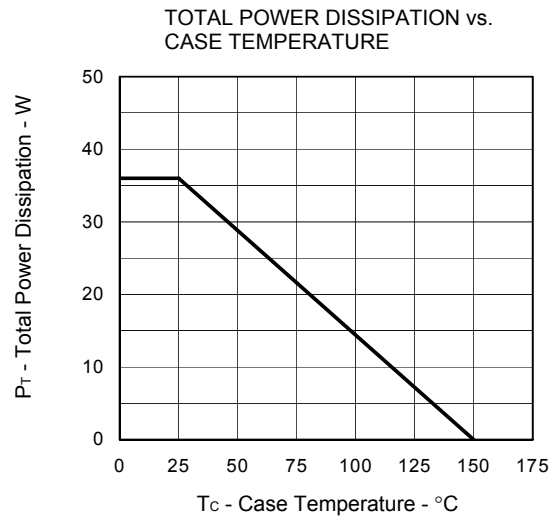
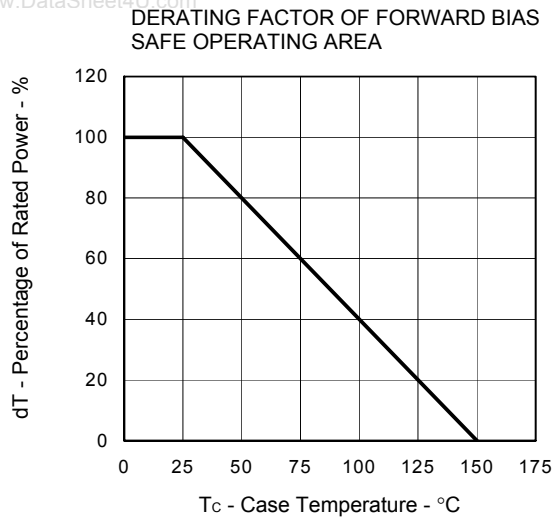


TEST CIRCUIT 2 GATE CHARGE

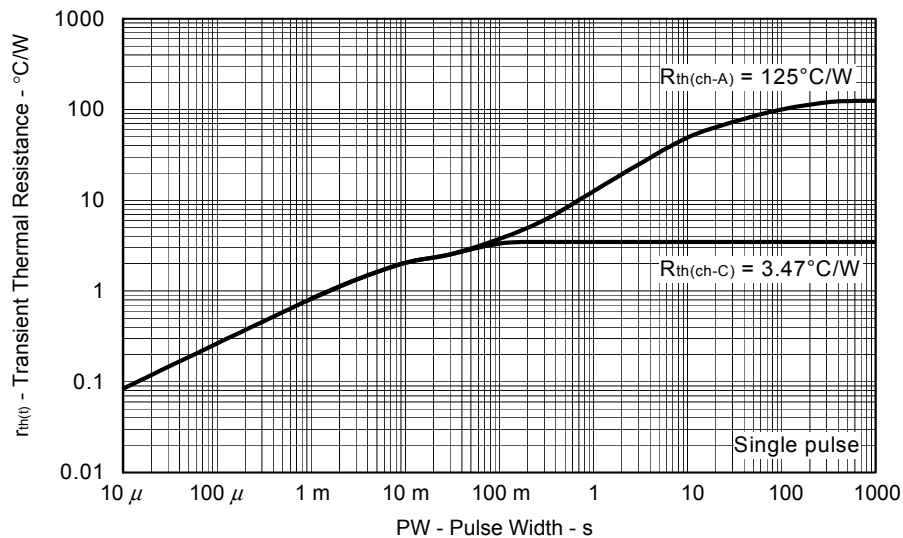


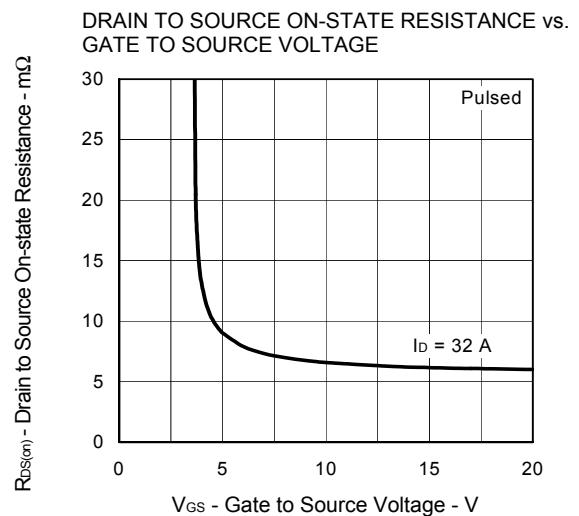
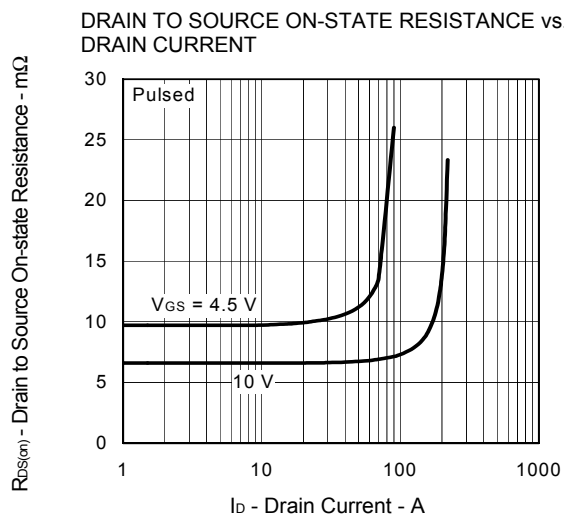
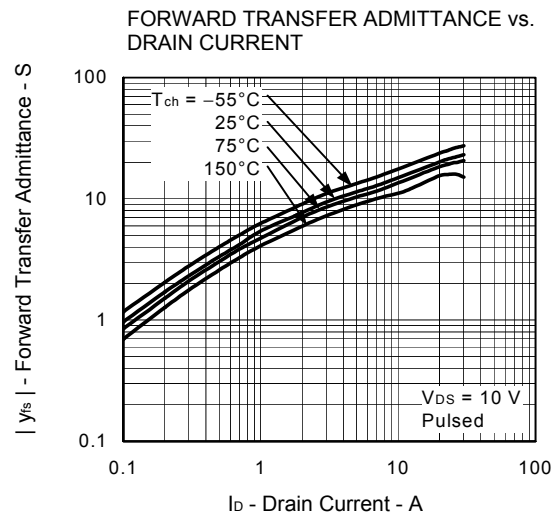
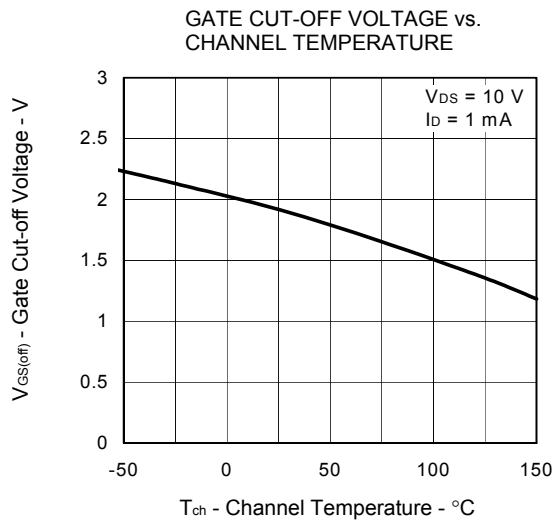
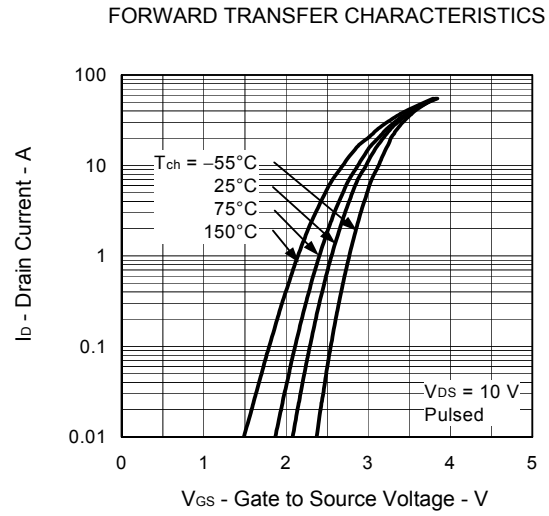
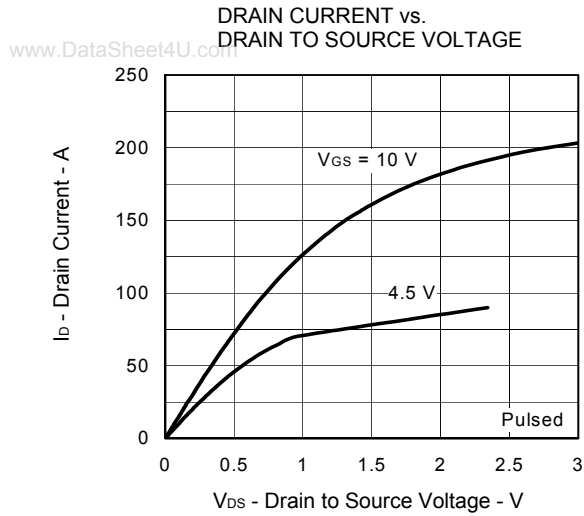
TYPICAL CHARACTERISTICS (T_A = 25°C)

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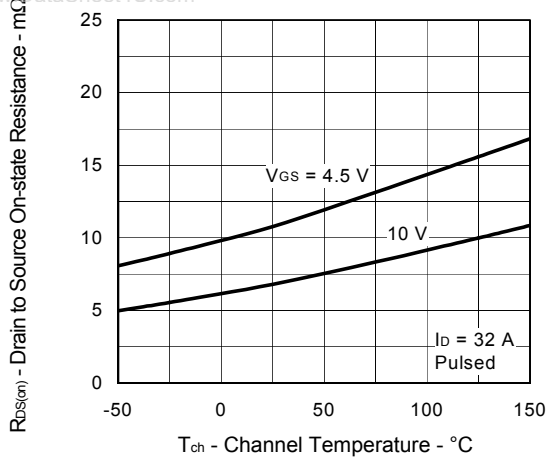


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

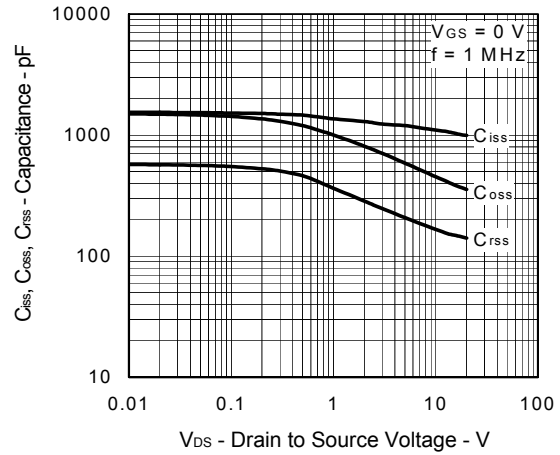




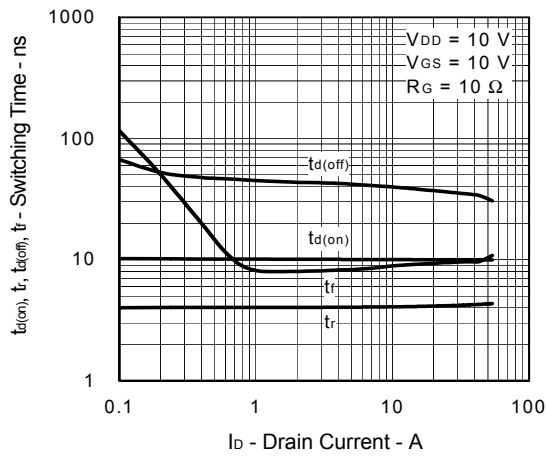
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



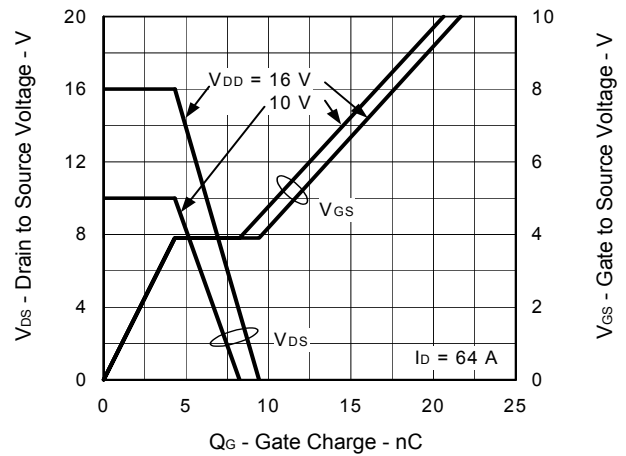
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



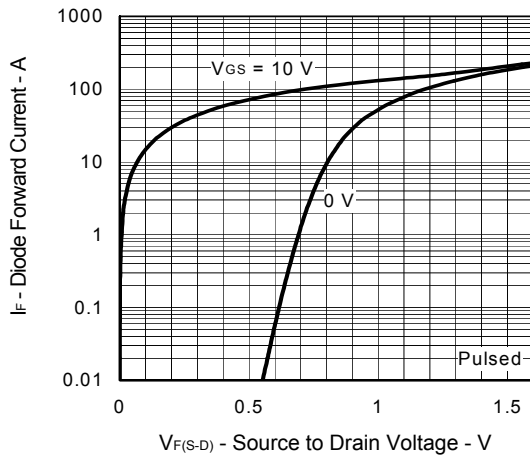
SWITCHING CHARACTERISTICS



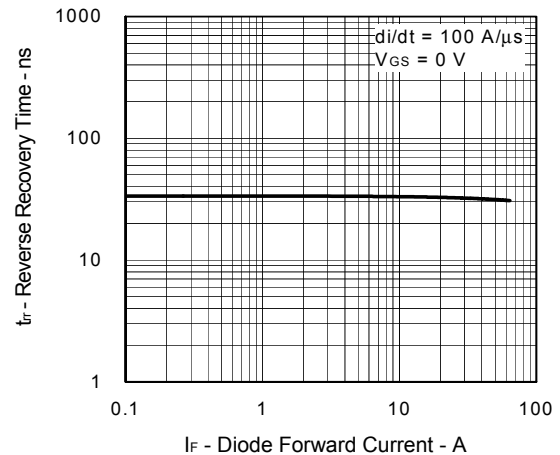
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



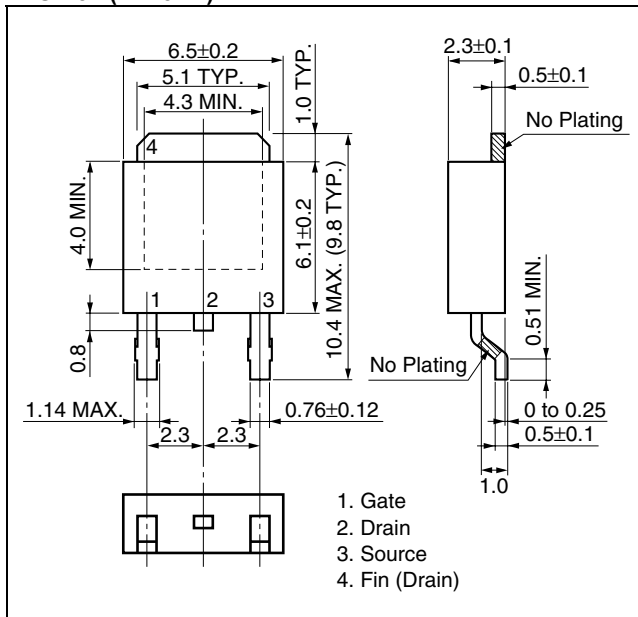
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



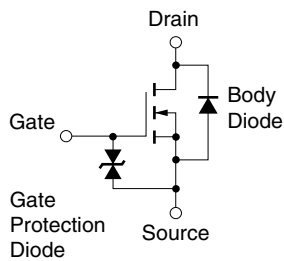
★ PACKAGE DRAWING (Unit: mm)

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TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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