

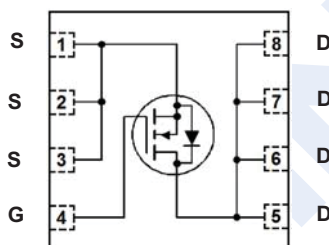
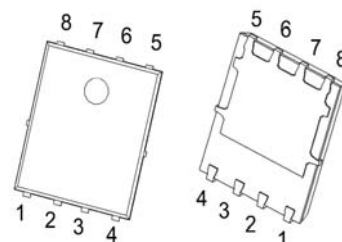
N-Channel MOSFET

2SK4002

■ Features

- $V_{DS} (V) = 150V$
- Max $r_{DS(on)} = 56\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 4.4\text{ A}$
- Max $r_{DS(on)} = 71\text{ m}\Omega$ at $V_{GS} = 6\text{ V}$, $I_D = 3.8\text{ A}$
- Max $r_{DS(on)} = 75\text{ m}\Omega$ at $V_{GS} = 4.5\text{ V}$, $I_D = 3.7\text{ A}$
- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery

DFN5x6-8(PDFNWB5x6-8L)

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current (Note 1)	I_D	4.4	A
Pulsed Drain Current (Note 3)	I_{DM}	30	
Single Pulse Avalanche Energy (Note 2)	EAS	73	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1)	P_D	50	W
		2.5	
Thermal Resistance.Junction- to-Ambient (Note 1)	R_{thJA}	50	$^\circ\text{C/W}$
Thermal Resistance.Junction- to-Case	R_{thJC}	2.5	
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150	

Notes:

1. R_{thJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.
 R_{thJC} is guaranteed by design while R_{thCA} is determined by the user's board design.
2. EAS of 73 mJ is based on Starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 7\text{ A}$, $V_{DD} = 150\text{ V}$, $V_{GS} = 10\text{ V}$.
3. Pulsed I_D limited by junction temperature, $t_d \leq 100\text{ }\mu\text{s}$, please refer to SOA curve for more details.

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■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DS}	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\text{V}$	150			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120\text{V}$, $V_{GS} = 0\text{V}$			1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$			± 100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}$, $I_D = 4.4\text{A}$			56	m Ω
		$V_{GS} = 6\text{V}$, $I_D = 3.8\text{A}$			71	
		$V_{GS} = 4.5\text{V}$, $I_D = 3.7\text{A}$			75	
		$V_{GS} = 10\text{V}$, $I_D = 4.4\text{A}$, $T_J = 125^\circ\text{C}$			110	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{V}$, $I_D = 4.4\text{A}$		21		S
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 75\text{V}$, $f = 1\text{MHz}$		952	1335	pF
Output Capacitance	C_{oss}			74	105	
Reverse Transfer Capacitance	C_{rss}			3	5	
Gate Resistance	R_g		0.1	0.6	1.8	Ω
Turn-On DelayTime	$t_{d(on)}$	$V_{DD} = 75\text{V}$, $I_D = 4.4\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 6\ \Omega$		6.8	14	ns
Turn-On Rise Time	t_r			1.4	10	
Turn-Off DelayTime	$t_{d(off)}$			19	34	
Turn-Off Fall Time	t_f			2.9	10	
Total Gate Charge	Q_g	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 75\text{V}$ $I_D = 4.4\text{A}$	15	21	nC
Total Gate Charge	Q_g	$V_{GS} = 0\text{V}$ to 4.5V		7.6	11	
Gate Source Charge	Q_{gs}			2.1		
Gate Drain Charge	Q_{gd}			2.3		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 4.4\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		53	85	ns
Body Diode Reverse Recovery Charge	Q_{rr}			51	82	nC
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_S = 1.9\text{A}$ (Note 4)			1.2	V
		$V_{GS} = 0\text{V}$, $I_S = 4.4\text{A}$ (Note 4)			1.3	

Notes: 4. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

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■ Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

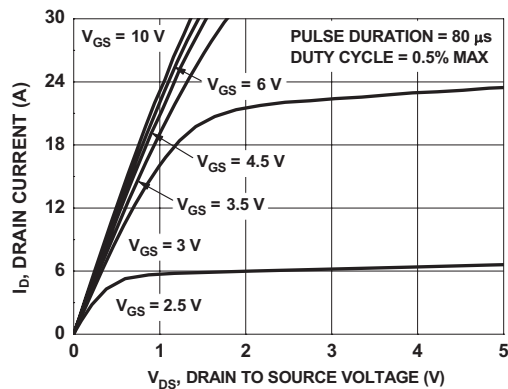


Figure 1. On Region Characteristics

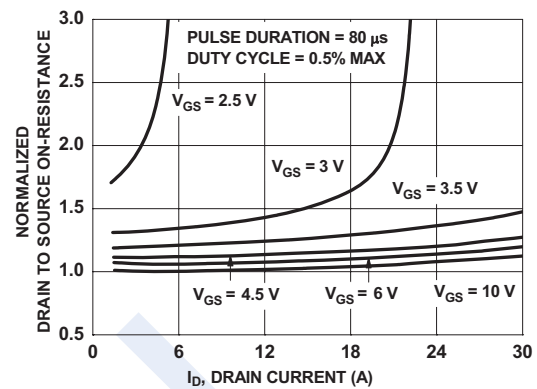


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

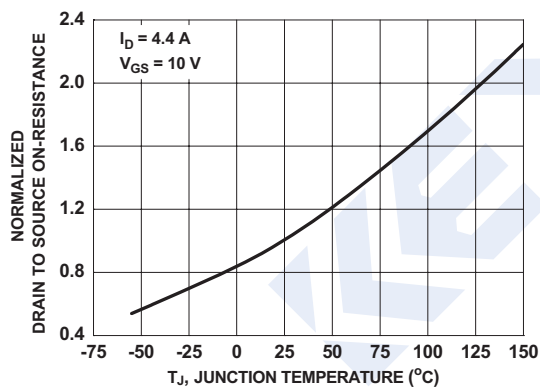


Figure 3. Normalized On Resistance vs Junction Temperature

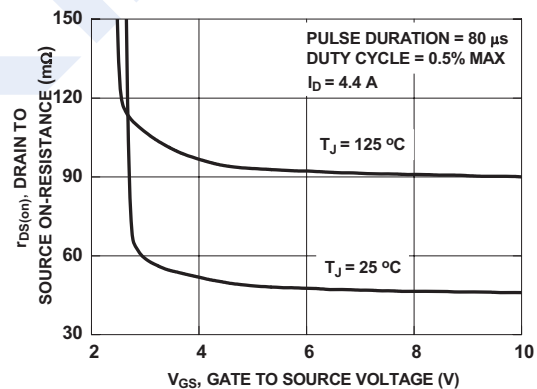


Figure 4. On-Resistance vs Gate to Source Voltage

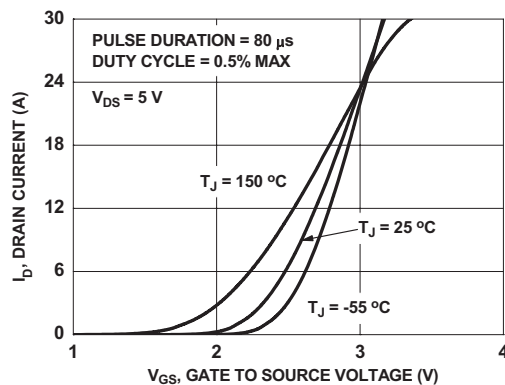


Figure 5. Transfer Characteristics

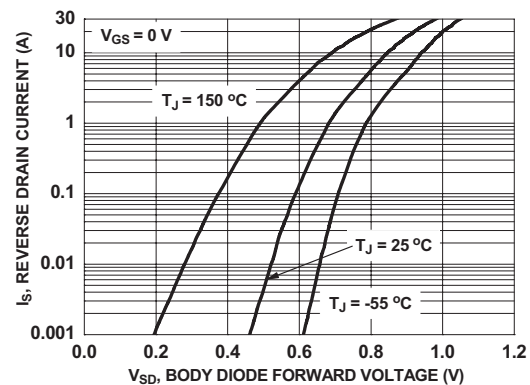


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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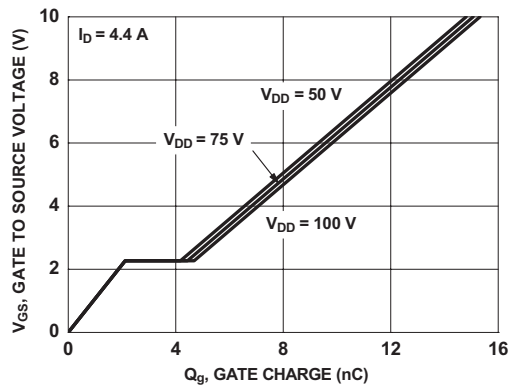


Figure 7. Gate Charge Characteristics

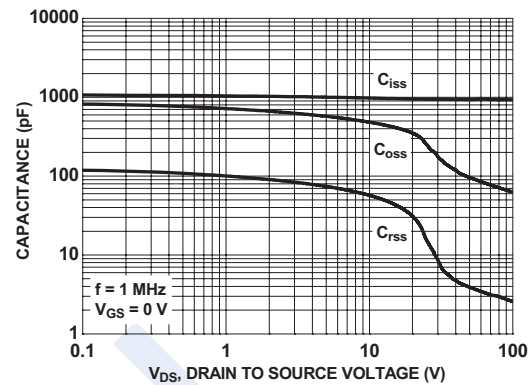


Figure 8. Capacitance vs Drain to Source Voltage

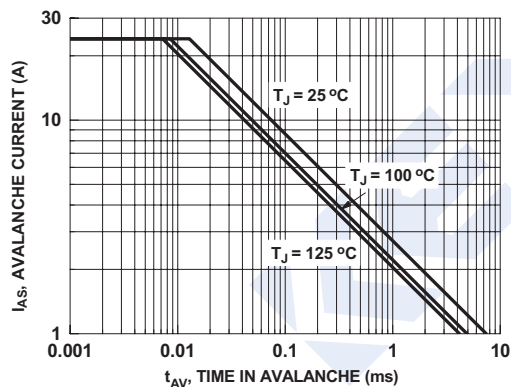


Figure 9. Unclamped Inductive Switching Capability

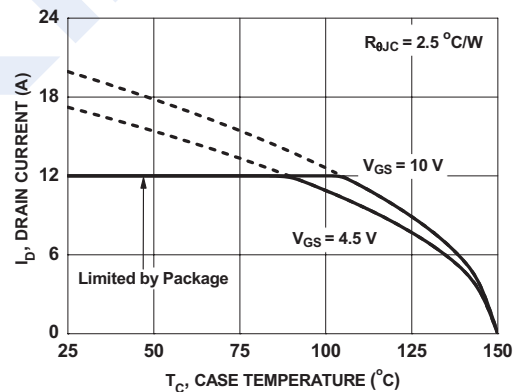


Figure 10. Maximum Continuous Drain Current vs Case Temperature

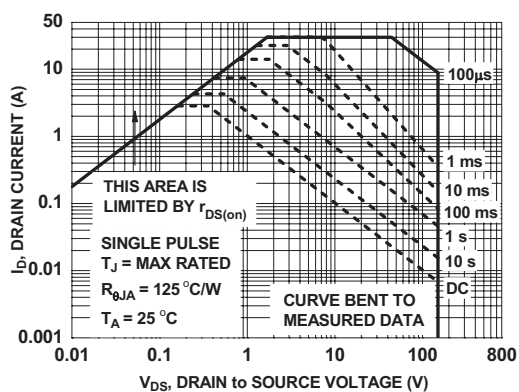


Figure 11. Forward Bias Safe Operating Area

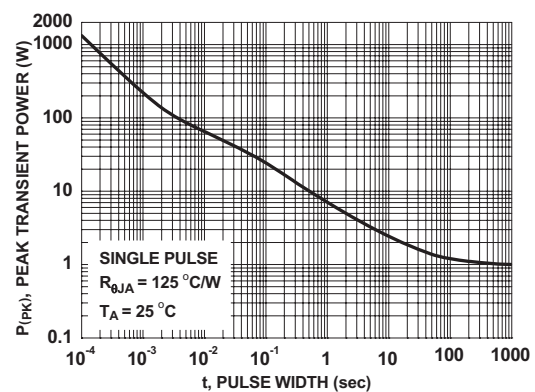


Figure 12. Single Pulse Maximum Power Dissipation

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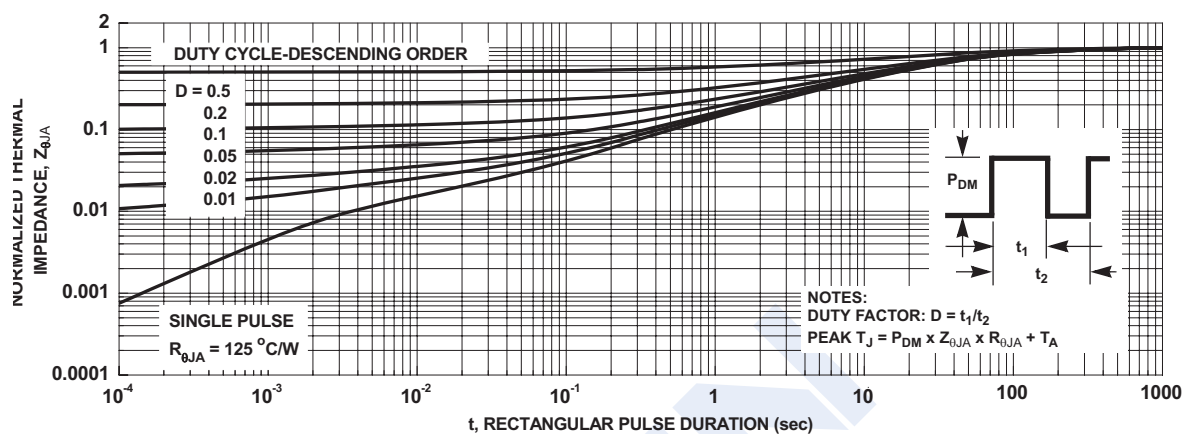
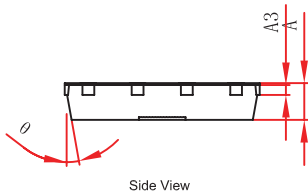
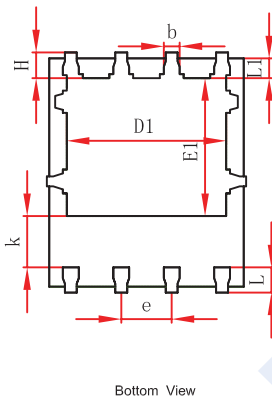
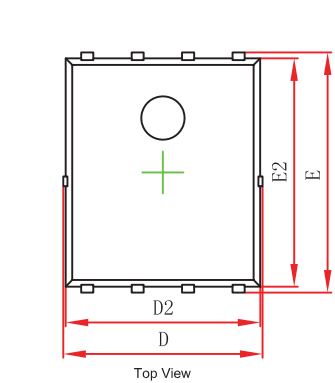


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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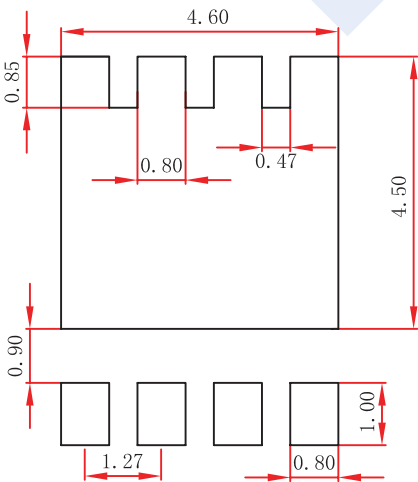
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DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°		12°	

DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.