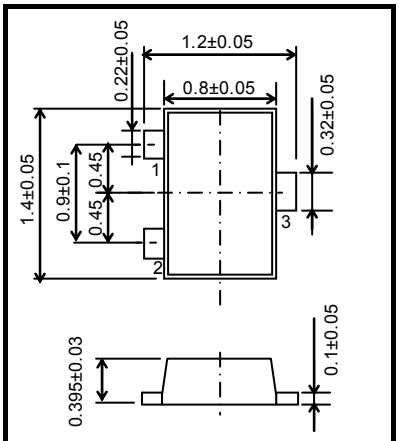
TOSHIBA Field Effect Transistor Silicon N Channel Junction Type

2SK4059TK

For ECM

- Application for compact ECM

Unit: mm



TESM3 1.Drain
2.Source
3.Gate

JEDEC	-
JEITA	-
TOSHIBA	2-1R1A

Weight: 2.2mg (typ.)

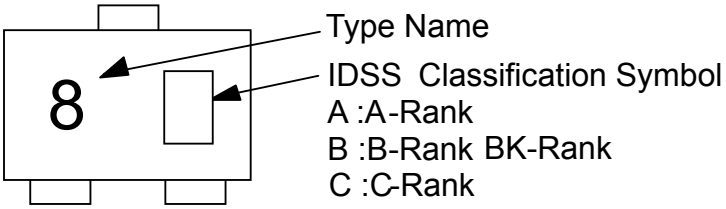
Absolute Maximum Ratings (Ta=25°C)

Characteristic	Symbol	Rating	Unit
Gate-Drain voltage	V_{GDO}	-20	V
Gate Current	I_G	10	mA
Drain power dissipation (Ta = 25°C)	P_D	100	mW
Junction Temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55~125	°C

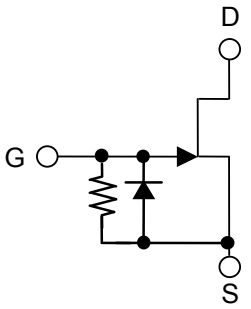
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

IDSS CLASSIFICATION
A-Rank 140~240μA
B-Rank 210~350μA
BK-Rank 210~400μA
C-Rank 320~500μA

Marking



Equivalent Circuit

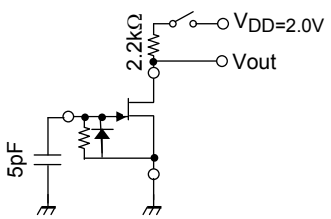


Electrical Characteristics (Ta=25°C)

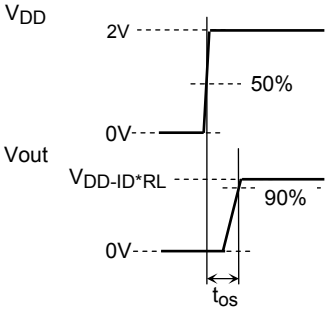
Characteristic	Symbol	Test Condition		Min	Typ.	Max	Unit
Drain Current	I_{DSS}	V_{DS} = 2 V, V_{GS} = 0	A	140	—	240	μA
			B	210	—	350	
			BK	210	—	400	
			C	320	—	500	
Drain Current	I_D	V_{DD} = 2 V, RL= 2.2kΩ,Cg = 5pF	A	125	—	260	μA
			B	190	—	370	
			BK	190	—	420	
			C	290	—	500	
Gate-Source Cut-off Voltage	$V_{GS(OFF)}$	V_{DS} = 2 V, I_D = 1μA		-0.1	—	-1.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 2 V,V_{GS} = 0V		1.35	1.85	—	mS
Gate-Drain Voltage	$V_{(BR)GDO}$	IG=-10μA		-20	—	—	V
Input capacitance	C_{iss}	V_{DS} = 2 V, V_{GS} = 0, f = 1 MHz		—	4.0	—	pF
Voltage Gain	Gv	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF, f = 1kHz,vin=100mV	A	-1.2	+0.9	—	dB
			B	-0.2	+1.4	—	
			BK	-0.2	+1.7	—	
			C	+0.5	+1.8	—	
Delta Voltage Gain	DGv(f)	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF,f = 1kHz~100Hz,vin=100mV		—	0	-1	dB
Delta Voltage Gain	DGv(V)	V_{DD} = 2V~1.5V, RL= 2.2kΩ,Cg = 5pF,f = 1kHz, vin=100mV	A	—	-0.6	-1.1	dB
			B	—	-0.8	-1.7	
			BK	—	-1.1	-2.0	
			C	—	-1.4	-3.2	
Noise Voltage	VN	V_{DD} = 2V, RL= 1kΩ,Cg = 10pF,Gv=80dB, A-Curve Filter	A	—	33	75	mV
			B	—	38	80	
			BK	—	40	85	
			C	—	42	90	
Total Harmonic Distortion	THD	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF, f = 1kHz, vin=50mV	A	—	1.3	—	%
			B	—	0.6	—	
			BK	—	0.5	—	
			C	—	0.1	—	
Time Output Stability	tos	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF		—	100	200	ms

Time Output Stability Test Method

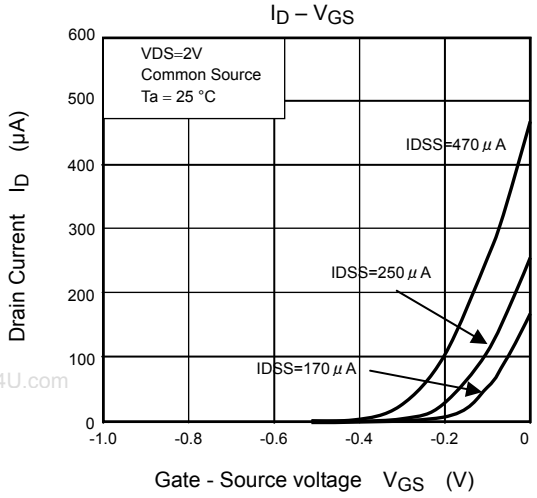
a) TEST CIRCUIT



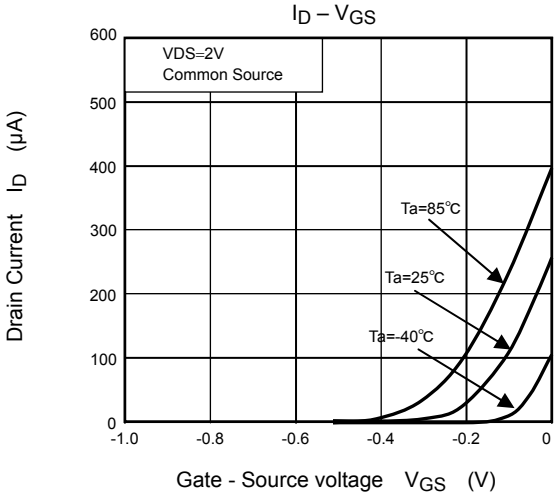
b) TEST SIGNAL



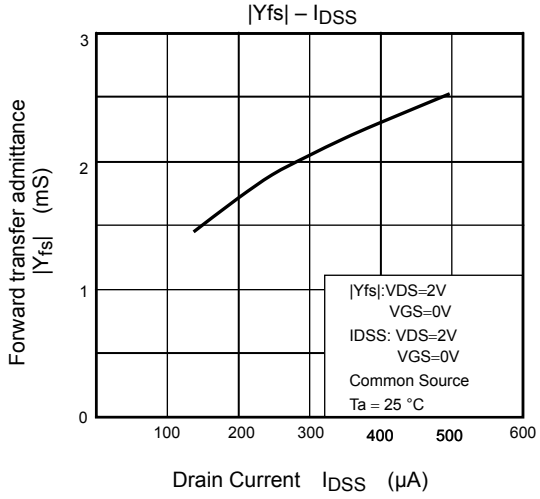
$I_D - V_{GS}$



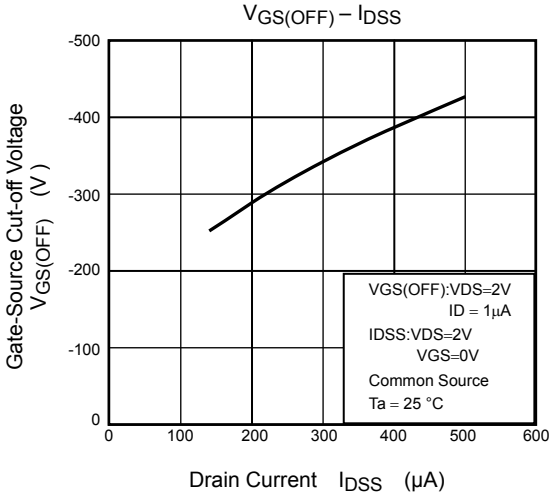
$I_D - V_{GS}$



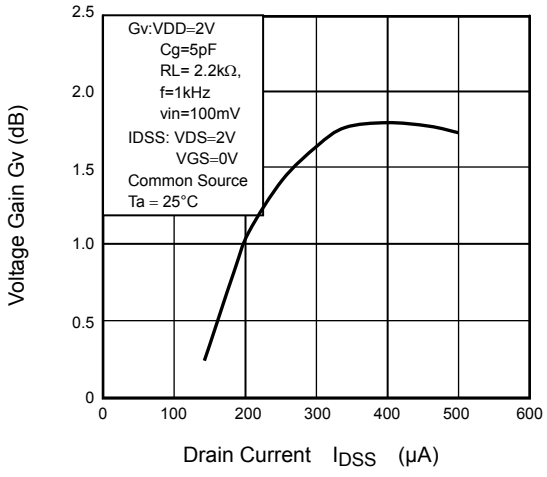
$|Yfs| - I_{DSS}$



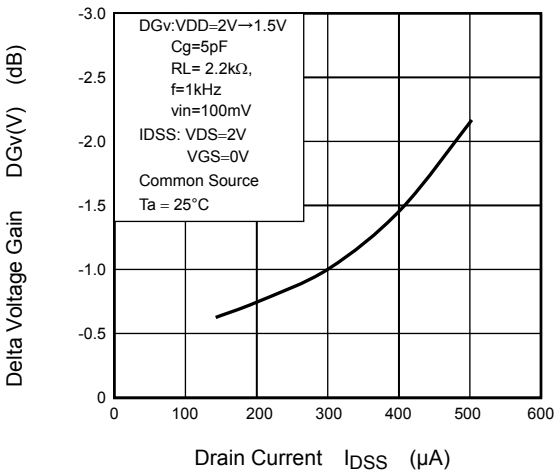
$V_{GS(OFF)} - I_{DSS}$



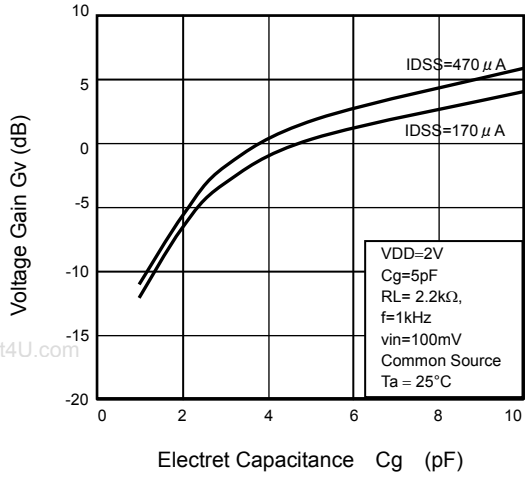
$Gv - I_{DSS}$



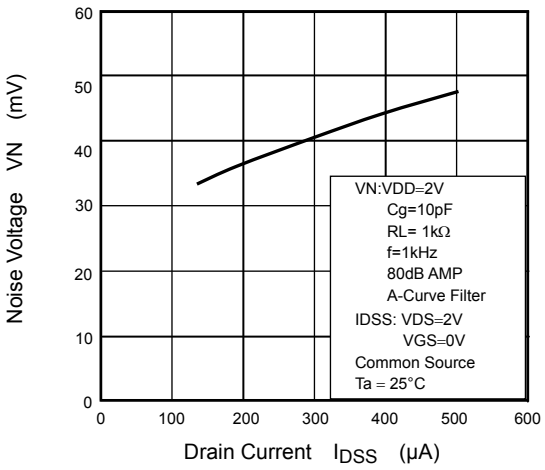
$DGv(V) - I_{DSS}$



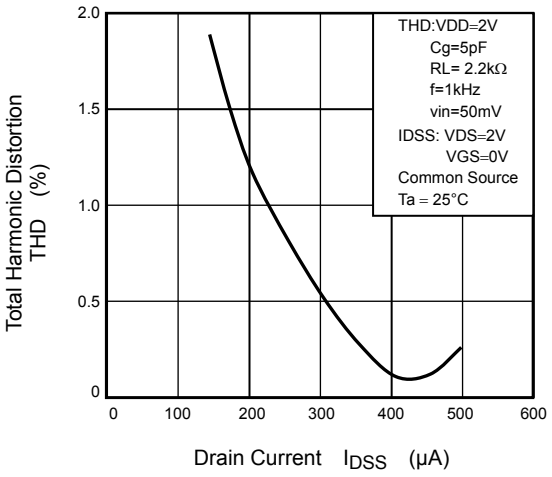
Gv – Cg



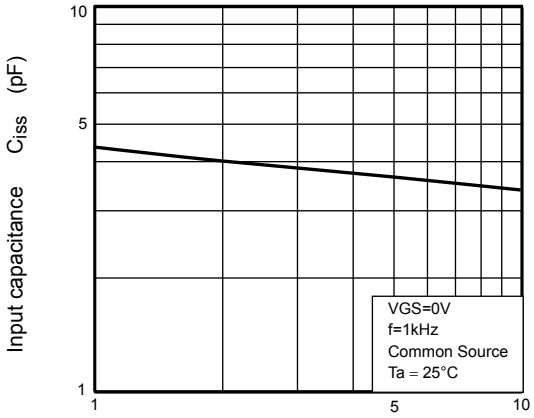
VN – I_{DSS}



THD– I_{DSS}



C_{iss} – V_{DS}



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20070701-EN GENERAL

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