

# MOS FIELD EFFECT TRANSISTOR

# 2SK4144

## SWITCHING

### N-CHANNEL POWER MOS FET

#### DESCRIPTION

The 2SK4144 is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4144-AZ <sup>Note</sup>	Sn-Ag-Cu	Vinyl bag 200 p/bag	Isolated TO-220 typ. 2.2 g
2SK4144-S12-AZ <sup>Note</sup>		Tube 50 p/tube	

**Note** Pb-free (This product does not contain Pb in the external electrode.)

#### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 5.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 35 \text{ A)}$   
 $R_{DS(on)2} = 7.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 35 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 5500 \text{ pF TYP. (} V_{DS} = 10 \text{ V)}$
- Built-in gate protection diode

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±70	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±280	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	35	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Repetitive Avalanche Current <sup>Note2</sup>	I <sub>AR</sub>	49.5	A
Repetitive Avalanche Energy <sup>Note2</sup>	E <sub>AR</sub>	245	mJ

(Isolated TO-220)



**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** T<sub>ch</sub> ≤ 150°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V, L = 100 μH

#### THERMAL RESISTANCE

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	3.57	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	62.5	°C/W

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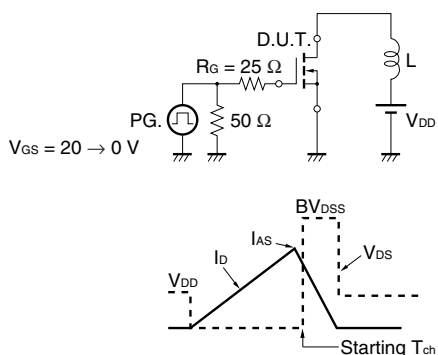
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<R> ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

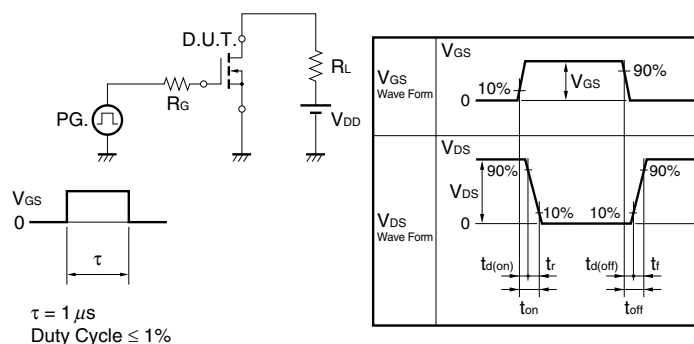
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 35 A	28	56		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 35 A		4.7	5.8	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 35 A		5.3	7.3	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V,		5500		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		1050		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		350		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 35 A,		20		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		12.2		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		100		ns
Fall Time	t <sub>f</sub>			9.5		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 48 V,		96		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V,		18		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 70 A		23.5		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 70 A, V <sub>GS</sub> = 0 V		0.9	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 70 A, V <sub>GS</sub> = 0 V,		48		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		69		nC

Note Pulsed

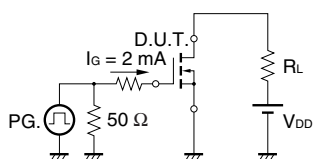
TEST CIRCUIT 1 AVALANCHE CAPABILITY



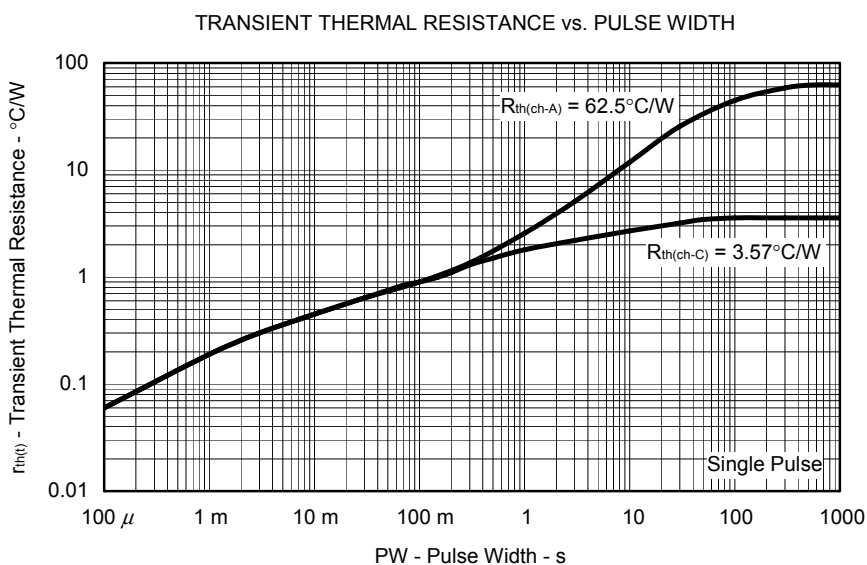
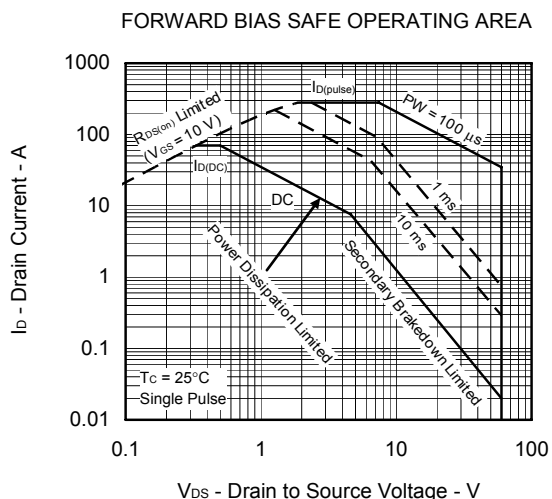
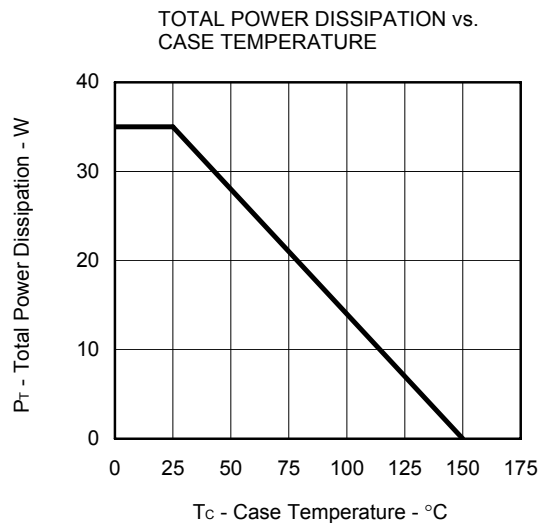
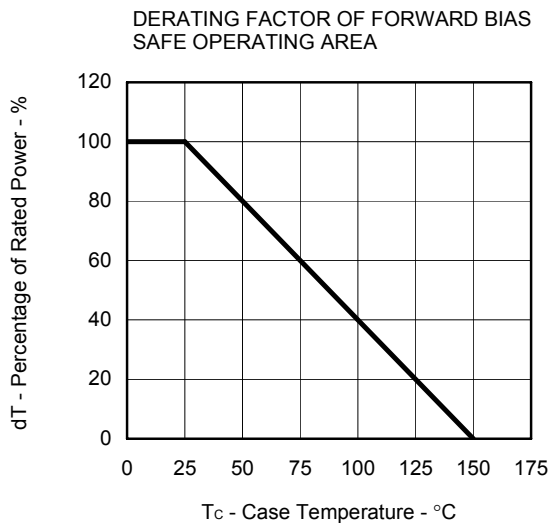
TEST CIRCUIT 2 SWITCHING TIME



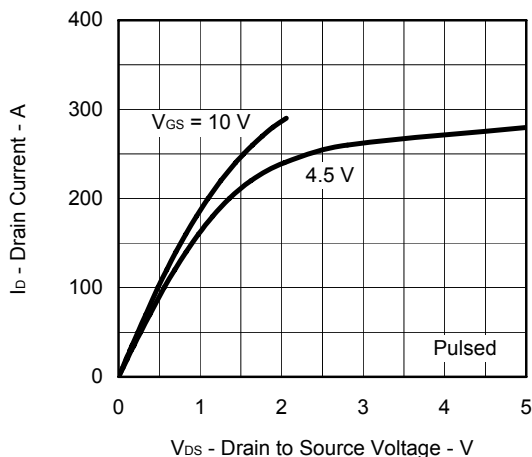
TEST CIRCUIT 3 GATE CHARGE



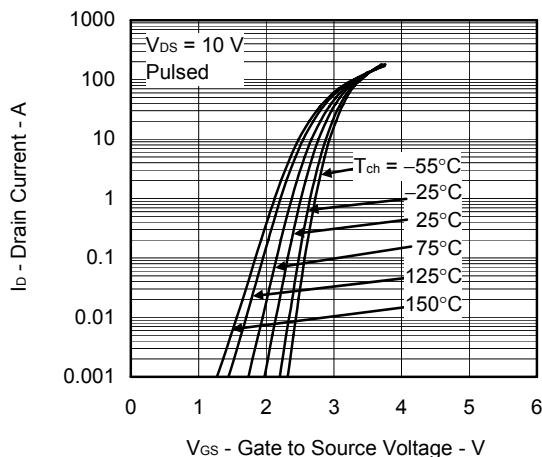
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



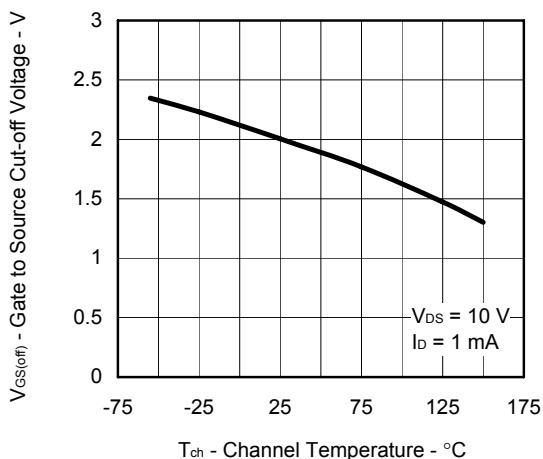
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



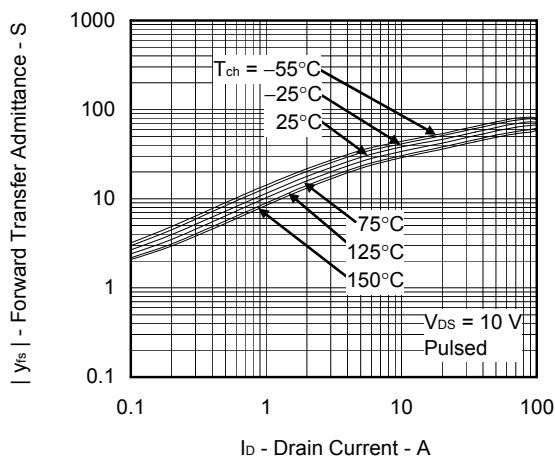
FORWARD TRANSFER CHARACTERISTICS



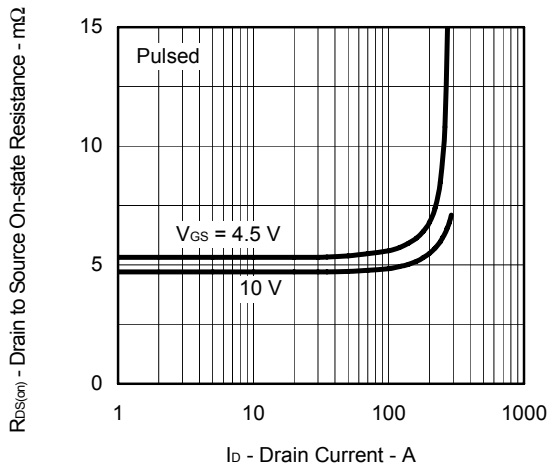
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



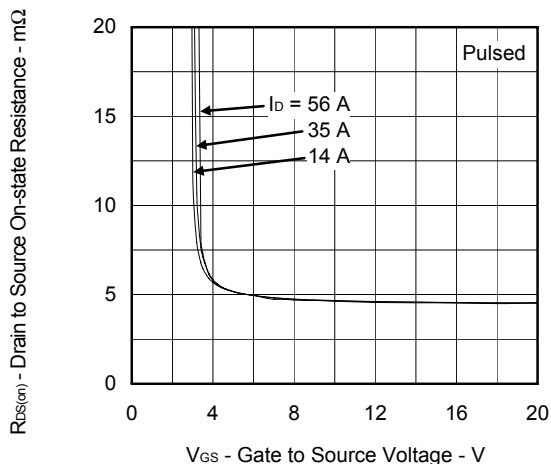
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



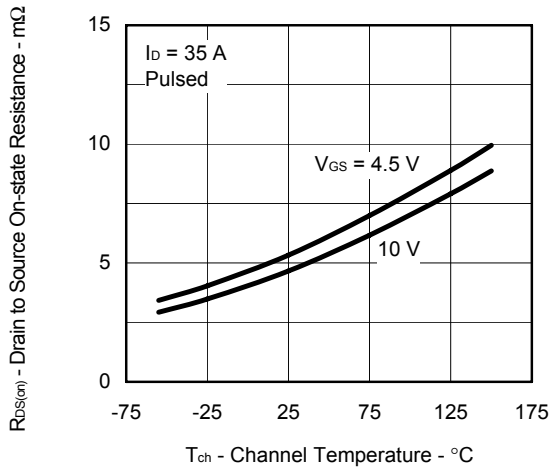
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



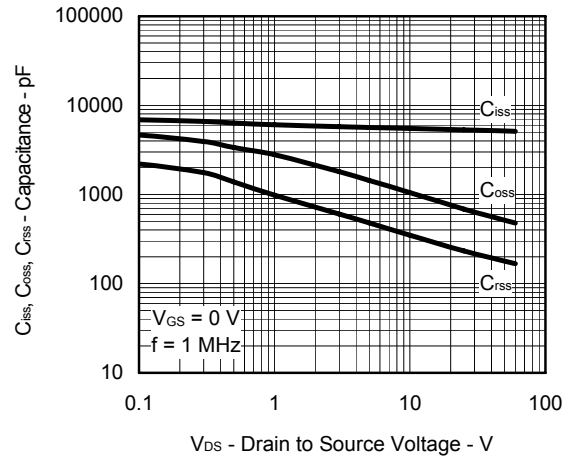
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



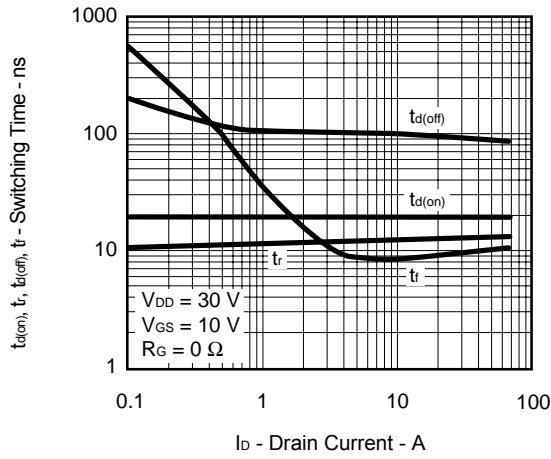
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



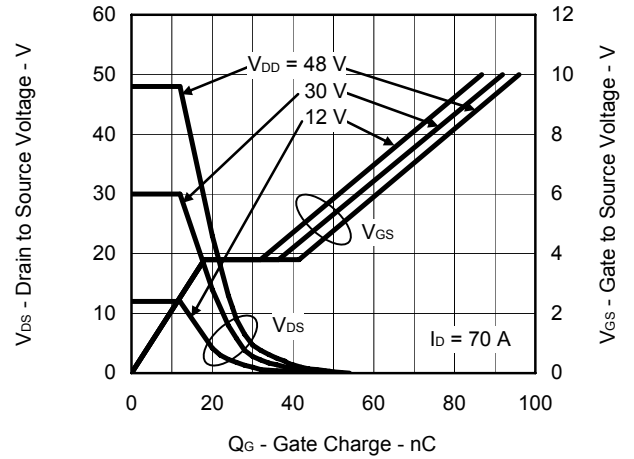
<R> CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



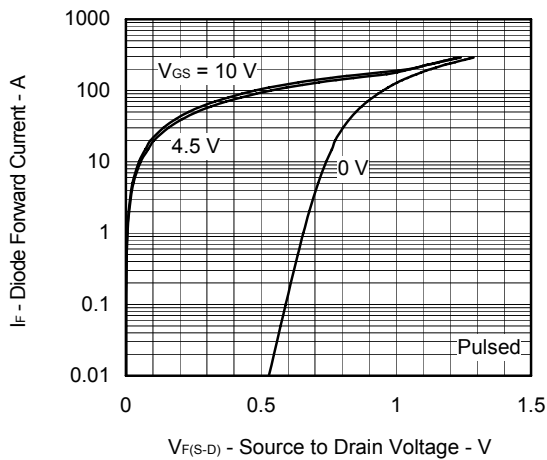
<R> SWITCHING CHARACTERISTICS



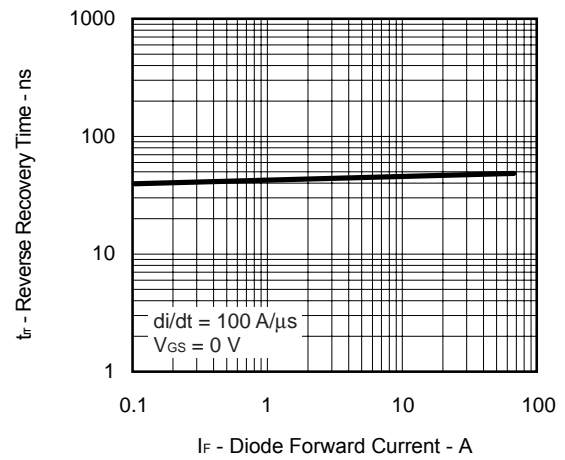
<R> DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

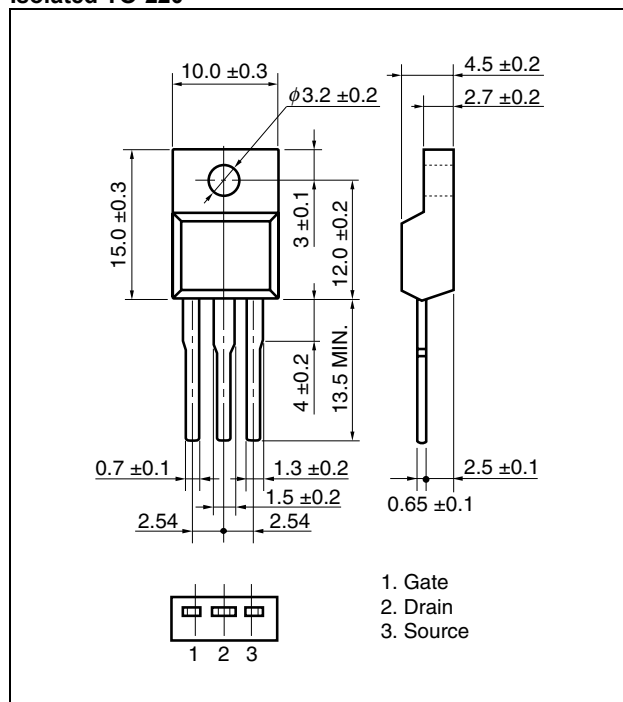


<R> REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

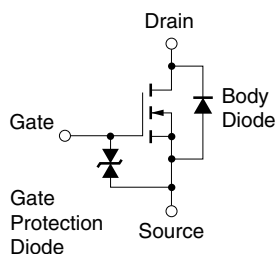


PACKAGE DRAWING (Unit: mm)

Isolated TO-220

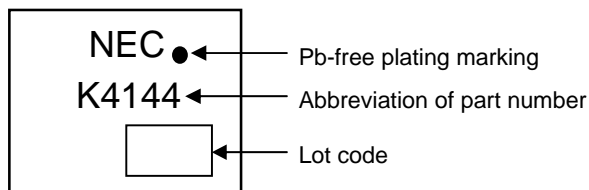


EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**MARKING INFORMATION**



**RECOMMENDED SOLDERING CONDITIONS**

The 2SK4144 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating	Maximum temperature (Pin temperature): 300°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P300

**Caution Do not use different soldering methods together (except for partial heating).**

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