DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

2SK4178

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4178 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 9.0 mΩ MAX. (V_{GS} = 10 V, I_D = 30 A)
- Low gate to drain charge
  Q_{GD} = 3.7 nC TYP. (V_{DD} = 15 V, I_D = 30 A)
- 4.5 V drive available

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4178(1)-S27-AY Note	Pure Sn (Tin)	Tube 75 p/tube	TO-251 (MP-3-b) typ. 0.34 g
2SK4178-ZK-E1-AY Note		Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g
2SK4178-ZK-E2-AY Note			

Note Pb-free (This product does not contain Pb in external electrode).

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±48	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±144	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	33	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	23	A
Single Avalanche Energy Note2	E_{AS}	52.9	mJ

(TO-251)

(TO-252)

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 0.1 mH

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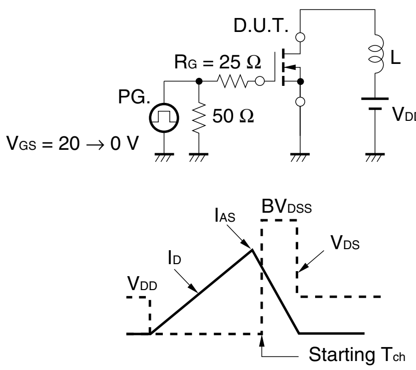
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

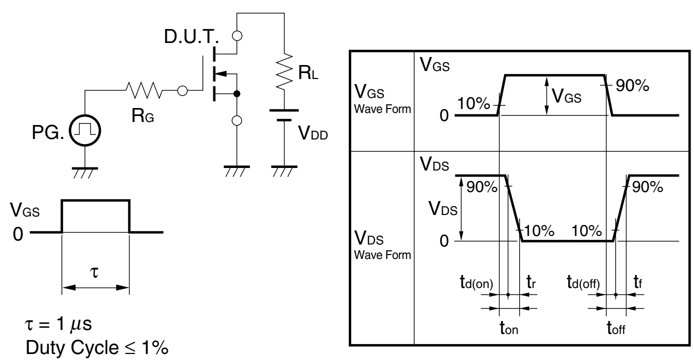
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 12 A	7	15		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 30 A		6.8	9.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 12 A		9.8	15	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		1500		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		360		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		126		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 30 A,		9		ns
Rise Time	t_r	V_{GS} = 10 V,		9.7		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 3 Ω		32		ns
Fall Time	t_f			7.7		ns
Total Gate Charge	Q_{G1}	V_{DD} = 15 V, V_{GS} = 10 V, I_D = 30 A		24		nC
	Q_{G2}	V_{DD} = 15 V, V_{GS} = 4.5 V, I_D = 30 A		11.5		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 15 V, I_D = 30 A		3.7		nC
Gate to Drain Charge	Q_{GD}			3.7		nC
Gate Resistance	R_G			1.2		Ω
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		0.87	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V,		29		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		23		nC

Note Pulsed

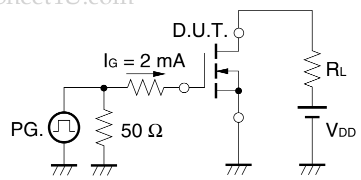
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

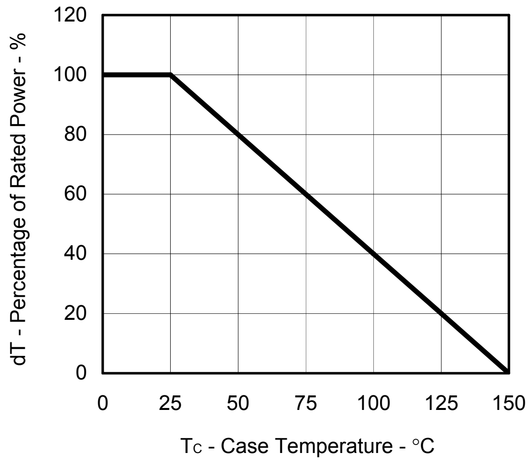


TEST CIRCUIT 3 GATE CHARGE

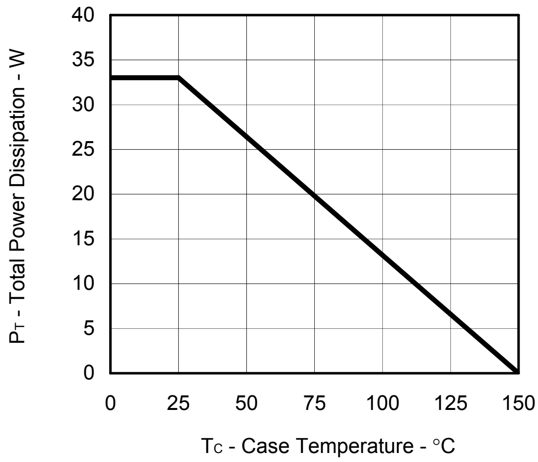


TYPICAL CHARACTERISTICS (T_A = 25°C)

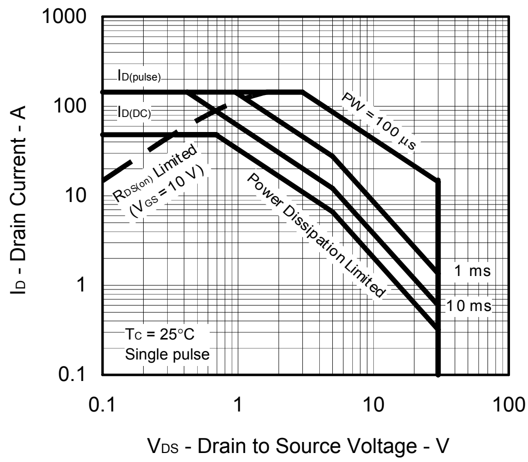
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



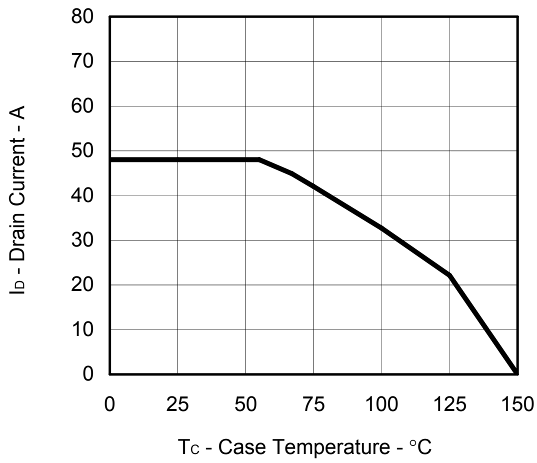
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



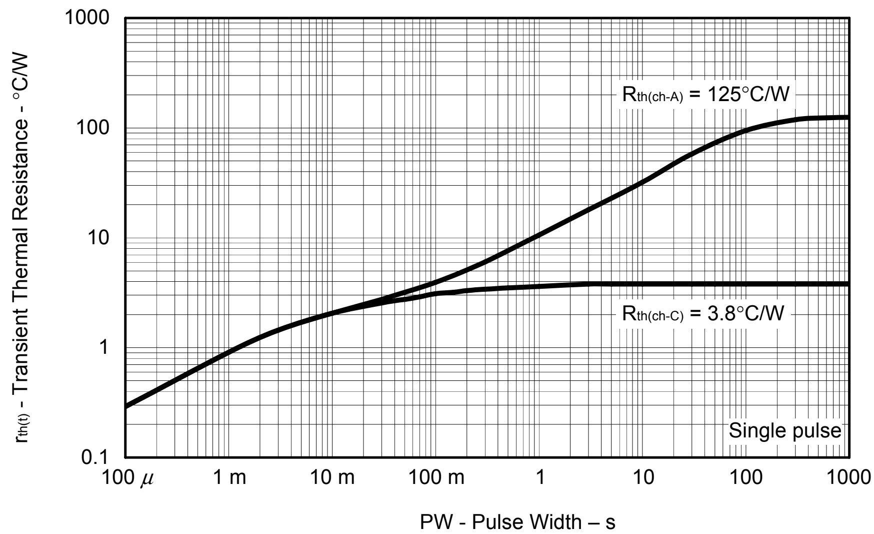
FORWARD BIAS SAFE OPERATING AREA

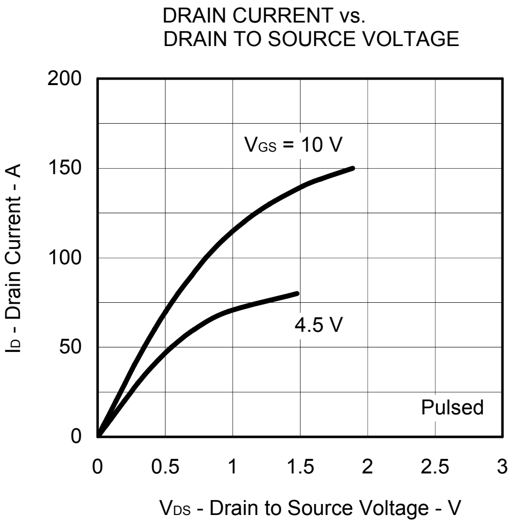


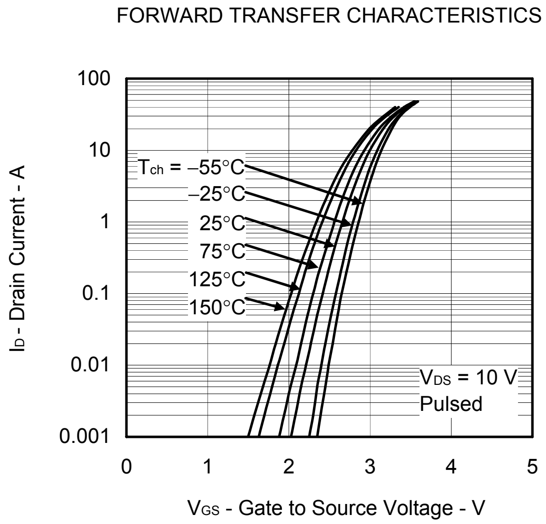
DRAIN CURRENT vs. CASE TEMPERATURE

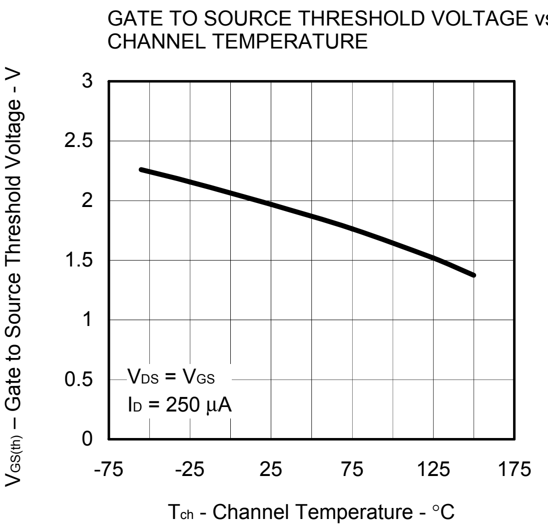


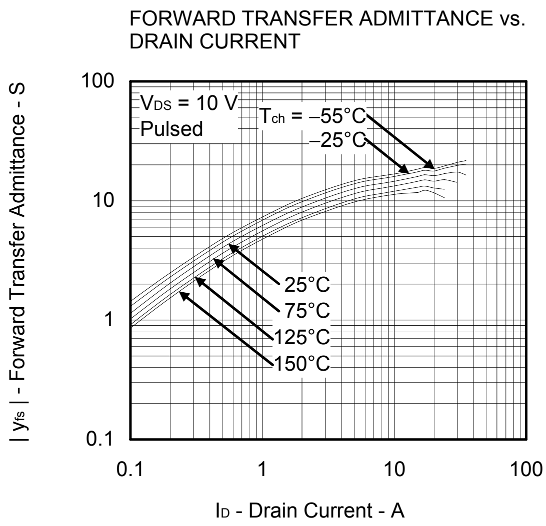
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

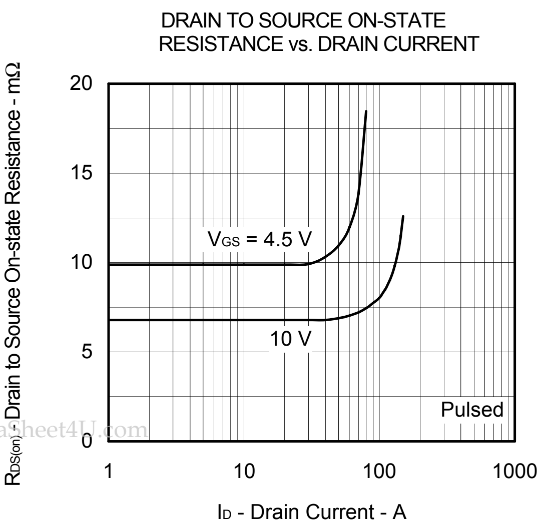


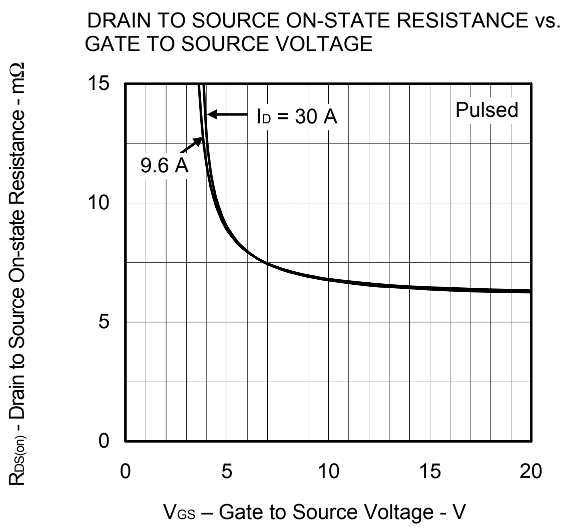

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE
ID - Drain Current - A
VDS - Drain to Source Voltage - V
VGS = 10 V
4.5 V
Pulsed
200
150
100
50
0
0.5
1
1.5
2
2.5
3


FORWARD TRANSFER CHARACTERISTICS
ID - Drain Current - A
VGS - Gate to Source Voltage - V
Tch = –55°C
–25°C
25°C
75°C
125°C
150°C
VDS = 10 V
Pulsed
100
10
1
0.1
0.01
0.001
0
1
2
3
4
5

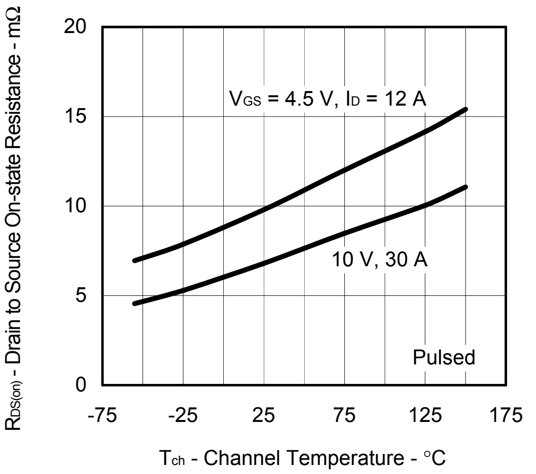

GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE
VGS(th) – Gate to Source Threshold Voltage - V
Tch - Channel Temperature - °C
VDS = VGS
ID = 250 μA
3
2.5
2
1.5
1
0.5
0
-75
-25
25
75
125
175


FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT
| yfs | - Forward Transfer Admittance - S
ID - Drain Current - A
VDS = 10 V
Pulsed
Tch = –55°C
–25°C
25°C
75°C
125°C
150°C
100
10
1
0.1
0.1
1
10
100

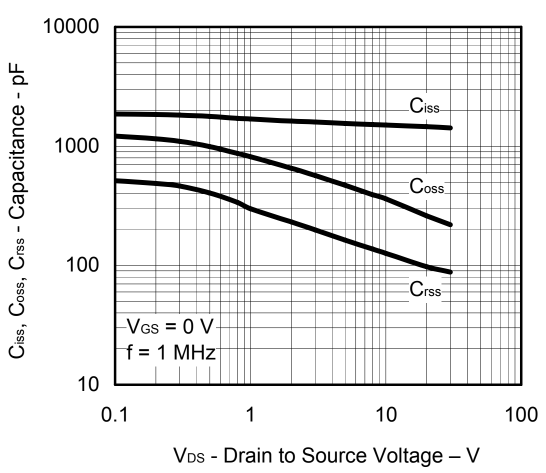

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT
RDS(on) - Drain to Source On-state Resistance - mΩ
ID - Drain Current - A
VGS = 4.5 V
10 V
Pulsed
20
15
10
5
0
1
10
100
1000


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE
RDS(on) - Drain to Source On-state Resistance - mΩ
VGS – Gate to Source Voltage - V
ID = 30 A
9.6 A
Pulsed
15
10
5
0
0
5
10
15
20

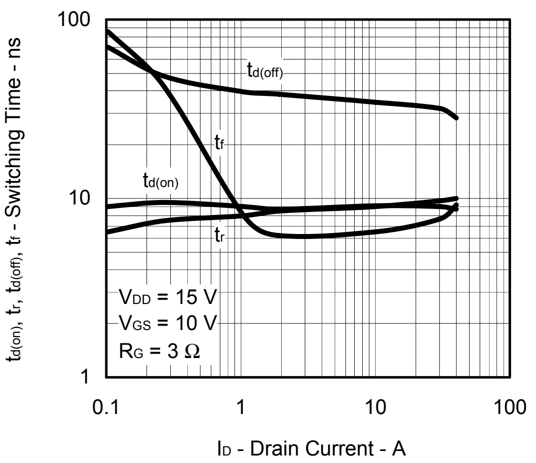
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



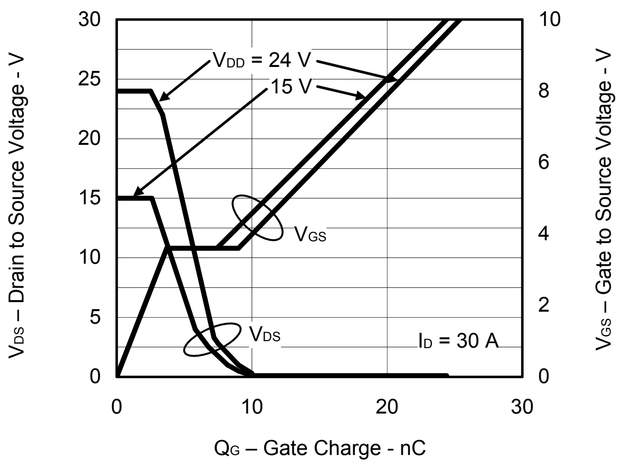
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



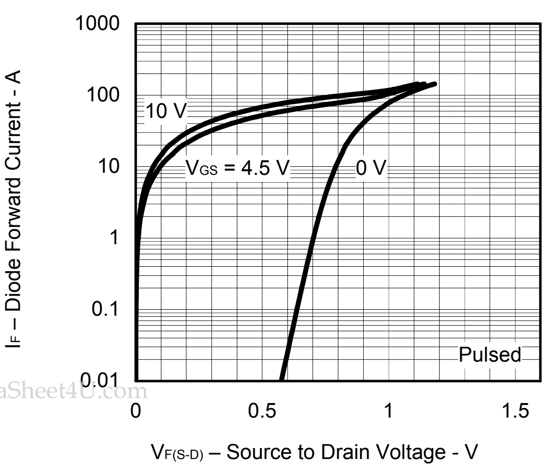
SWITCHING CHARACTERISTICS



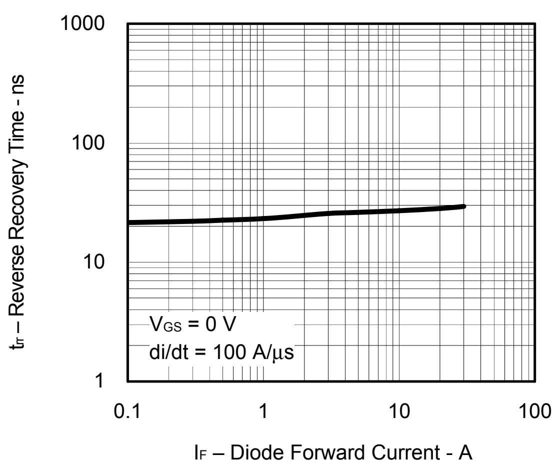
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



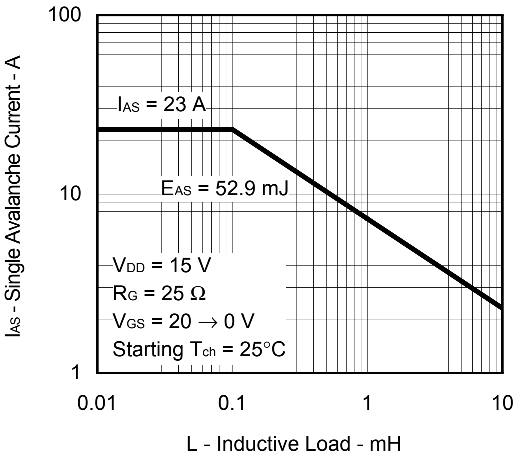
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



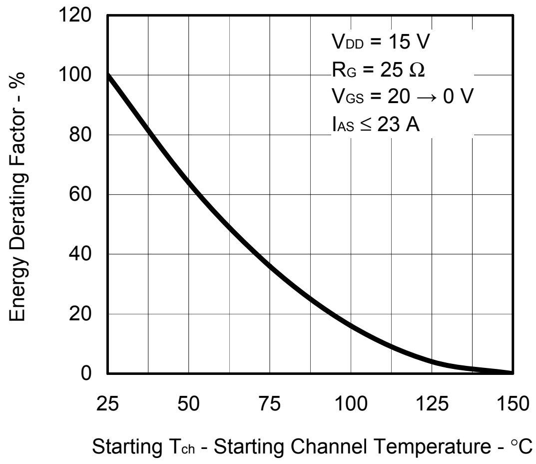
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

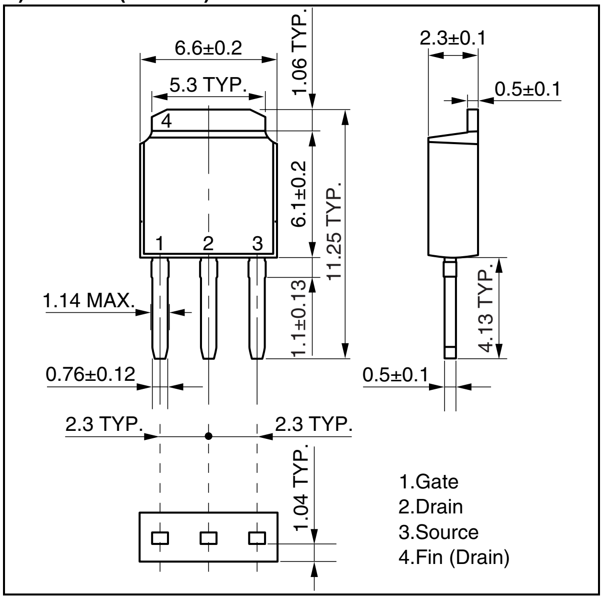


SINGLE AVALANCHE ENERGY
DERATING FACTOR

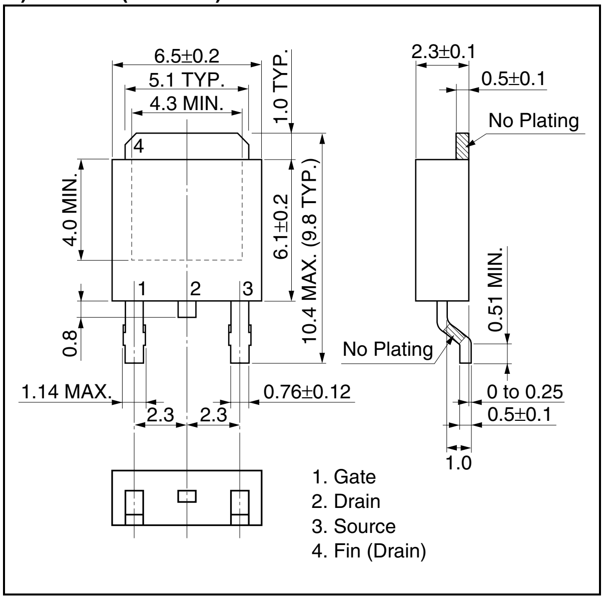


PACKAGE DRAWINGS (Unit: mm)

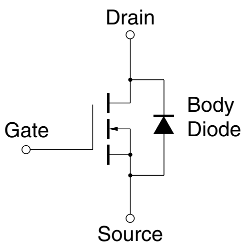
1) TO-251 (MP-3-b)



2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.