

## SWITCHING

## N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK4212A is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 8.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$   
 $R_{DS(on)2} = 14 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 20 \text{ A)}$
- Low total gate charge  
 $Q_G = 24 \text{ nC TYP. (} V_{DD} = 15 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$
- 4.5 V drive available
- Avalanche capability ratings

### ORDERING INFORMATION

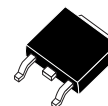
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4212A-ZK-E1-AY <sup>Note</sup>	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g
2SK4212A-ZK-E2-AY <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode).

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 48$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 125$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	16	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	25	mJ

(TO-252)



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$ ,  $L = 0.1 \text{ mH}$

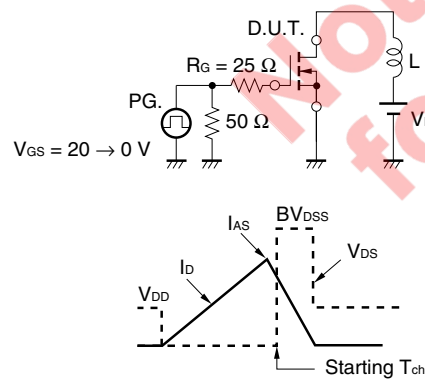
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# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

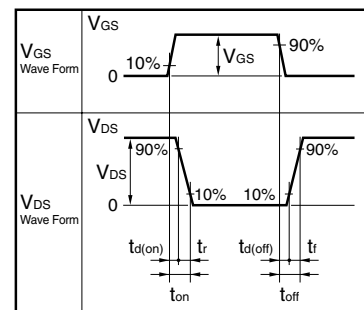
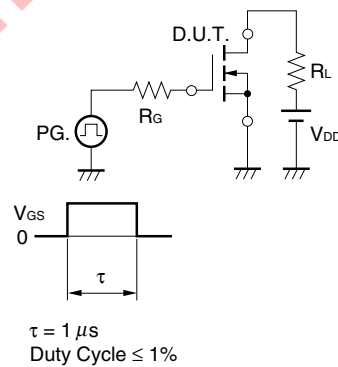
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5		3.0	V
Forward Transfer Admittance <b>Note</b>	y <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 12 A	9	19		S
Drain to Source On-state Resistance <b>Note</b>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		7.2	8.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		10.4	14	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V,		1200		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		180		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		100		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 30 A,		14		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		11		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 3 Ω		43		ns
Fall Time	t <sub>f</sub>			10		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		24		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V,		3		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 30 A		7		nC
Body Diode Forward Voltage <b>Note</b>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		0.89	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V,		21		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		12		nC

**Note** Pulsed

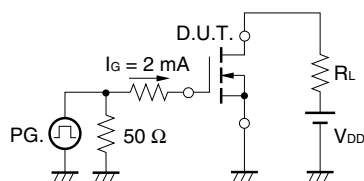
## TEST CIRCUIT 1 AVALANCHE CAPABILITY



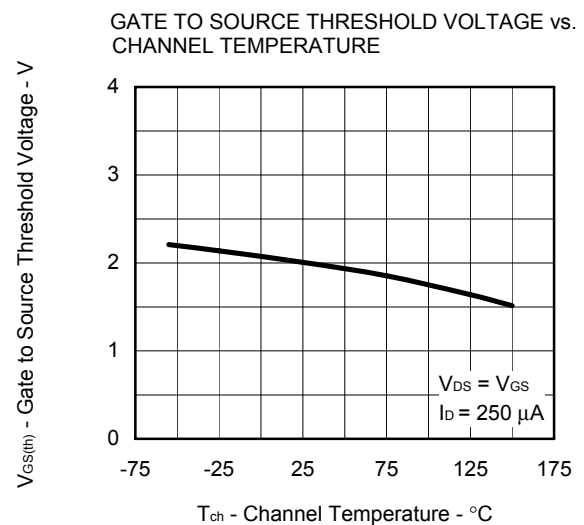
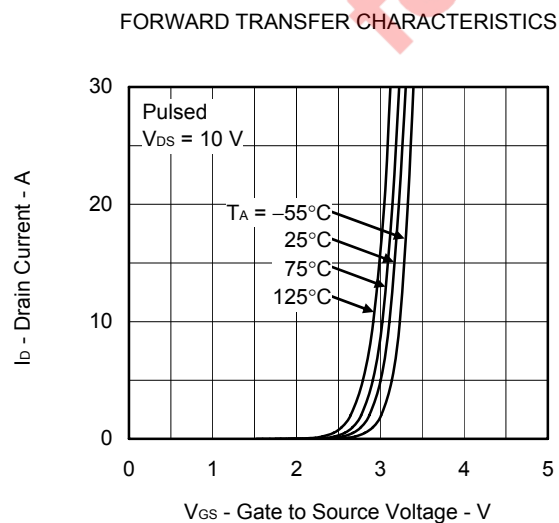
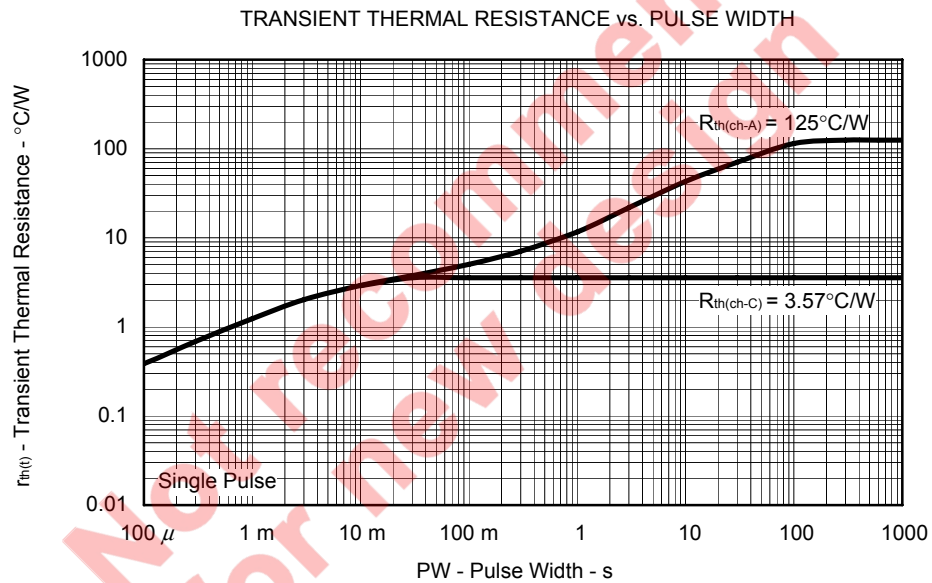
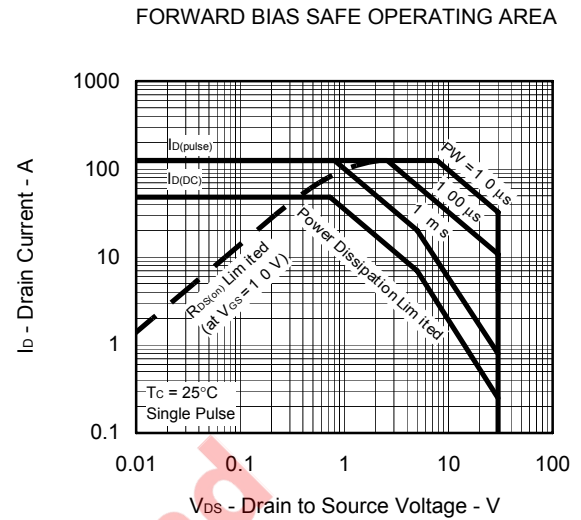
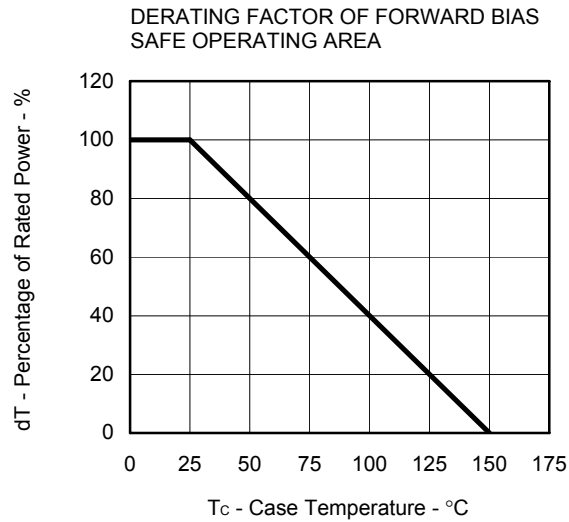
## TEST CIRCUIT 2 SWITCHING TIME



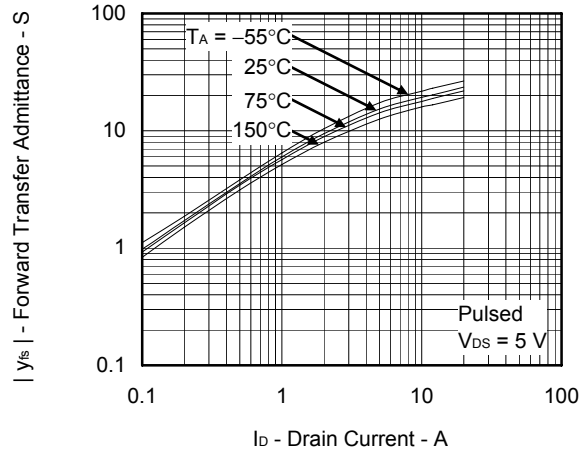
## TEST CIRCUIT 3 GATE CHARGE



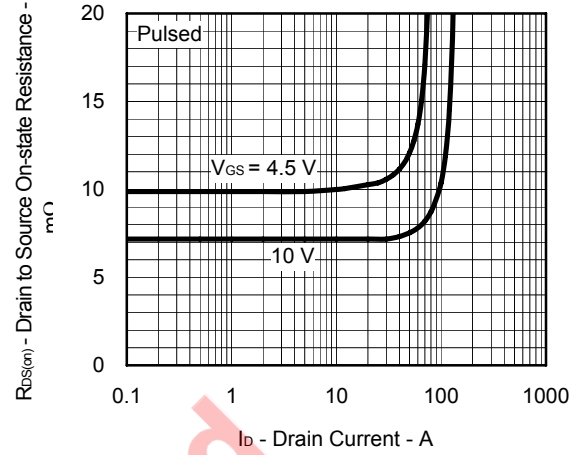
# TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



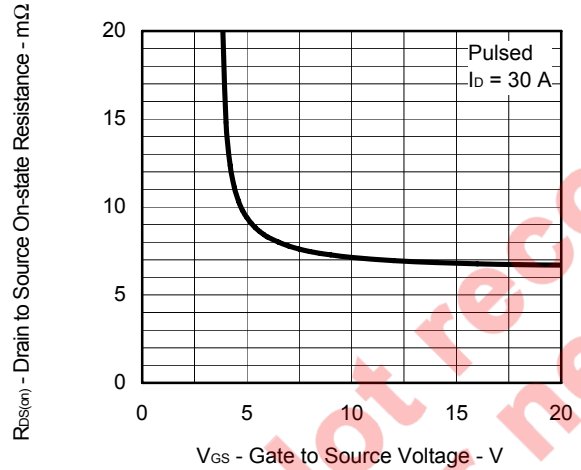
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



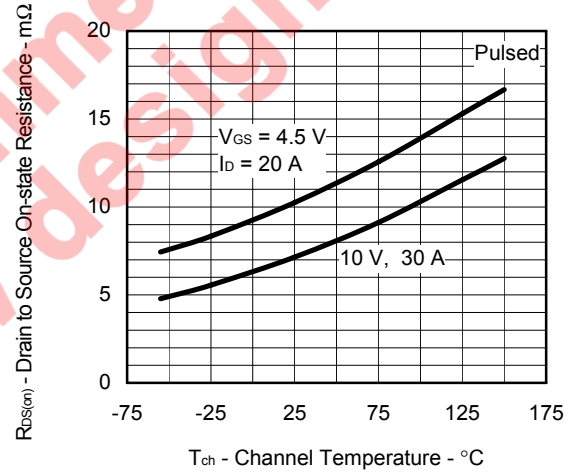
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



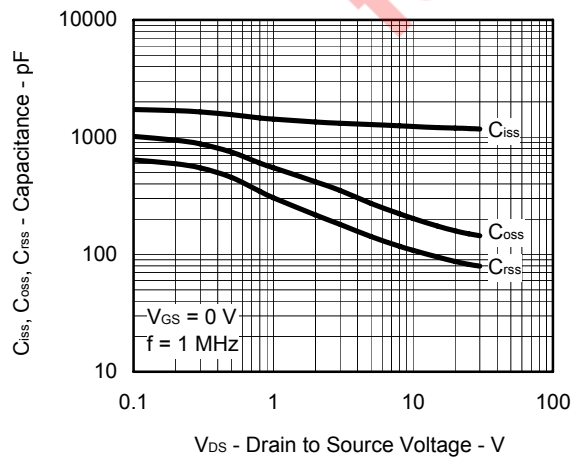
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



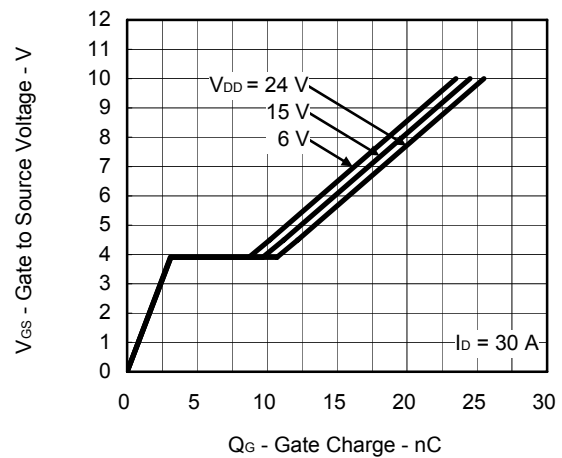
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

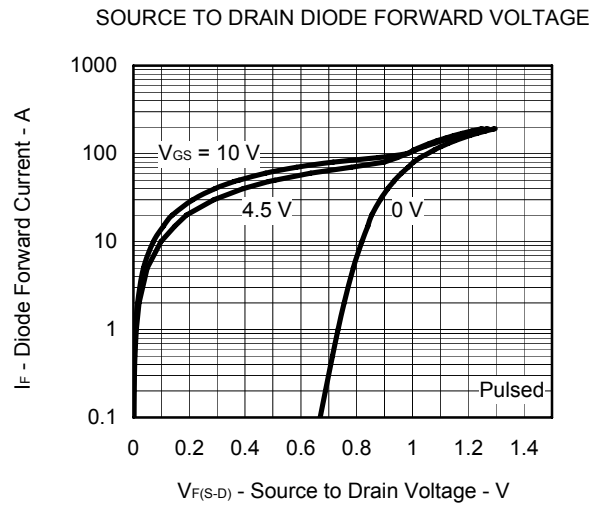


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

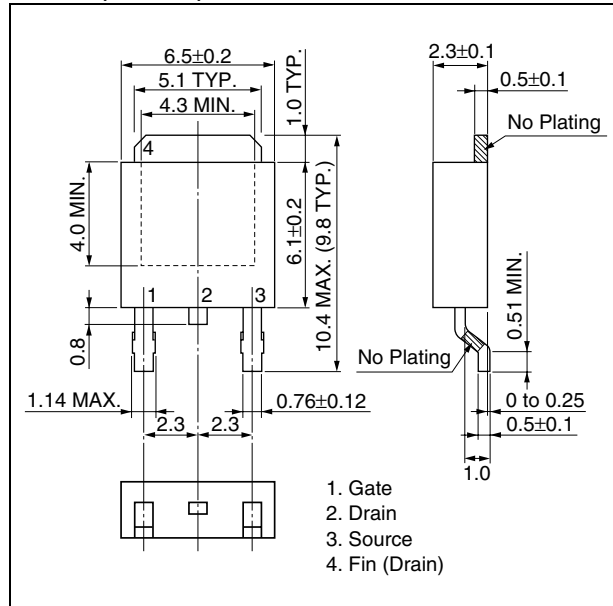




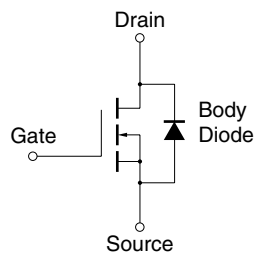
Not recommend  
for new design

PACKAGE DRAWINGS (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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