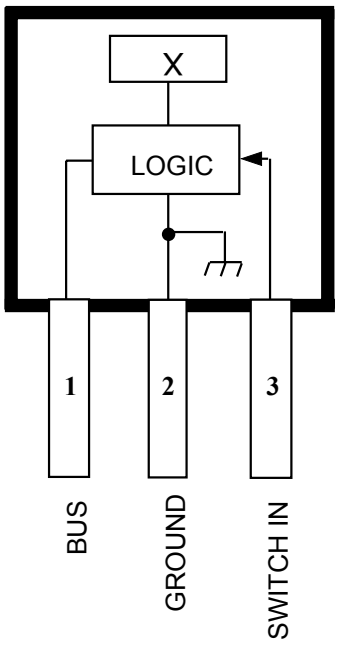
3054

Data Sheet
27680.1*

MULTIPLEXED TWO-WIRE HALL-EFFECT SENSOR ICs



Dwg. PH-005

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage, V_{BUS} . . . . . **18 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Operating Temperature Range, T_A
A3054KU . . . . . **-40°C to +125°C**
A3054SU . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**
Package Power Dissipation,
P_D . . . . . **635 mW**

The A3054KU and A3054SU Hall-effect sensor ICs are digital magnetic sensing ICs capable of communicating over a two-wire power/signal bus. Using a sequential addressing scheme, the device responds to a signal on the bus and returns the diagnostic status of the IC, as well as the status of each monitored external magnetic field. As many as 30 devices can function on the same two-wire bus. This IC is ideal for multiple sensor applications where minimizing the wiring harness size is desirable or essential.

Each device consists of high-resolution bipolar Hall-effect switching circuitry, the output of which drives high-density CMOS logic stages. The logic stages decode the address pulse and enable a response at the appropriate address. The combination of magnetic-field or switch-status sensing, low-noise amplification of the Hall-transducer output, and high-density decoding and control logic is made possible by the development of a new IC DABiC™ (digital analog bipolar CMOS) fabrication technology. The A3054SU is an improved replacement for the original UGN3055U.

These unique magnetic sensing ICs are available in two temperature ranges; the A3054SU operates within specifications between -20°C and +85°C, while the A3054KU is rated for operation between -40°C and +125°C. Alternative magnetic and temperature specifications are available on special order. Both versions are supplied in 0.060" (1.54 mm) thick, three-pin plastic SIPs. Each device is clearly marked with a two-digit device address (XX).

FEATURES

- Complete Multiplexed Hall-Effect ICs with Simple Sequential Addressing Protocol
- Allows Power and Communication Over a Two-Wire Bus (Supply/Signal and Ground)
- Up to 30 Hall-Effect Devices Can Share a Bus
- Diagnostic Capabilities
- Magnetic-Field or Switch-Status Sensing Applications
- Low Power of DABiC Technology Favors Battery-Powered and Mobile Applications
- Ideal for Automotive, Consumer, and Industrial Applications

Always order by complete part number:

Part Number	Operating Temperature Range
A3054KU-XX	-40°C to +125°C
A3054SU-XX	-20°C to +85°C

where XX = address (01, 02, … 29, 30).

ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits			
			Min	Typ	Max	Units
Power Supply Voltage	V_{BUS}		—	—	15	V
Signal Current	I_S	DUT Addressed, B > 300 G	12	15	20	mA
Quiescent Current	I_{QL}	V_{BUS} = 6 V	—	1.5	2.5	mA
	I_{QH}	V_{BUS} = 9 V	—	1.4	2.5	mA
	ΔI_Q	$I_{QL} - I_{QH}$	—	100	300	µA
Address Range	Addr	Factory Specified	1	—	30	—
Clock Thresholds	V_{CLH}	LOW to HIGH	—	—	8.5	V
	V_{CHL}	HIGH to LOW	6.5	—	—	V
	V_{CHYS}	Hysteresis	—	0.8	—	V
Max. Clock Frequency*	f_{CLK}	50% Duty Cycle	2.5	—	—	kHz
Address LOW Voltage	V_L		V_{RST}	6.0	V_{CHL}	V
Address HIGH Voltage	V_H		V_{CLH}	9.0	V_{BUS}	V
Reset Voltage	V_{RST}		2.5	3.5	5.5	V
Propagation Delay*	t_{plh}	LOW to HIGH	10	20	30	µs
	t_{phl}	HIGH to LOW	—	5.0	10	µs
Pin 3-2 Resistance	R_{SWH}	DUT Addressed, B < 5 G	—	50	—	kΩ
	R_{SWL}	DUT Addressed, B > 300 G	—	200	—	Ω
Pin 3-2 Output Voltage	V_{SWH}	DUT Addressed, B < 5 G	—	3.9	—	V
	V_{SWL}	DUT Addressed, B> 300 G	—	30	—	mV

MAGNETIC CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Magnetic Threshold†	B_{OP}	Turn-On	50	150	300	G
	B_{RP}	Turn-Off	5.0	100	295	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	5.0	50	—	G

Typical Data is at T_A = +25°C and is for design information only.
*This parameter, although warranteed, is not production tested.
†Alternative magnetic switch point specifications are available on special order. Please contact the factory.

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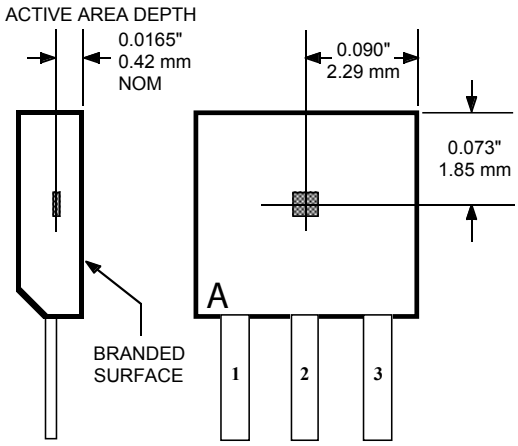
ELEMENT LOCATION

(±0.005” [0.13 mm] die placement)



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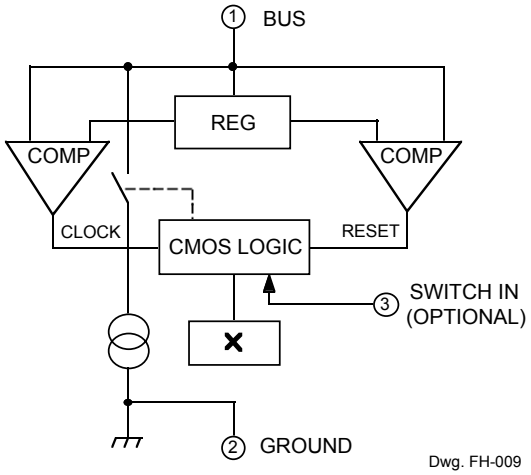
FUNCTIONAL BLOCK DIAGRAM



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DEFINITION OF TERMS

Device Address

Each bus device has a factory-specified predefined address. At present, allowable device addresses are integers from 01 to 30.

LOW-to-HIGH Clock Threshold (V_{CLH})

Minimum voltage required during the positive-going transition to increment the bus address and trigger a diagnostic response from the bus devices. This is also the maximum threshold of the on-chip comparator that monitors the supply voltage, V_{BUS}.

HIGH-to-LOW Threshold (V_{HL})

Maximum voltage required during the negative-going transition to trigger a *signal* current response from the bus devices. This is also the maximum threshold of the on-chip comparator that monitors the supply voltage, V_{BUS}.

Bus HIGH Voltage (V_H)

Bus HIGH voltage during addressing. Voltage should be greater than V_{CLH}.

Address LOW Voltage (V_L)

Bus LOW voltage during addressing. Voltage should be greater than V_{RST} and less than V_{CHL}.

Bus Reset Voltage (V_{RST})

Voltage level while resetting devices.

Devuce Quiescent Current Drain (I_Q)

The current drain of bus devices when active but not addressed. I_{QH} is the quiescent current drain when the device is not addressed and is at V_H I_{QL} is the quiescent current drain when the device is not addressed and is at V_L. Note that I_{QL} is greater than I_{QH}.

Diagnostic Phase

Period on the bus when the address voltage is at V_H. During this period, a correctly addressed device responds by increasing its current drain on the bus. This response from the device is called the **diagnostic response** and the bus current *increase* is called the **diagnostic current.**

Signal Phase

Period on the bus when the address voltage is at V_L. During this period, a correctly addressed device that detects a magnetic field greater than the magnetic operate point, B_{OP}, responds by maintaining a current drain of I_S on the bus. This response from the device is called the **signal response** and the bus current is called the **signal current.**

Device Address Response Current (I_S)

Device current during the *diagnostic* and the *signal* responses of the bus device. This is accomplished by enabling an internal constant-current source.

ADDRESSING PROTOCOL

Magnetic Operate Point (B_{OP})

Minimum magnetic field required to switch ON the Hall amplifier and switching circuitry of the addressed device. This circuitry is only active when the device is addressed.

Magnetic Release Point (B_{RP})

Magnetic field required to switch OFF the Hall amplifier and switching circuitry after the output has been switched ON. When a device is deactivated by changing the bus address, all magnetic memory is lost.

Magnetic Hysteresis (B_{HYS})

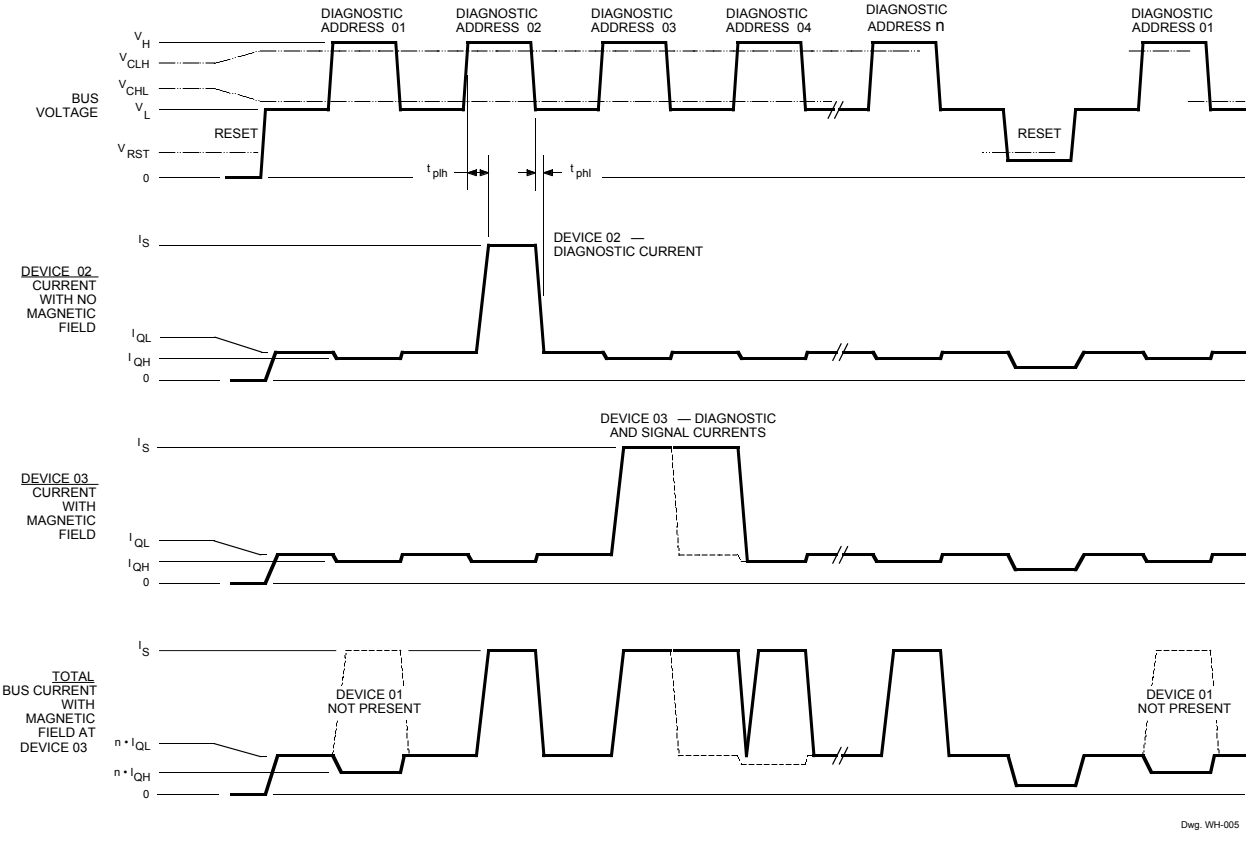
Difference between the B_{OP} and B_{RP} magnetic field thresholds.

A device may be addressed by changing the supply voltage as shown in Figure 1. A preferred addressing protocol is as follows: the bus supply voltage is brought low (<2.5 V) so that all devices on the bus are reset. The voltage is then raised to the address LOW voltage (V_L) and the bus quiescent current is measured. The bus is then toggled between V_L and V_H (address HIGH voltage), with each positive transition representing an increment in the bus address. After each voltage transition, the bus current may be monitored to check for diagnostic and signal responses from sensor ICs.

Device Addressing

When a device detects a bus address equal to its factory-programmed address, it responds with an increase in its supply current drain (I_S) during the next HIGH portion

FIGURE 1
BUS TIMING



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ofthe address cycle. This response may be used as an indication that the device is "alive and well" on the bus and is called the *diagnostic* response. If the device detects an ambient magnetic field, it continues with I_S during the low portion of the address cycle. This response from the device is called the *signal* response. When the next positive (address) transition is detected, the device becomes disabled, and its contribution to the bus signal current returns to I_Q.

Bus Current

Figure 1 shows the addressing protocol. The top trace represents the bus voltage transitions as controlled by the bus driver (see Applications Notes for an optimal bus driver schematic). The second trace represents the bus current contribution of Device 02. The *diagnostic* response from the device indicates that it detected its address on the bus. However, no *signal* current is shown, which indicates that sufficient magnetic field is not detected at the chip surface and that pin 3 is open circuited. The third trace represents the current drain of Device 03 when a magnetic field is detected. Note both the *diagnostic* and *signal* currents from the device. The last trace represents the overall bus current drain. When no devices are addressed, the net bus current is the sum of quiescent currents of all devices on the bus (for 'n' devices, the bus current drain is $n \bullet I_Q$).

Bus Issues

After a reset, while at the address LOW voltage (VL), and before the first address pulse, bus current calibration may be performed. This feature allows for fail-safe detection of signal current and eliminates detection problems caused by low signal current (I_S), the operation of devices at various ambient temperatures, lot-to-lot variation of quiescent current, and the addition or replacement of devices to the bus while in the field. At present, a maximum of 30 active devices can coexist on the same bus, each with a different address. Address

TYPICAL DEVICE QUIESCENT CURRENT

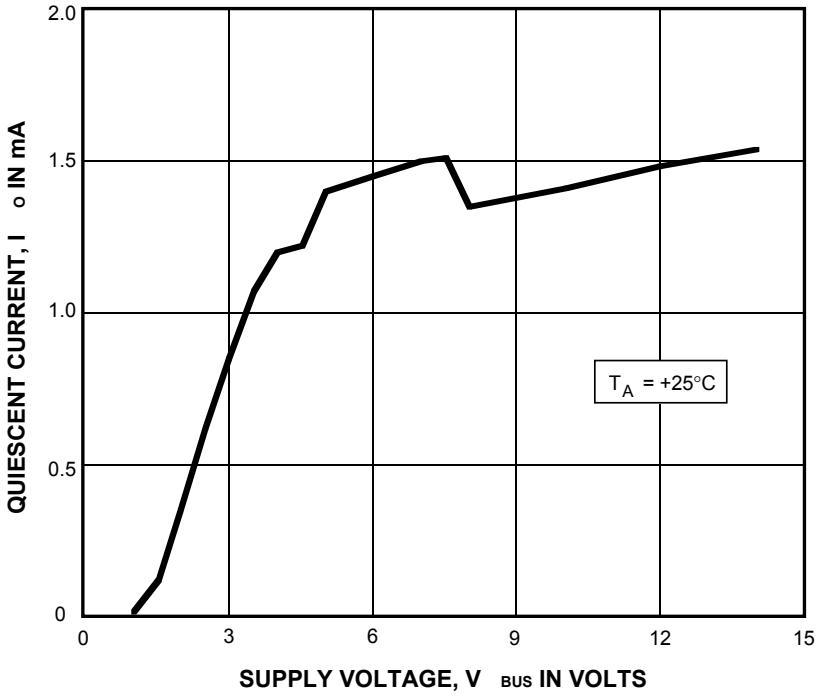

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FIGURE 2
DEVICE CONNECTIONS

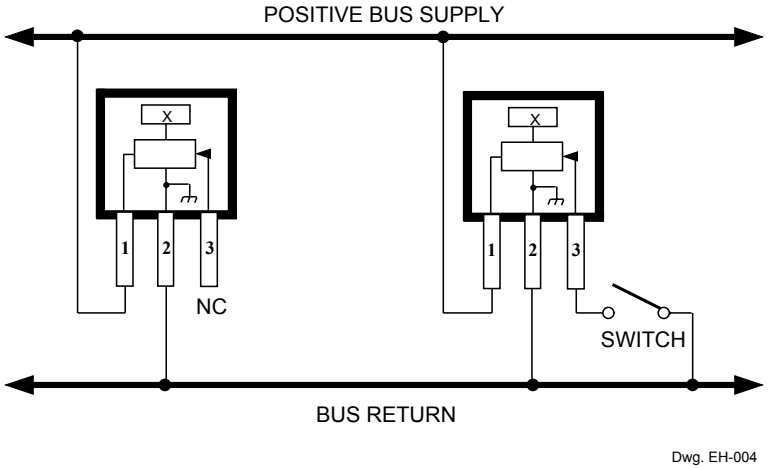

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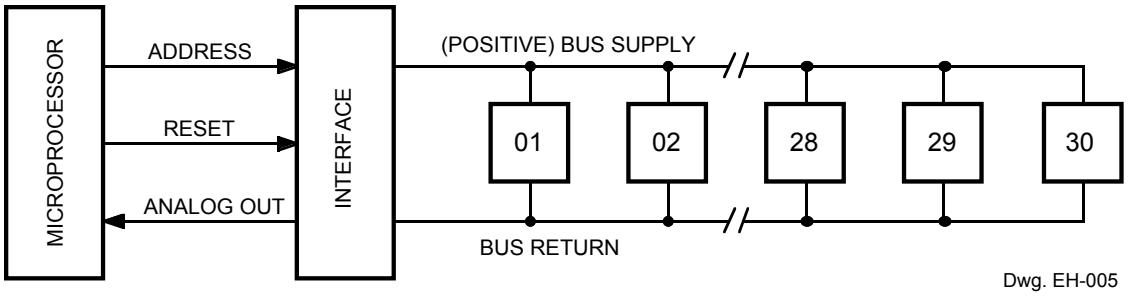
FIGURE 3
BUS INTERCONNECTION



31 is designed to be inactive to allow for further address expansion of the bus (to 62 maximum addresses). In order to repeat the address cycle, the bus must be reset, as shown in Figure 1, by bringing the supply voltage to below V_{RST}. Devices have been designed not to 'wrap-around'.

Magnetic Characteristics

The device IC has been designed to respond to an external magnetic field whose magnetic strength is greater than B_{OP}. It accomplishes this by amplifying the output of an on-chip Hall transducer and applying it to a threshold detector. In order that bus current is kept to a minimum, the transducer and amplification circuitry is kept powered down until the device is addressed. Hence, the magnetic status is evaluated only when the device is addressed.

External Switch Sensing

Pin 3 of the IC may be used to detect the status of an external switch when magnetic field sensing is not desired (and in the absence of a magnetic field). The allowable states for the switch are 'open' or 'closed' (shorted to device ground).

APPLICATIONS NOTES

Magnetic Actuation

The left side of Figure 2 shows the wiring of an A3054KU or A3054SU when used as a magnetic threshold detector. Pin 1 of the device is wired to the positive terminal of the bus, pin 2 is connected to the bus negative terminal, and *pin 3 has no connection.*

Mechanical Actuation

The right side of Figure 2 shows the wiring of an A3054KU or A3054SU when used to detect the status of a mechanical switch. In this case, pin 3 is connected to the switch. The other side of the switch is connected to the bus return (negative bus supply or ground). When the mechanical switch is closed, and the correct bus address is detected by the IC, the device responds with a signal current. If the switch is open, only the diagnostic current is returned.

Bus Configuration

A maximum of 30 individually addresable devices may be connected across the same two-wire bus as shown in Figure 3. It is recommended that the devices use a dedicated digital ground wire to minimize the effects of changing ground potential (as in the case of chassis ground in the automotive industry).

The bus was not designed to require two-wire twisted pair wiring to the devices. However, in areas of extreme electromagnetic interference, it may be advisable to install a small bypass capacitor (0.01 μF for example) between the supply and ground terminals of each device instead of using the more expensive wiring.

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Bus Driver

It is recommended that the bus be controlled by microprocessor-based hardware for the following reasons:

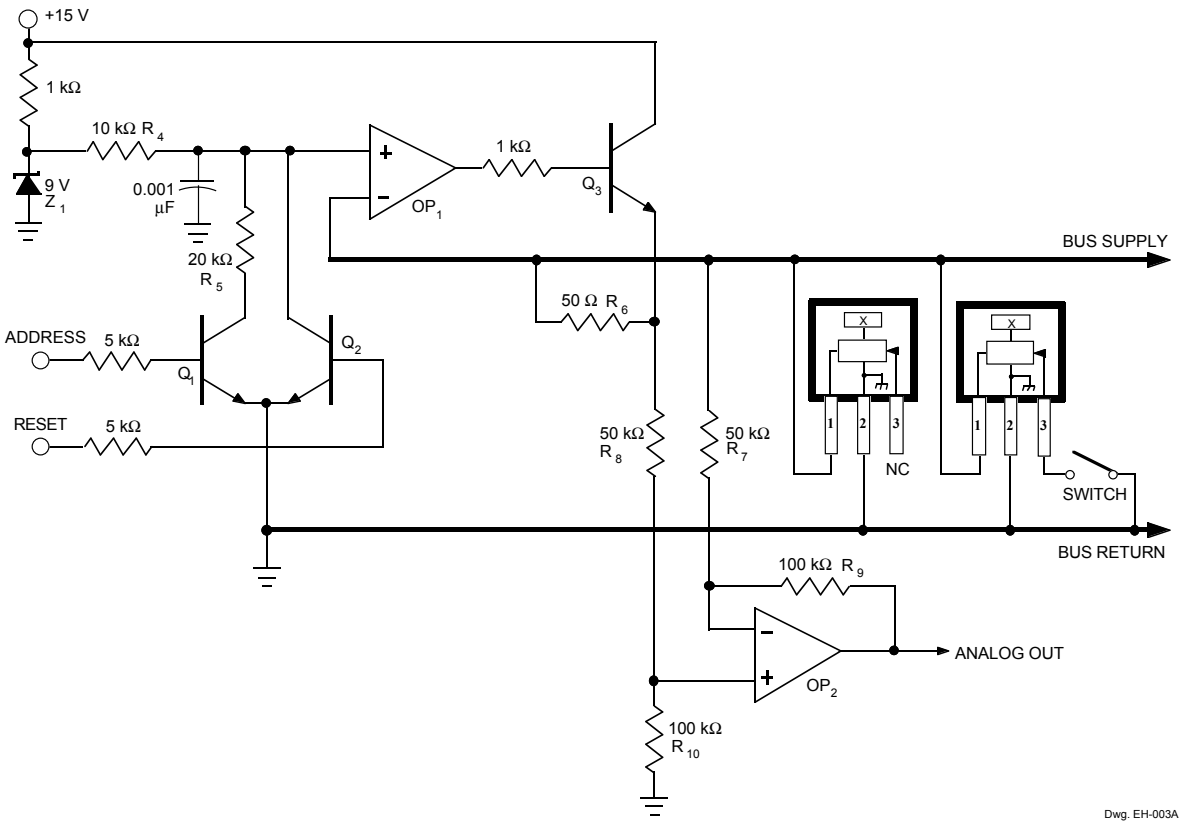
- Device address information may be stored in ROM in the form of a look-up table.
- Bus faults can be pinpointed by the microprocessor by comparing the diagnostic response to the expected response in the ROM look-up table.
- The microprocessor, along with an A/D converter, can also be used to self calibrate the quiescent currents in the bus and hence be able to easily detect a signal response.
- The microprocessor can also be used to filter out random line noise by digitally filtering the bus responses.
- The microprocessor can easily keep track of the signal responses and initiate the appropriate action (e.g., light a lamp or sound an alarm, and also pinpoint the location of the signal).

Optimally, the microprocessor is used to control bus-driving circuitry that will accept TTL-level inputs to drive the bus and will return an analog voltage representation of the bus current.

Interface Schematic

The bus driver is easily designed using a few operational amplifiers, resistors, and transistors. Figure 4 shows a schematic of a recommended bus driver circuit that is capable of providing 6 V to 9 V transitions, resetting the bus, and providing an analog measurement of the bus current for the A/D input of the microprocessor.

FIGURE 4
BUS INTERFACE SCHEMATIC



In Figure 4, the ADDRESS input provides a TTL-compatible input to control the bus supply. A HIGH (5 V) input switches Q_1 ON and sets the bus voltage to 6 V through the resistor divider R_4, R_5, and Zener Z_1. A LOW input switches Q_1 OFF and sets the bus voltage to 9 V (Z_1). This voltage is fed into the positive input of the operational amplifier OP_1 and is buffered and made available at BUS SUPPLY (or device supply). Bus reset control is also available in the form of a TTL-compatible input. When the RESET input is HIGH, Q_2 is switched ON and the positive input of the operational amplifier is set to the saturation voltage of the transistor (approximately 0 V). This resets the bus.

A linear reading of the bus current is made possible by amplifying the voltage generated across R_6 (which is $I_{BUS} \bullet R_6$). The amplifier, OP_2, is a standard differential amplifier of gain R_9/R_7 (provided that $R_7 = R_8$, $R_9 = R_{10}$). The gain of the total transim-pedance amplifier is given by:

$$V_{OUT} = I_{BUS} \bullet R_6 \bullet R_9/R_7$$

This voltage is available at the ANALOG OUT terminal.

Bus Control Software

The processing of the bus current (available at ANALOG OUT) is best done by feeding it into the A/D input of a microprocessor. If the flexibility provided by a microprocessor is not desired, this signal could be fed into threshold detection circuitry; e.g., comparator, and the output used to drive a display.

Related References

1. G. AVERY, "Two-Terminal Hall Sensor," *ASSIGNEE: Sprague Electric Company, North Adams, MA, United States. Patent number 4,374,333; Feb. 1983.*

2. T. WROBLEWSKI and F. MEISTERFIELD, "Switch Status Monitoring System, Single-Wire Bus, Smart Sensor Arrangement There Of," *ASSIGNEE: Chrysler Motor Corporation, Highland Park, MI, United States. Patent number 4,677,308; June 1987.*

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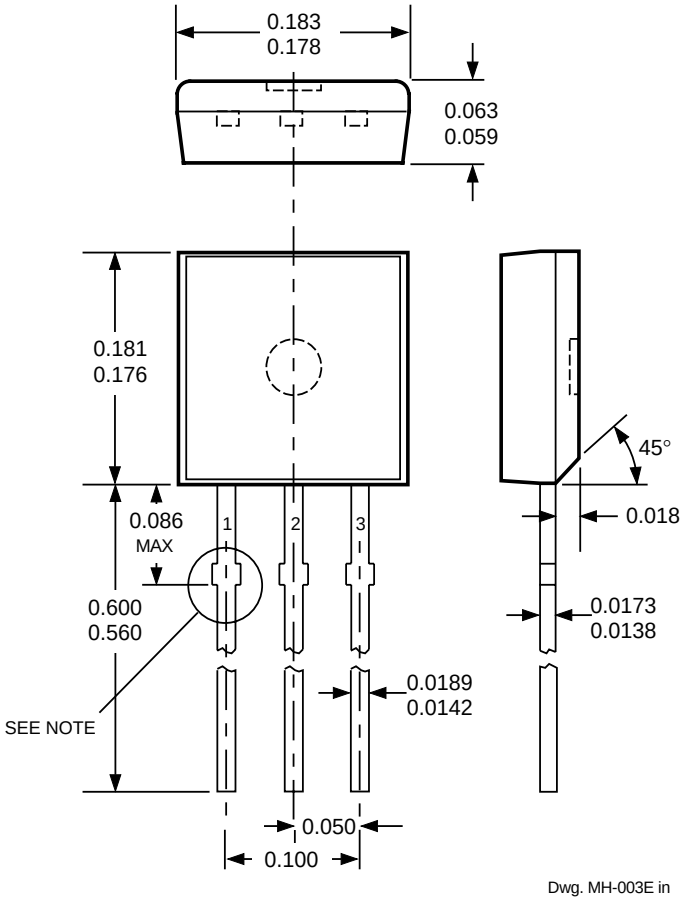
Dimensions in Inches
(controlling dimensions)



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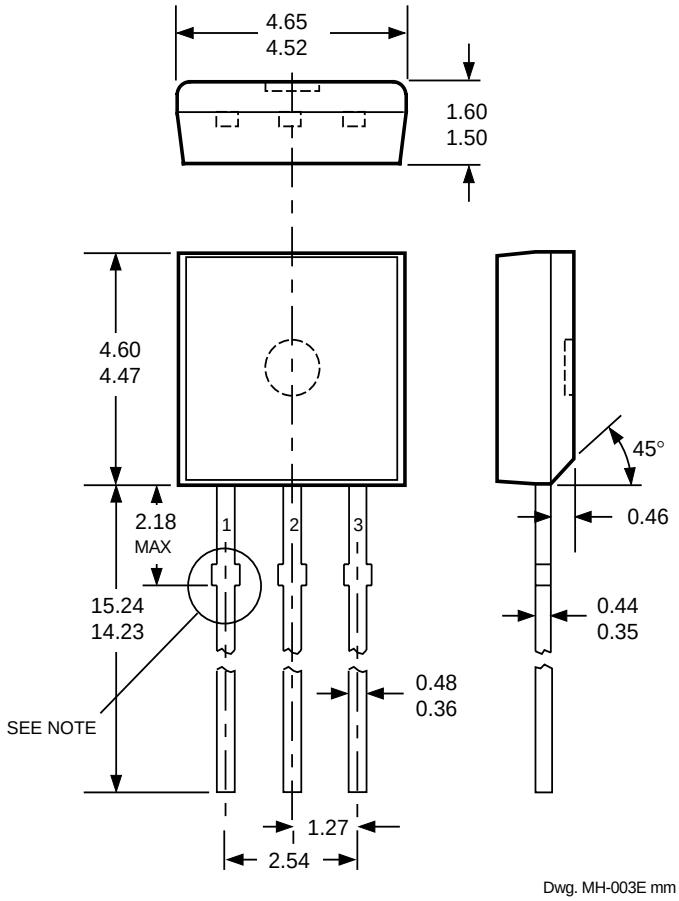
Dimensions in Millimeters
(for reference only)



Dwg. MH-003E mm

NOTES:1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

2. Exact body and lead configuration at vendor's option within limits shown.

3. Height does not include mold gate flash.

4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).

5. Where no tolerance is specified, dimension is nominal.

6. Minimum lead length was 0.500" (12.70 mm). If existing product to the original specifications is not acceptable, contact sales office before ordering.

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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