RS data

Keyboard encoder i.c. 309-509

The RS2376 Keyboard Encoder I.C. is a fully integrated P-MOS keyswitch encoding circuit, suitable for encoding a keyboard with up to 88 switches, plus shift and control, into a useable 9 bit data code, i.e. the standard 8 bit ASC II data code + one parity bit.

The RS2376 offers the facilities of two key roll-over operation with N-key lockout and has user-selectable odd or even parity and output polarity. A self contained oscillator and debounce circuit are incorporated in the device, requiring only the addition of a resistor and capacitor for each function. The outputs are directly TTL/MOS logic compatible.

The RS 76 key Keyboard (336-703) is designed to accept the RS2376 Keyboard Encoder I.C., enabling a full ASCII code keyboard to be easily constructed.

Features

- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.

Figure 1 **Pin connections**

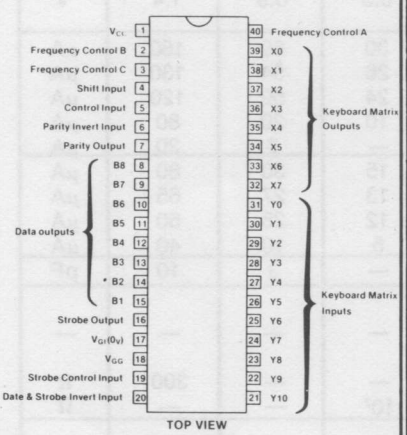
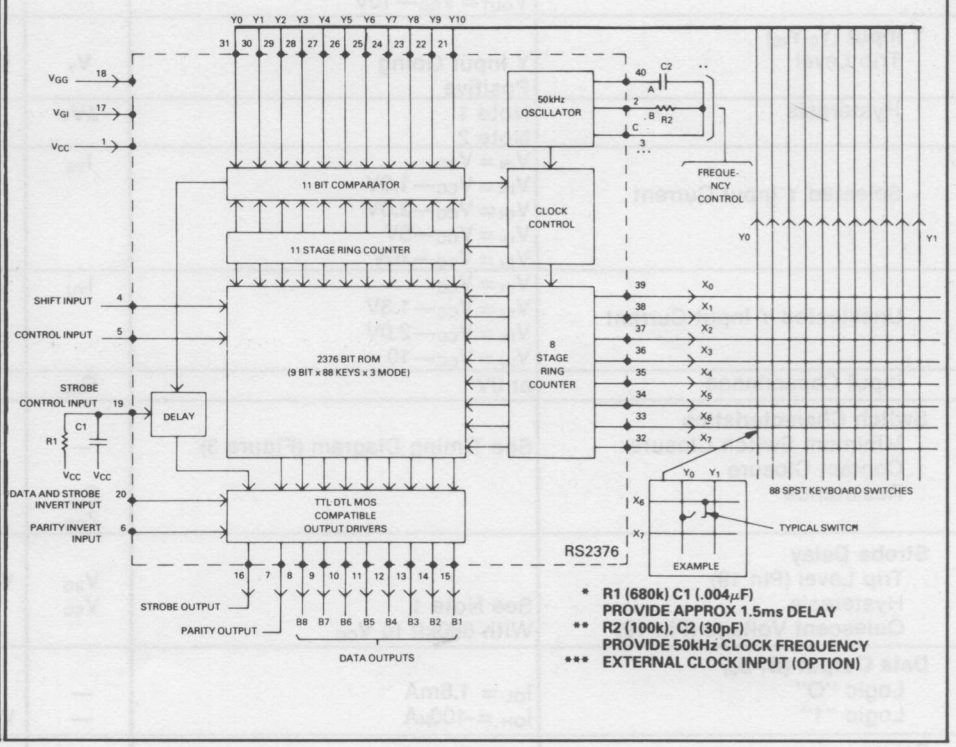


Figure 2 **Block diagram**



Electrical characteristics

Maximum ratings

V_{GI} and V_{GG} (with respect to V_{CC}) ——— −20V to +0.3 V
Logic input voltages (with respect to V_{CC}) ——— −20 V to 0.3 V
Storage Temperature ——— −65°C to +150°C
Operating Temperature Range ——— 0°C to +70°C

Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC}=5 Volts ± 0.5 Volts, (V_{cc}=Substrate Voltage)
V_{GG}=−12 Volts ± 1.0 Volts, V_{GI}=OV
Operating Temperature (TA)=0°C to +70°C

Characteristics	Conditions	Symbol	Min	Typ*	Max	Units
Clock Frequency	See Block diagram (Figure 2) footnote for typical R — C values	f	10	50	100	kHz
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level		V_{10}	V_{GG}	—	+0.8	V
Logic "1" Level		V_{11}	V_{CC}−1.5	—	V_{CC}+0.3	V
Shift & Control Input Current	V_I = +5V	$I_{INS,C}$	15	36	60	μA
	V_I = 0V		8	16	30	μA
Data, Parity Invert Input Current	V_I = −5V to +5V	$I_{IND,P}$	—	.01	1	μA
X Output (X_0-X_7) Logic "1" Output Current	V_{OUT} = V_{CC}	I_{XI}	—	0	—	μA
	V_{OUT} = V_{CC}−1.3V		80	150	400	μA
	V_{OUT} = V_{CC}−2.0V		140	300	800	μA
	V_{OUT} = V_{CC}−5V		250	700	1500	μA
	V_{OUT} = V_{CC}−10V		500	1500	3000	μA
Logic "0" Output Current	V_{OUT} = V_{CC}	I_{XO}	15	30	80	μA
	V_{OUT} = V_{CC}−1.3V		13	27	65	μA
	V_{OUT} = V_{CC}−2.0V		12	25	60	μA
	V_{OUT} = V_{CC}−5V		5	10	40	μA
	V_{OUT} = V_{CC}−10V		—	1	20	μA
Y Input (Y_0-Y_{10}) Trip Level	Y Input Going Positive	V_Y	V_{CC}−5	V_{CC}−3	V_{CC}−2	V
Hysteresis	Note 1	ΔV_Y	0.5	0.9	1.4	V
	Note 2					
Selected Y Input Current	V_{IN} = V_{CC}	I_{YS}	30	60	160	μA
	V_{IN} = V_{CC}−1.3V		26	54	130	μA
	V_{IN} = V_{CC}−2.0V		24	50	120	μA
	V_{IN} = V_{CC}−5V		10	20	80	μA
	V_{IN} = V_{CC}−10V		—	2	20	μA
Unselected Y Input Current	V_{IN} = V_{CC}	I_{YU}	15	30	80	μA
	V_{IN} = V_{CC}−1.3V		13	27	65	μA
	V_{IN} = V_{CC}−2.0V		12	25	60	μA
	V_{IN} = V_{CC}−10		5	10	40	μA
Input Capacitance	at 0V	C_{IN}	—	3	10	pF
Switch Characteristics Minimum Switch Closure	See Timing Diagram (Figure 3)	—	—	—	—	—
Contact Closure Resistance		Z_{CC}	—	—	300	Ω
		Z_{CO}	10^7	—	—	Ω
Strobe Delay Trip Level (Pin 19)		V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V
Hysteresis	See Note 1	V_{SD}	0.5	0.9	1.4	V
Quiescent Voltage (Pin 19)	With 680kΩ to V_{CC}		−3	−5	−8	V
Data Output (B_1-B_9) Logic "O"	I_{OL} = 1.6mA	—	—	—	0.4	V
Logic "1"	I_{OH} =−100μA	—	V_{CC}−1	—	—	V
Power I_{CC}	V_{CC} = +5V	—	—	5	10	mA
I_{GG}	V_{GG} = −12V	—	—	5	10	mA

*Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output=eleven.

Operation

The RS2376 contains a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/MOS compatible output drivers.

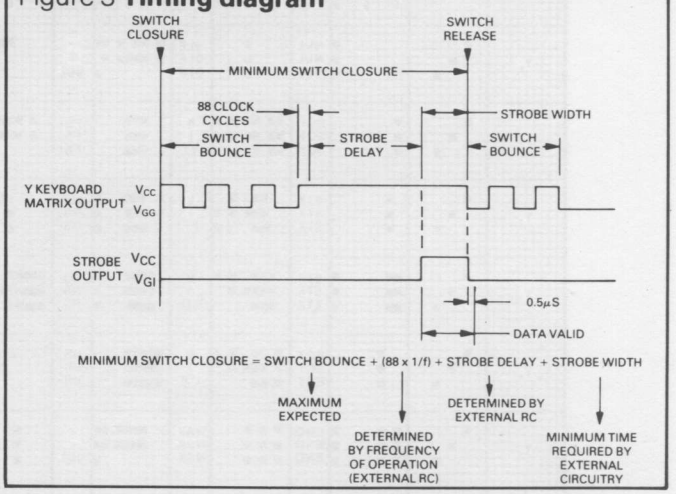
The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0-X7) and one input of the 11-bit cmparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1-D8 (pins 8-15) and the Strobe Output (pin 16).

Figure 3 **Timing diagram**



Typical characteristic curves

Figure 4 **Strobe delay VS. C1**

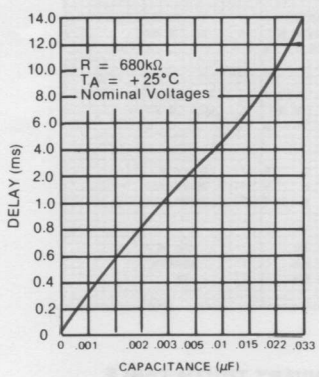


Figure 5 **Oscillator frequency VS. C2**

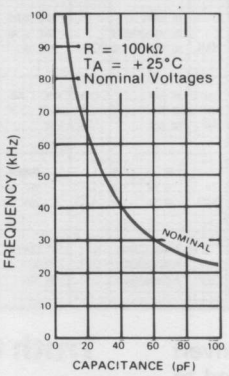


Figure 6 **Typical output on resistance (R_{DON}) VS. Gate bias voltage (V_{GS})**

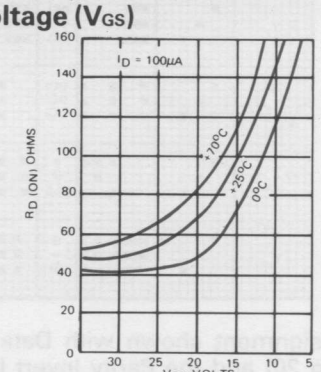


Figure 7 **Typical power consumption (mW) VS. Temp (°C)**

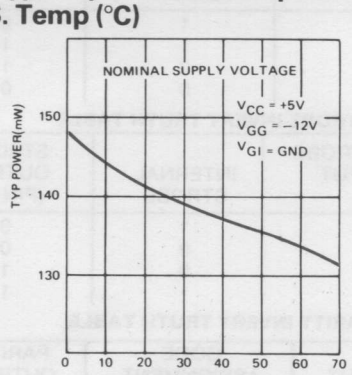
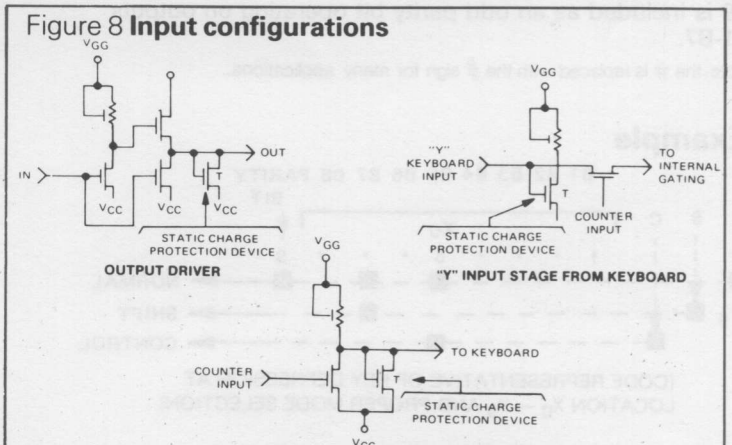


Figure 8 **Input configurations**



Power supply connections

Figure 9 **TTL operation**

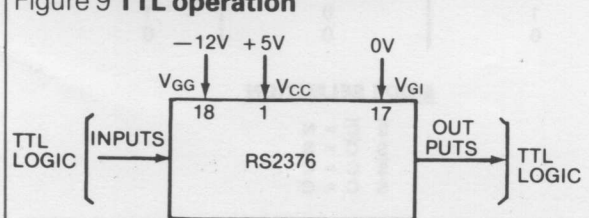
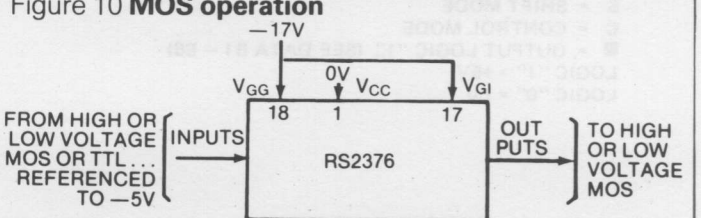


Figure 10 **MOS operation**



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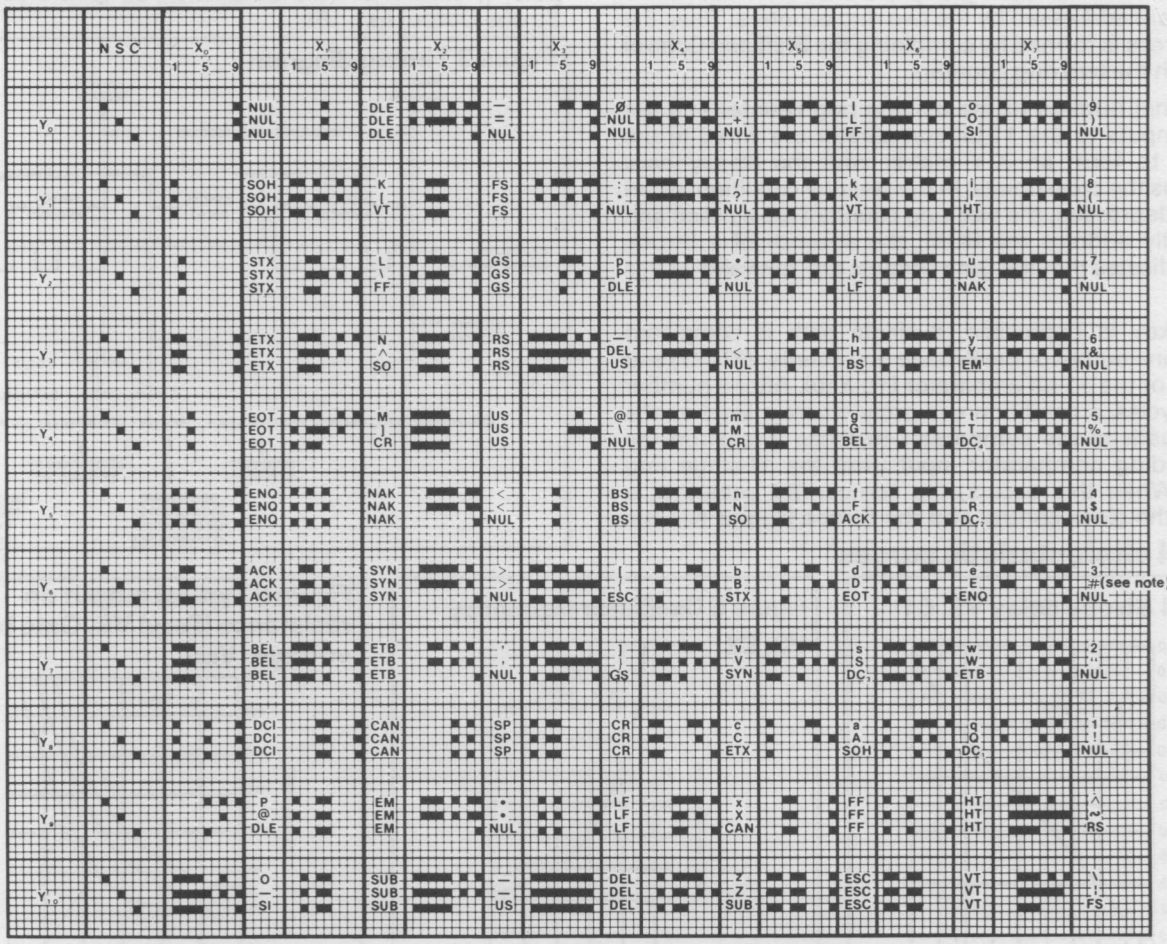
Code assignment chart

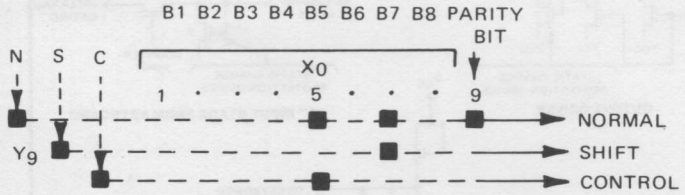
■ represents a Logic "1"



Code Assignment shown with Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6) tied to Logic "O". This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

Note: the # is replaced with the £ sign for many applications.

Example



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0 — Y_9 AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = 0V

Truth tables

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

MODE SELECTION

$\overline{S}\ \overline{C}$ = N
$S\ \overline{C}$ = S
$\overline{S}\ C$ = C
$S\ C$ = C

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