DESCRIPTION

The 3101A is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 3101A is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 3101A assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 3101A is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N3101A, B or F. For the military temperature range (−55°C to +125°C) specify S3101A, F only.

FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
  S3101A – 50ns, MAXIMUM
  N3101A – 35ns, MAXIMUM
- WRITE CYCLE TIME:
  S3101A – 25ns, MAXIMUM
  N3101A – 25ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S3101A – (−150μA) MAXIMUM
  N3101A – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

APPLICATIONS

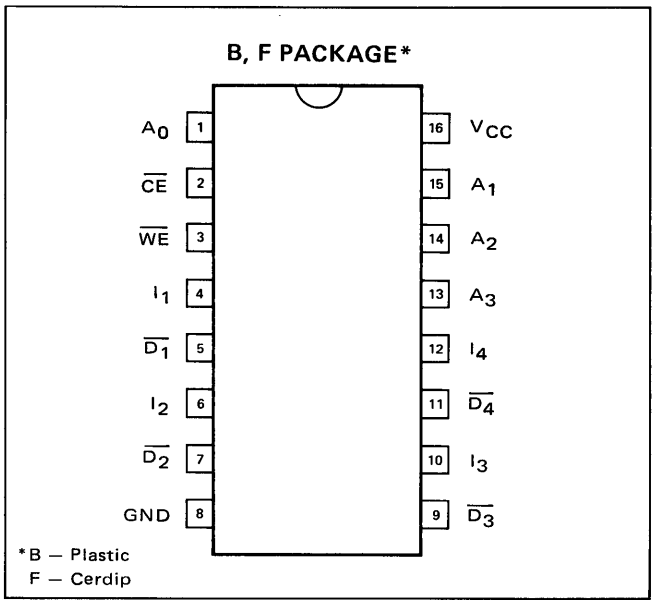
SCRATCH PAD MEMORY

BUFFER MEMORY

PUSH DOWN STACKS

CONTROL STORE

PIN CONFIGURATION

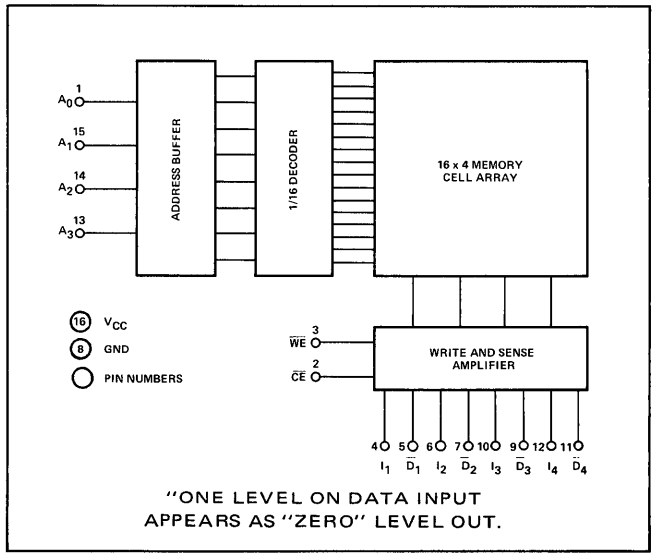


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{D}_N$
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	1
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N3101A)	0° to +75°	°C
	(S3101A)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A[1,2,3]			N3101A[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	$V_{IN} = 0.45V$		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	$V_{IN} = 5.5V$			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	$I_{IN} = -12mA$, V_{CC} = MIN (Note 6)					−1.0	−1.5	V
		$I_{IN} = -18mA$, V_{CC} = MIN (Note 6)		−0.8	−1.2				V
V_{OL}	"0" Output Voltage	$I_{OUT} = 16mA$, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	$V_{IH} = 2.0V$, $V_{CC} = 5.0V$		5			5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0V$, $V_{CC} = 5.0V$, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	105		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", $V_{OUT} = 5.5V$, V_{CC} = MIN		<1	100		<1.0	100	μA
		$\overline{CE}$ = "1", $V_{OUT} = 2.4V$, V_{CC} = MIN		<1	40				μA

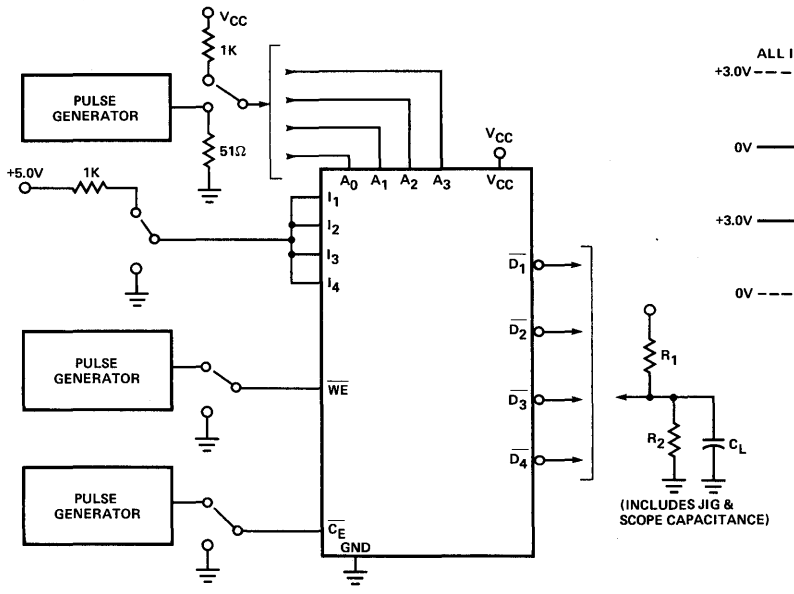
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.

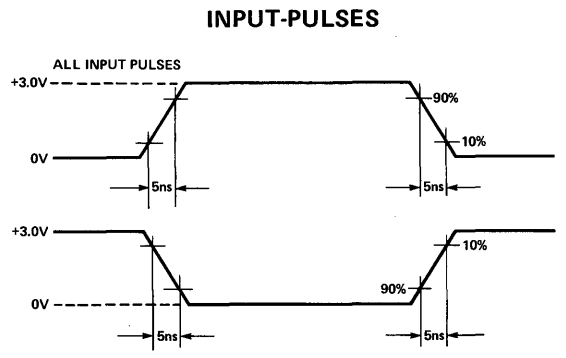
SWITCHING CHARACTERISTICS

S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A			N3101A			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			25	50	10		35	ns
T_{CE}	Chip Enable Access Time			12	25	5		17	ns
T_{CD}	Chip Enable Output Disable Time			12	25	5		17	ns
T_{WD}	Write Enable to Output Disable Time			15	25			20	ns
T_{WR}	Write Recovery Time			22	40			35	ns
Write Set-up Times		$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$							
T_{WSA}	Address to Write Enable		0			0	-8		ns
T_{WSD}	Data In to Write Enable		25			20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0			0	-5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		0			0			ns
T_{WHD}	Data In to Write Enable		0			0	-3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		0			0			ns
T_{WP}	Write Enable Pulse Width (Note 7)		25	18		25	18		ns

AC TEST LOAD AND WAVEFORMS



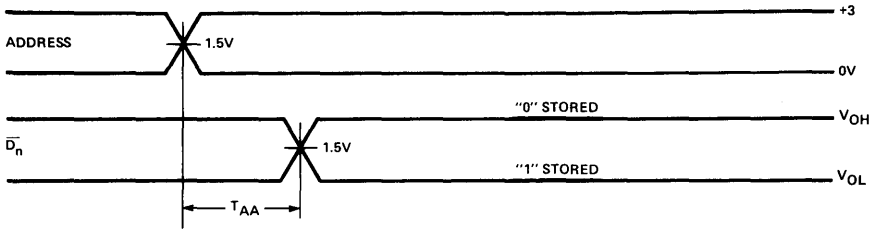


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

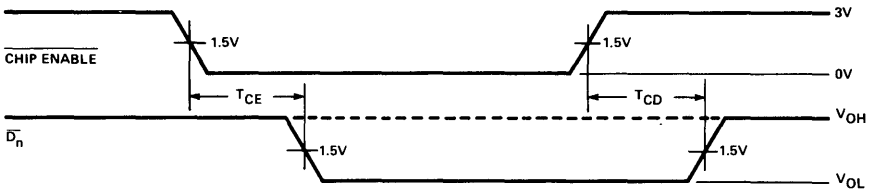
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

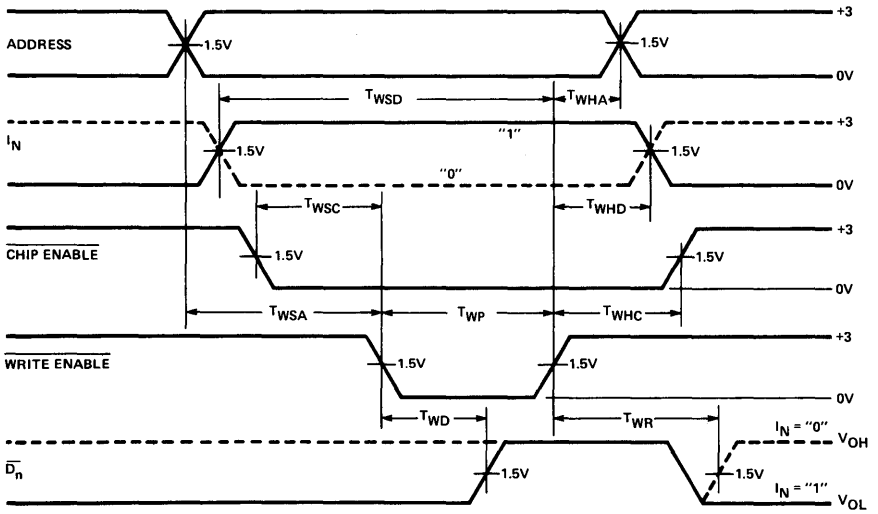
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.