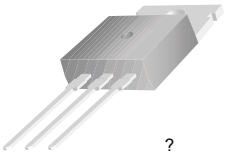
3205

product description

FHP3205 is a low-voltage high-current power MOS field effect transistor, widely used in power inverters

Features

110A, 55V, RDS(on) = 8.0mΩ fast switching speed



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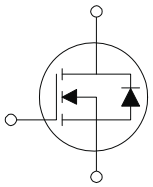
Pb

Available

RoHS*

COMPLIANT



Limit value (TC=25℃)

parameter name	symbol	Parameter value	unit
Drain-source voltage	V_{DS}	55	V
Drain current @Tc=25℃	I_D	110	A
Gate-source voltage	V_{GS}	±20	V
Dissipated power @Tc=25℃	P_D	200	W
Junction temperature	T_J	175	℃
Storage temperature	T_{stg}	-55 ~ 175	℃
avalanche	E_{AS}	20	mJ

Dynamic characteristic value

Parameter Description	symbol	Test Conditions	Minimum value	Typical value	maximum	unit
Input capacitance Output	C_{iss}	$V_{DS=25v}$, $V_{GS=0V}$, f=1.0 MHz	--	3247	--	pF
capacitance Reverse	C_{oss}	$V_{DS=25v}$, $V_{GS=0V}$, f=1.0 MHz	--	781	--	pF
transmission capacitance	C_{rss}	$V_{DS=25v}$, $V_{GS=0V}$, f=1.0 MHz	--	211	--	pF

	B_{VDSS}	$V_{GS=0V}$, $I_{D=250\mu}$ A	55	--	--V	
	I_{DSS}	$V_{DS=55v}$, $V_{GS=0V}$	--	--	25	μA
	$I_{GSS(F/R)}$	$V_{GS=20V}$, $V_{DS=0V}$	--	--	100	nA
	$R_{DS(ON)}$	$V_{GS=10V}$, $I_{D=62A}$	--	--	8.0	
	$V_{GS(th)}$	$V_{DS=}$ V_{GS}, $I_{D=250\mu A}$	2.0	--	4.0 V	
	g_{FS}	$I_{D=62A}$, $V_{DS=25V}$	44	--	--S	

	Qg	$V_{DS=44V}$ $I_{D=62A}$ $V_{GS=10V}$	--	--	146	nC
	Qgs		--	--	35	nC
	Qgd		--	--	54	nC

( )	Td(on)	$V_{DD=28V}$ $I_{D=62A}$ $R_{G=4.5?}$ $V_{GS=10V}$	--	14	--	ns
	Tr		--	101	--	ns
	Td(off)		--	50	--	ns
	tf		--	65	--	ns

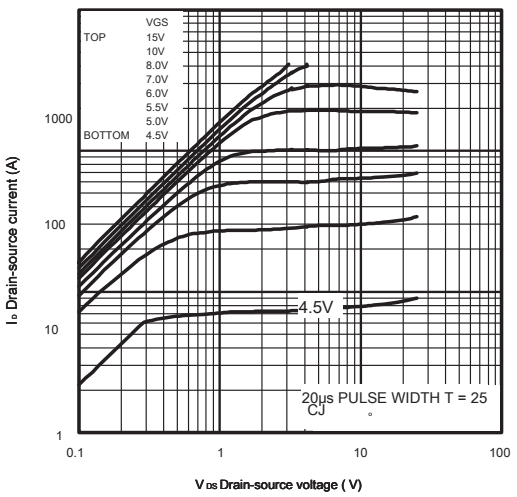


Fig 1. Output characteristics

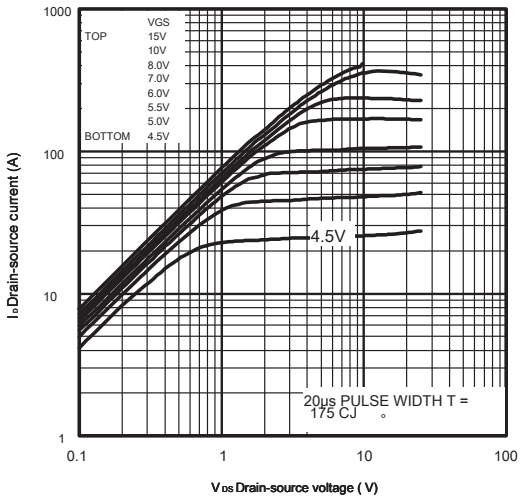


Fig 2. Output characteristics

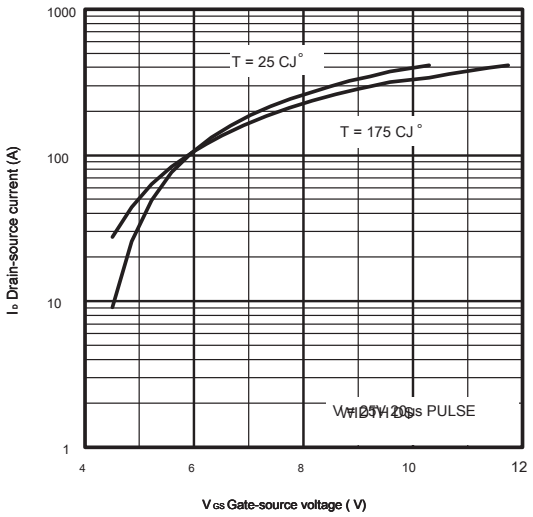


Fig 3. Change characteristics

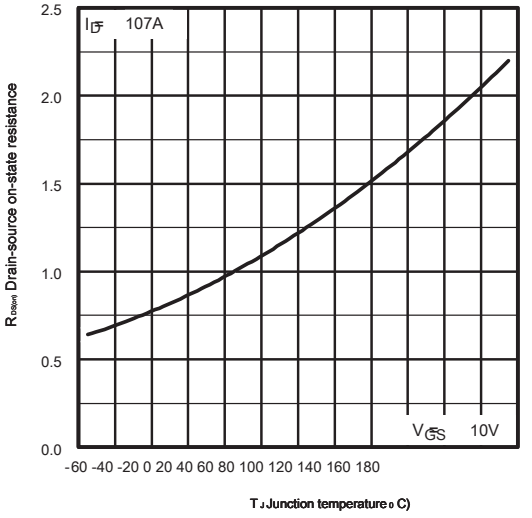


Fig 4. On-state resistance vs. temperature

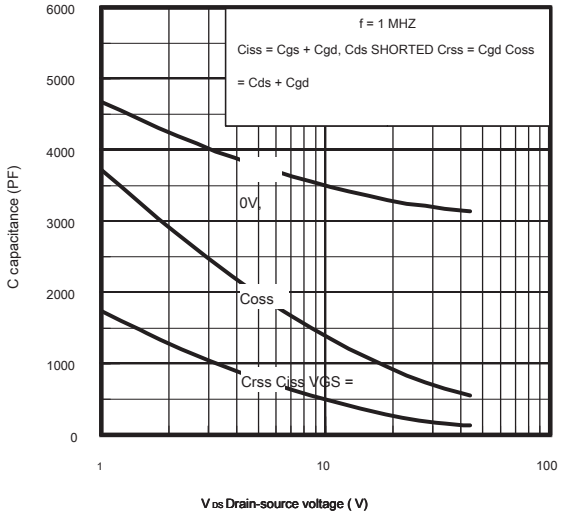


Fig 5. Relationship between capacitance and drain-source voltage

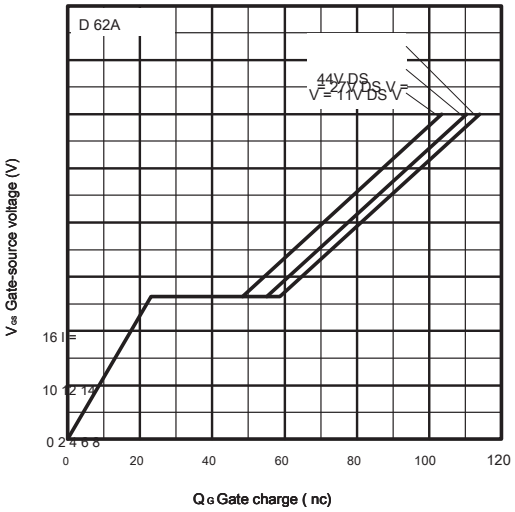


Fig 6. Gate charge vs. gate-source voltage

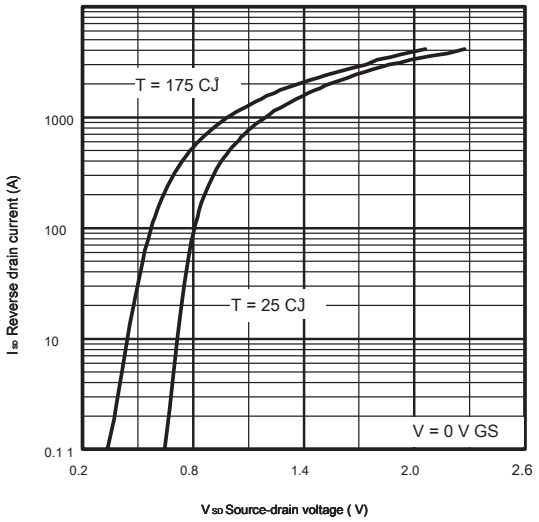


Fig 7. Source-drain diode forward characteristics

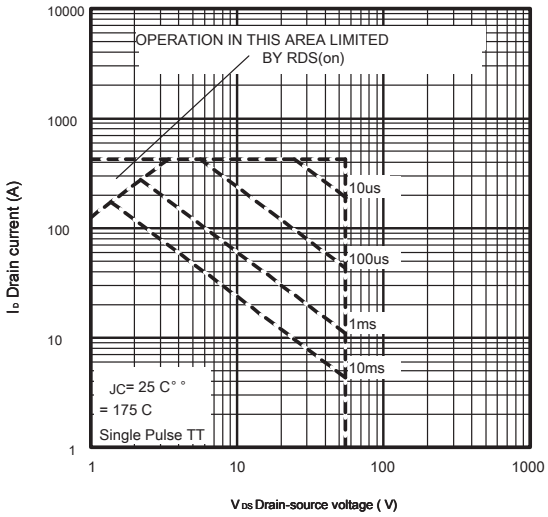


Fig 8. Maximum safe use range

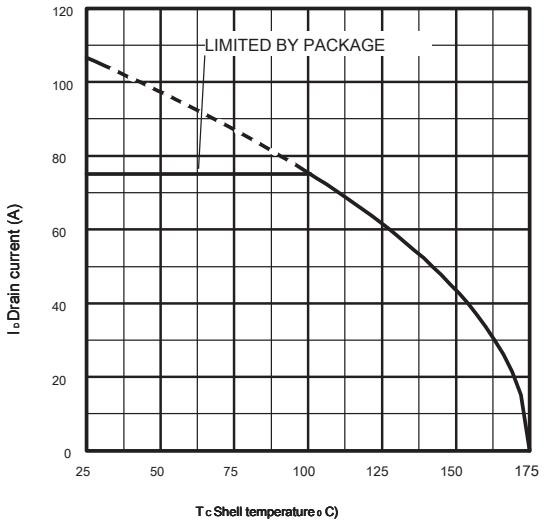


Fig 9. Relationship between maximum drain capacitance and case temperature

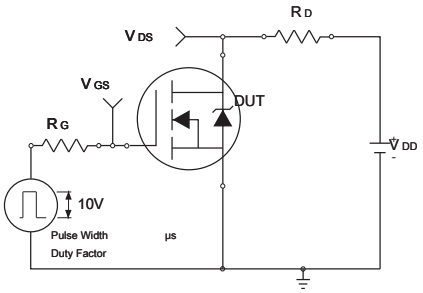


Fig 10a. Switch test circuit

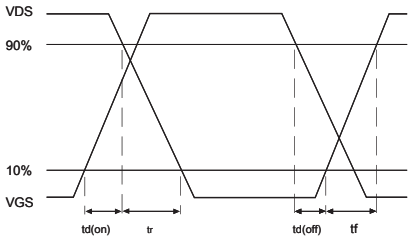


Fig 10b. Switching time waveform

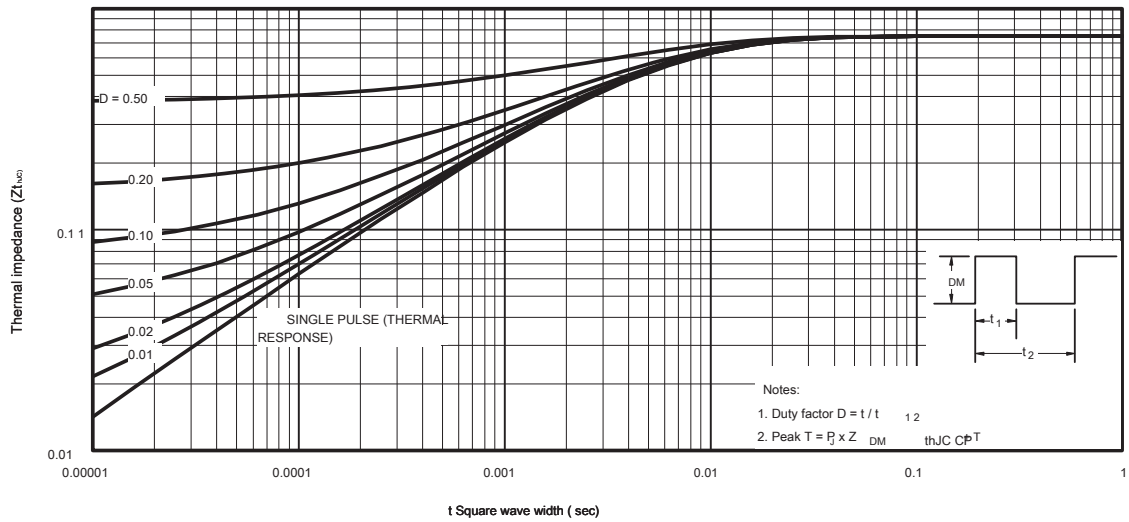


Fig 11. Maximum thermal impedance change

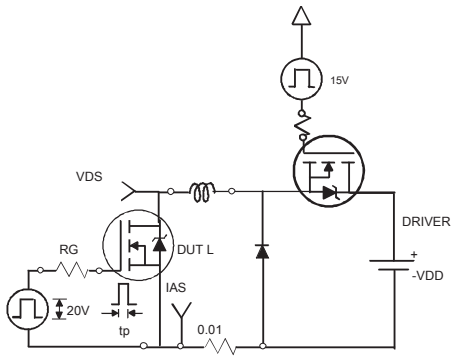


Fig 12a. Unlimited inductance test circuit

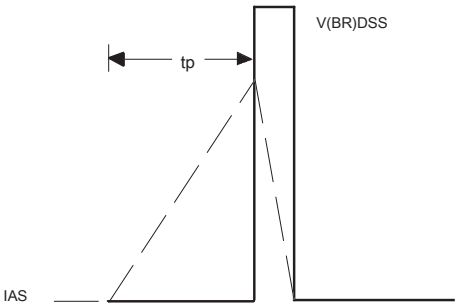


Fig 12b. Test waveform

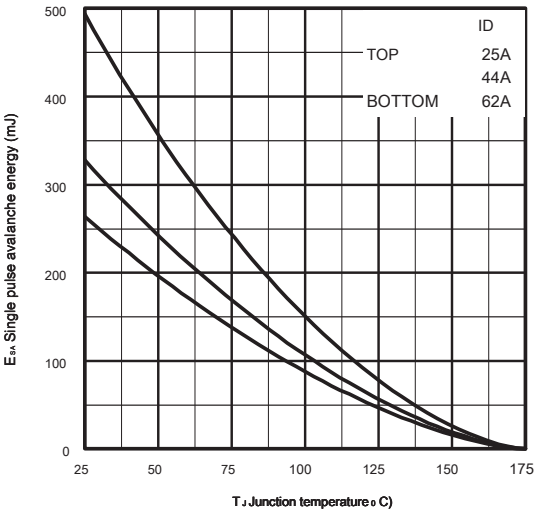


Fig 12c. Relationship between maximum avalanche energy and drain current

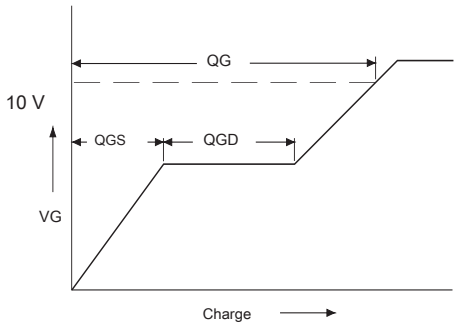


Fig 13a. Gate charge curve

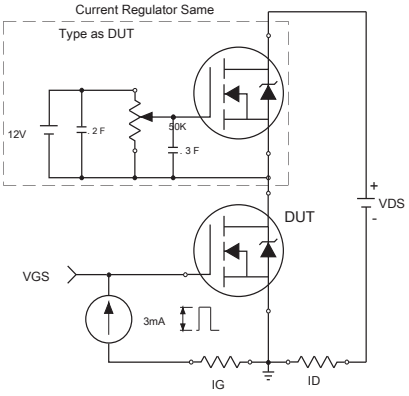
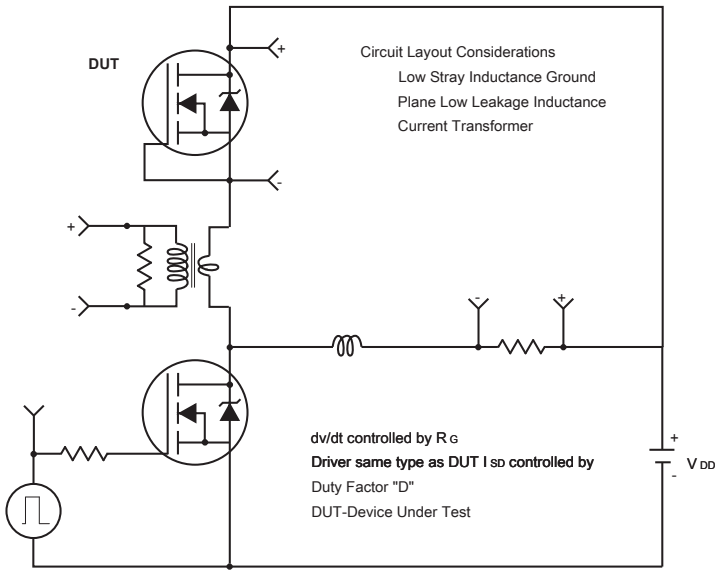
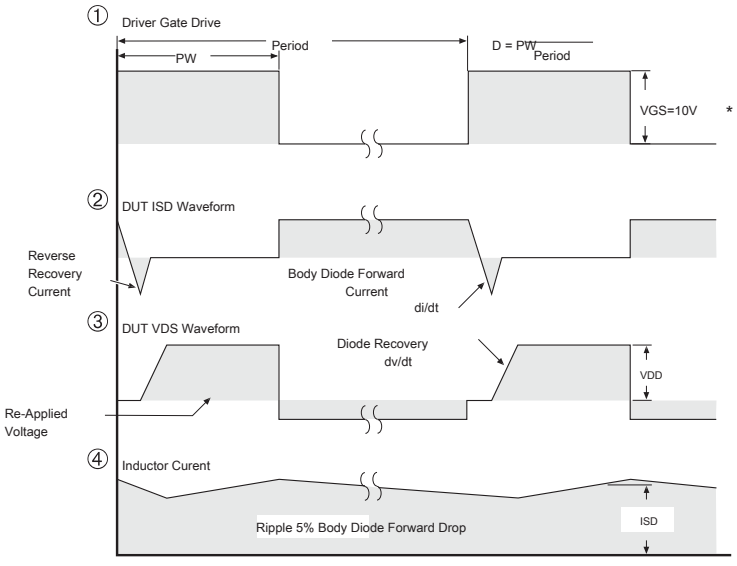


Fig 13b. Gate charge test circuit

Diode reverse recovery characteristics dv/dt Test circuit



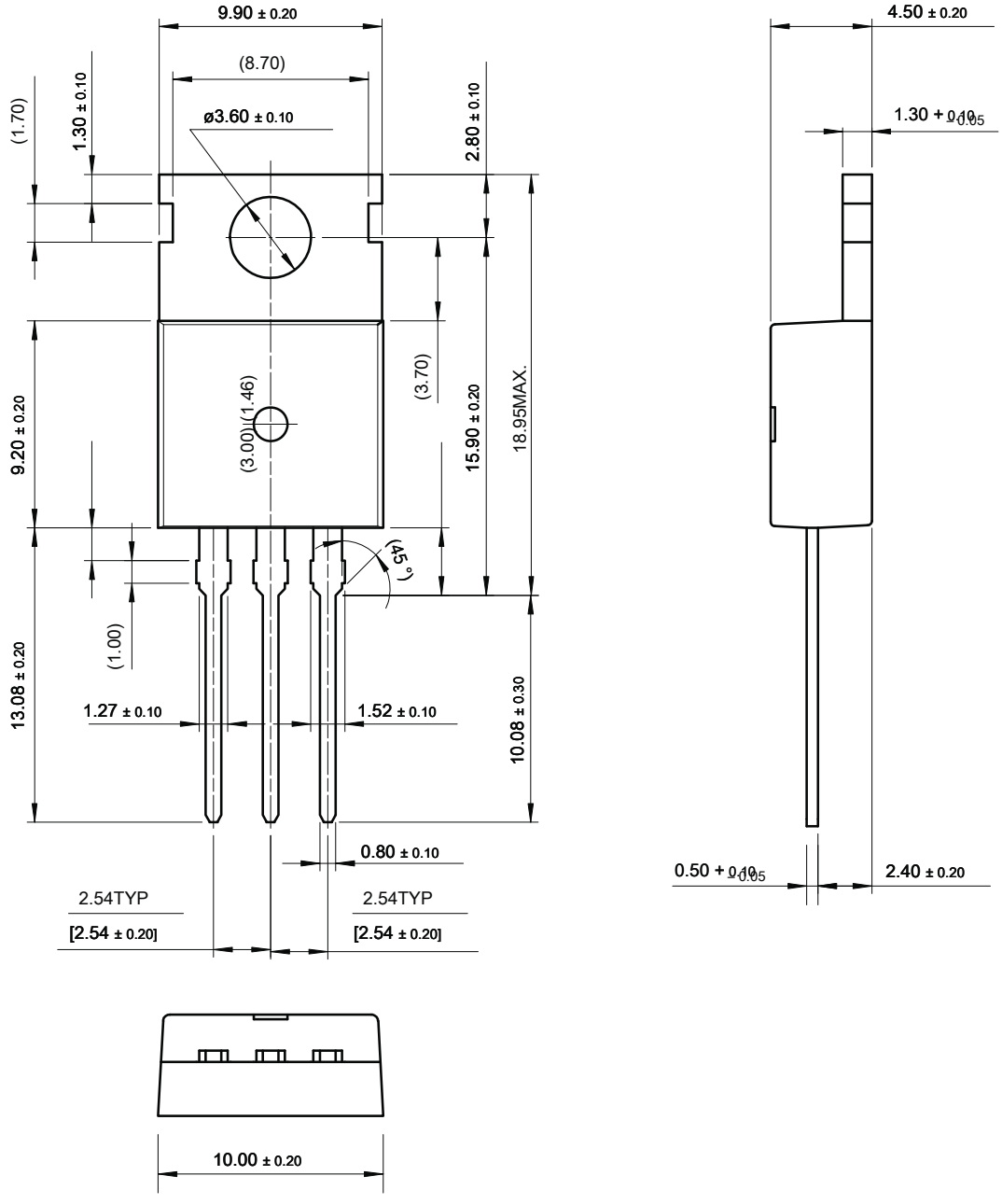


* V GS = 5V for Logic Level Devices R G

Fig 14. Test waveform

Dimensions

3 ???



Dimensions: mm