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# SSI 32P3015/3016
## Pulse Detector with Programmable Filter

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## DESCRIPTION

The SSI 32P3015/3016 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 72 Mbit/s.

The SSI 32P3015/3016 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed. The 32P3016 also has a level pin output.

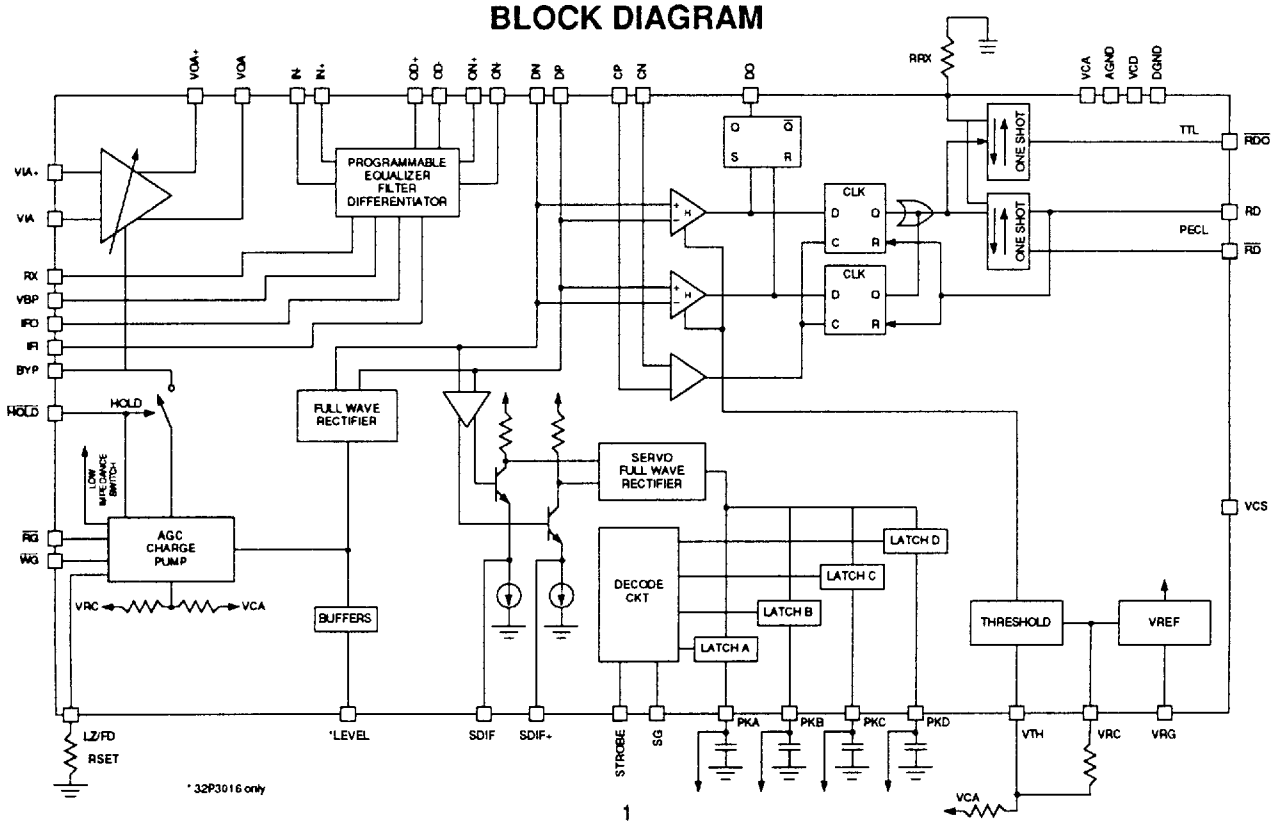
Ideal for constant density recording applications, the SSI 32P3015/3016 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3015/3016 requires only a +5V supply voltage and are available in a 48-lead TQFP package. The 32P3015 is also available in a 44-lead SOM package.

## FEATURES

- **Compatible with 72 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC Input Impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.5 ns filter group delay variation from 0.3 FC to FC = 27 MHz**
- **Independent positive and negative threshold qualification to suppress error propagation**
- **0.5 ns max pulse pairing**
- **Servo differentiator and 4-burst servo capture**
- **+5V only operation**
- **48-lead TQFP package, 44-lead SOM 32P3015 only**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The SSI 32P3015/3016 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 72 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

### MODES OF OPERATION

The SSI 32P3015/3016 can operate in one of three modes as controlled by $\overline{RG}$, $\overline{WG}$, and SG.

**Normal Read Mode** $\overline{RG}$ = 0, $\overline{WG}$ = 1, SG = X

In the normal read mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the $\overline{RD}$ and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

**Servo Read Mode** $\overline{RG}$ = 1, $\overline{WG}$ = 1, SG = 1

In the servo read mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

**Write Mode** $\overline{RG}$ = X, $\overline{WG}$ = 0, SG =X

In the write mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

### AGC AMPLIFIER

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}]$$ (See note 2)

### AGC ACTIONS

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal read and servo read mode

($\overline{RG}$ = X, $\overline{WG}$ = 1) SG = X

**Slow Decay:** When the DP/DN signal is below 1 Vppd, a slow decay current, ID, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. ID = 0.0075 x IFI. At T = 27°C, the maximum ID is 4.5 µA when the filter cutoff frequency is 27 MHz.

**Slow Attack:** When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, ICH, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

**Fast Attack:** When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, ICHF, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo read mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3015/3016 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write mode ($\overline{RG}$ = X, $\overline{WG}$ = 0) SG = X

In the write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo tead mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. A0 = 11, K = 0.22, VR = 3.6.

### Write-to-Read Transition
### ($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1) SG = X

When the SSI 32P3015/3016 switches from the write to read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period. For the next time period, the device then enters either the fast decay or attack mode depending on the signal level at the DP/DN pins. The time period, t, is determined by an external resistor, RT, from the LZ/FD pin to ground. For the low impedance:

$$TLZ(\mu s) = \frac{RT(k\Omega)}{78} - 0.26$$

and for fast decay:

$$TFD(\mu s) = \frac{RT(k\Omega)}{37} - 0.85$$

## PROGRAMMABLE FILTER

The SSI 32P3015/3016 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, $fc$, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{ at } T = 27°C$$

IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The $fc$ is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$\text{Boost (dB)} = 20 \log_{10}[(\frac{Kb \cdot VBP}{VRG}) + 1]$$

$$Kb = 3.225 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

When DACs are used, the boost relation then reduces to:

$$\text{Boost (dB)} = 20 \log_{10}[(Kb \cdot \frac{S\_Code}{127}) + 1]$$

## PULSE QUALIFICATION

The SSI 32P3015/3016 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

### Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

## FUNCTIONAL DESCRIPTION (continued)

The SSI 32P3015/3016 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3015/3016 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and can be calculated by the equation below:

PWRD (ns) = 1.33 RRX (kΩ) + 0.9879

$\overline{RDO}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the $\overline{RDO}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot can be calculated by the following equation PWRDO (ns) = 2.715 RRX (kΩ). DO output is a test point used to monitor the outputs of the internal comparators. It is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

The 32P3016 has a level output which is an amplified peak capture of DP-DN. It can be computed as level gain x DP - DN Vppd + VRC.

### Four-Burst Servo Differentiator and Capture

The SSI 32P3015/3016 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output.

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{1190Cs}{LCs^2 + (R + 48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$

$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with little or no offset common to all four channels.

GTA, GTB, GTC, and GTD are now generated on-chip, using STROBE and SG as inputs. N.B.: There must be exactly 4 strobe pulses withing the TRUE time of SG.

A two-bit counter and 4 gates produce:

GTA from the first STROBE pulse,

GTB from the second STROBE pulse,

GTC from the third STROBE pulse,

GTD from the fourth STROBE pulse.

Resetting of PKA, PKB, PKC, and PKD must still be done externally.

VCS Pin: This is a third +5V pin, intended not to be switched off by the customer in order to power down.

VCS is used as the high-voltage tie point for the ESD diodes from the 5 TTL-level input pins:

1) STROBE
2) SG
3) $\overline{RG}$
4) $\overline{WG}$
5) $\overline{HOLD}$

The purpose of this is to make it impossible for one or more of the TTL-level input drives to attempt to support the chip, via ESD diodes, when VCC and VCD are switched off.

VCS also supports the held servo voltages at pins PKA, PKB, PKC, and PKD. This is done by using VCN as the +5V supply for SSIN, PKCTRLN (via VPB), and LSERVO.

RRX Pin: This pin connects to an external precision, low T-C resistor, which is used to set the discharge currents of the one-shots, OSE_A and OSE_B, which in turn determine the pulse widths of the TTL ouput pulse, $\overline{RDO}$, and of the ECL ouput pulses, RD and $\overline{RD}$. This permits adjustment of the pulse widths for different applications and/or for variations in on-chip capacitances, and reduces the pulse-width changes caused by "corner" conditions.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

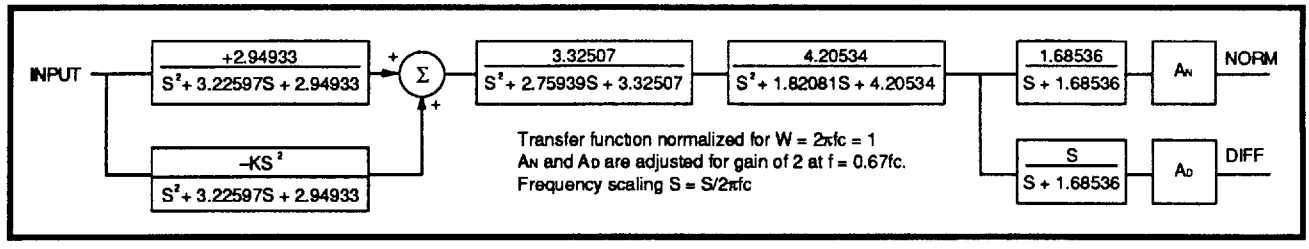



**FIGURE 1: Bessel Filter Transfer Function**

**TABLE 1: Typical Change in $f$ - 3 dB Point with Boost - $K = 2.94933\,(10^{\frac{BOOST\,(dB)}{20}} - 1)$**

| Boost (dB) | Gain@$fc$ (dB) | Gain@peak (dB) | $f$Peak/$fc$ | $f$-3dB/$fc$ | K |
|---|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 | 0 |
| 1 | -2 | 0.00 | no peak | 1.20 | 0.36 |
| 2 | -1 | 0.00 | no peak | 1.47 | 0.76 |
| 3 | 0 | 0.15 | 0.62 | 1.74 | 1.22 |
| 4 | 1 | 1.00 | 1.08 | 1.96 | 1.73 |
| 5 | 2 | 2.12 | 1.24 | 2.13 | 2.30 |
| 6 | 3 | 3.35 | 1.24 | 2.28 | 2.94 |
| 7 | 4 | 4.56 | 1.39 | 2.42 | 3.65 |
| 8 | 5 | 5.82 | 1.39 | 2.54 | 4.46 |
| 9 | 6 | 7.04 | 1.39 | 2.66 | 5.36 |
| 10 | 7 | 8.24 | 1.39 | 2.77 | 6.38 |
| 11 | 8 | 9.41 | 1.39 | 2.88 | 7.52 |
| 12 | 9 | 10.55 | 1.39 | 2.98 | 8.79 |
| 13 | 10 | 11.70 | 1.55 | 3.08 | 10.22 |

Notes: 1. $fc$ is the original programmed cutoff frequency with no boost.
2. $f$ - 3 dB is the new -3 dB value with boost implemented.
3. $f$peak is the frequency where the magnitude peaks with boost implemented.

e.g., $fc$ = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then $f$ - 3 dB = 27.69 MHz
$f$peak = 16.12 MHz

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| STROBE | I | TTL input. Enables servo gate according to Figure 3. |
| $\overline{RG}$ | I | TTL compatible input. When low, the device is in normal read mode. |
| $\overline{WG}$ | I | TTL compatible input. When low, the device is in write mode. |
| SG | I | TTL compatible input. When high the corresponding servo gate channel is enabled. |
| $\overline{HOLD}$ | I | TTL compatible input. When low the AGC action is suspended. |

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO | O | ECL compatible data comparator latch output pin. |
| RD, $\overline{RD}$ | O | ECL compatible read data output pins. |
| $\overline{RDO}$ | O | TTL compatible read data output. |
| SDIF+, SDIF- | – | Pins for external differentiating network for servo data. |
| PKA, PKB, PKC, PKD | O | Open npn emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by STROBE and SG. |
| LEVEL | O | NPN emitter output that provides an amplified fullwave rectified signal of DP-DN (32P3016 only.) The signal is referenced to VRC. |

**ANALOG PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RRX | – | Pin to set, via external R, output pulse widths. |
| VRC | – | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | – | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | – | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | – | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | – | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | – | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| LZ/FD | – | Pin for external resistor to set timing for both Low-Z input and fast decay modes. |
| BYP | – | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD, VCS | – | Analog, Digital, and Servo +5V |
| AGND, DGND | – | Analog and Digital grounds. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | | RATING |
|---|---|---|
| Storage Temperature | | -65 to +150°C |
| Junction Operating Temperature | Tj | +130°C |
| Supply Voltage | VCA, VCD | -0.7 to 7V |
| Voltage Applied to Inputs | | -0.7 to VCA, VCD V and VCS |

**RECOMMENDED OPERATING CONDITIONS**

| | | |
|---|---|---|
| Supply Voltage, VCS = VCA = VCD = VCC | | 4.5V < VCC < 5.5V |
| Ambient Temperature | Ta | 0°C<Ta<70°C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| PD | Power Dissipation | Outputs unloaded<br>4.5V < VCA, VCD < 5.5V | | 490 | 600 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| TTL Input Low Voltage | VIL | | -0.3 | | 0.8 | V |
| TTL Input High Voltage | VIH | | 2.0 | | VCC +0.3 | V |
| TTL Input Low Current | IIL | VIL = 0.4V | -0.4 | | | mA |
| TTL Input High Current | IIH | VIH = 2.7V | | | 0.1 | mA |
| PECL Output High Voltage | VOH | VCC = 5V | VCC -1.02 | | VCC-0.4 | V |
| PECL Differential Output Swing | VOE | VCC = 5V | 0.3 | | 0.6 | V |
| PECL Output Rise and Fall Time | TRF | CL ≤ 10 pF | | | 3.5 | ns |
| Control Input Switching Times | TS | | | | 0.1 | µs |
| TTL Output Low Voltage | VOLT | IOL = 4 mA | | | 0.5 | V |
| TTL Output High Voltage | VOHT | IOH = -400 µA | 2.4 | | | V |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca = 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input Range | VIR | Filter boost at $fc$ = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at $fc$ = 11 dB | 20 | | 100 | mVppd |
| DP-DN Voltage | VD | VIA± = 0.1 Vppd | 0.90 | | 1.10 | Vppd |
| DP-DN Voltage Variation | VDV | 24 mV < VIA± < 240 mV | | | 8.0 | % |
| Gain Range | AV | | 1.9 | | 30 | V/V |
| Gain Sensitivity w.r.t. BYP Voltage | AVPV | | | 50 | | dB/V |
| VOA+ VOA- Dynamic Range | DR | THD = 1% max, Vin = 24 mVpp<br>THD = 2% max, Vin = 240 mVpp | 0.75 | | | Vppd |
| Differential Input Impedance | RINDA | $\overline{WG}$ = 1 | 4.7 | 5.8 | 8.4 | kΩ |
| | | $\overline{WG}$ = 0 | | 150 | | Ω |
| Single Ended Input Impedance | RINSA | $\overline{WG}$ = 1 | | 3 | | kΩ |
| | | $\overline{WG}$ = 0 | | 95 | | Ω |
| Differential Output Offset Variation | VOS | from min. gain to max. gain | -200 | | +200 | mV |
| Input Referred Noise Voltage | VIN | gain = max, Rs = 0Ω<br>filter not connected to<br>VOA+ and VOA-, BW = 15 MHz | | 9.5 | 15 | nV/√Hz |
| Bandwidth | BW | No AGC action, Gain = max | 55 | 81 | | MHz |
| Common Mode Rejection Ratio | CMRR | gain = max, Vin = 0 VDC +<br>100 mVpp @ 5 MHz | 40 | | | dB |
| Power Supply Rejection Ratio | PSRR | gain = max, 100 mVpp on VCA,<br>VCD @ 5 MHz | 45 | | | dB |
| Gain Decay Time | GDT | VIA± = 240 mV to 120 mV<br>VOA± < 0.9 Final Value<br>IFI = 600 µA | | 48 | | µs |
| Gain Attack Time | GAT | VIA± = 120 mV to 240 mV<br>VOA± < 1.1 Final Value<br>IFI = 600 µA | | 1.8 | | µs |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. 110 µA<IFI<600 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Discharge Current | ID | $\overline{WG}$ = 1, DP - DN = 0V | | 0.0075 x IFI | | A |
| Fast Discharge Current | IDF | | | 20 x ID | | A |
| Charge Pump Attack Current | ICH | $\overline{WG}$ = 1, DP - DN = 0.55V | | 40 x ID | | A |
| Charge Pump Fast Attack Current, Ichf | ICHF | $\overline{WG}$ = 1, DP - DN = 0.675V | | 9 x ICH | | A |
| BYP Pin Leakage Current | IK | $\overline{WG}$ or $\overline{HOLD}$ = 0<br>VBYP = VCC -1.5V | -0.1 | | +0.1 | µA |
| VRC Reference Voltage | VRC | | | VCA -VRG | | V |
| VRC Output Drive | IVRC | | -0.75 | | +0.75 | mA |
| VRG Reference Voltage | VRG | Isource 0 to 1 mA | 2.2 | | 2.45 | V |
| Low-Z Timing Accuracy | TLZ | TLZ = RT/78 - 0.26<br>RT> 45 kΩ | -30 | | +30 | % |
| Fast Decay Timing Accuracy | TLD | TFD = RT(kΩ)/37 -0.85<br>RT> 45 kΩ | -30 | | +30 | % |

### EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| Filter Cutoff Frequency | *fc* | RX = 5 kΩ<br>*fc* = 27 x IFI/(4 x IFO ) MHz<br>4 ≥ IFO/IFI ≥ 4/3 | 9 | | 27 | MHz |
| IFO Reference Current | IFO | IFO = 0.75/RX; Tj = 27°C<br>5 kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| IFI Program Current Range | IFI | Tj = 27°C, 27 MHz > *fc* > 9 MHz | 0.2 | | 0.6 | mA |
| FCA Filter FC Accuracy | FCA | *fc* = 27 MHz | -13 | | 13 | % |
| RX Range | RX | | 1.25 | | 5 | kΩ |
| Normal Low Pass Gain AO = (ON ±) / (IN±) | AO | Fin = 0.67*fc* | 1.4 | | 2.2 | V/V |
| Differentiated Low Pass Gain AD = (OD ±) / (IN±) | AD | Fin = 0.67*fc* | 0.8 AO | | 1.2 AO | V/V |
| Frequency Boost Accuracy | FBA | VBP = VRG | -1.5 | | +1.5 | dB |
| | | VBP/VRG = 0.5 | -1.0 | | +1.0 | dB |
| Group Delay Variation | TGD1 | *fc* = 27 MHz, VBP = 0 to VRG<br>*fc* > Fin > 0.3 *fc* | -0.7 | | +0.7 | ns |

**EQUALIZER/FILTER** (continued)
The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | TGD2 | $fc$ = 9 to 27 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3 $fc$ | -2.5 | | +2.5 | % |
| | TGD3 | $fc$ = 9 to 27 MHz, VBP = 0 to VRG<br>$fc$ < Fin < 1.25 $fc$ | -4 | | +4 | % |
| Output Offset Voltage Variation | VOSVF | 200 µA ≤ IFI ≤ 600 µA | -200 | | 200 | mV |
| VOF Filter Output<br><br>Dynamic Range | DRF | THD = 2.0% max, ON ±<br>THD = 2.5% max, OD ±<br>Fin = 0.67 $fc$ | 1.2 | | | Vpp |
| Filter Input Resistance | RINF | | 3 | 4 | | kΩ |
| Filter Input Capacitance | CINF | | | | 7 | pF |
| Filter Output Resistance | ROF | IO+ = 1.0 mA | | | 60 | Ω |
| Filter Output Current | IOF | | -1 | | 1 | mA |
| Eout Output Noise Voltage; ON+, ON- | VNN | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 2.3 | 5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 4.8 | 8.5 | mVRms |
| Eout Output Noise Voltage; OD+, OD- | VND | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 4.3 | 7.5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 11.4 | 21 | mVRms |

**DATA COMPARATOR**
The input signals are AC coupled to DP and DN.

| | | | | | | |
|---|---|---|---|---|---|---|
| Differential Input Resistance | RIND | | 8 | | 14 | kΩ |
| Differential Input Capacitance | CIND | | | | 5 | pF |
| Comparator Offset Voltage | VOSD* | | | | 4 | mV |
| Level Output Gain | LG** | I (Level) = 50 µA,<br>DP-DN = 0.25 to 0.5 VDC<br>LG = $(V_{LEVEL} - V_{RC})/2(DP-DN)$ | 0.73 | | 0.81 | V/V |
| Level Output Bandwidth | LBW** | ±1 dB referenced to 1 MHz | 20 | | | MHz |
| Level Offset Voltage | VLOS** | Output - VRC, $I_L$ = 50 µA | -30 | | +30 | mV |
| Threshold Voltage Gain | HYS | VTH - VRC = 0.3V | 0.4 | | 0.52 | V/V |
| | | VTH-VRC = 0.9V | 0.42 | | 0.49 | V/V |

* Not externally measurable ** 32P3016 only

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### CLOCKING

The input signals are AC coupled to CP and CN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Threshold Voltage Hysteresis | VSH* | | | 0.20 x GHYS x (VTH -VRC) | | V/V |
| Propagation Delay | TPDD | To DO | | 4.5 | | ns |
| VTH Input Bias Current | IVTH | | | | 2 | µA |
| Comparator Offset Voltage | VOSC | | | | 4 | mV |
| Differential Input Resistance | RINC | | 8 | | 14 | kΩ |
| Differential Input Capacitance | CINC | | | | 5 | pF |
| D Flip-Flop Set Up Time | TDS | DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz | | | 1 | ns |
| Pulse Pairing | PP | CP-CN = I Vppd square wave, F = 10 MHz | | | 0.5 | ns |
| Propagation Delay from CP-CN zero crossing to RD | TPDC | Vs = 20 mVpp square wave | | 9 | | ns |
| RD Output Pulse Width | PWRD | PWRD (ns) = 1.33 RRX (kΩ) + 0.9879 (RRX ≥ 4.5 kΩ, CL = 10 pF) | -30 | | +30 | % |
| $\overline{RDO}$, TTL Output Pulse Width | PWRDO | (RRX = 7.87 kΩ, CL = 10 pF) PWRDO (ns) = 2.715 RRX(kΩ) | -25 | | +25 | % |

### SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER

An external series network is connected between SDIF and SDIF to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

| | | | | | | |
|---|---|---|---|---|---|---|
| SDIF+ to SDIF- pin current | ISDIF | Differentiator impedance must be set so as not to dip the signal for this level | 1.4 | 2.0 | 2.6 | mA |
| Internal differentiator pull-up resistors | RDIF | Cannot be directly tested | 0.4 | 0.6 | 0.8 | kΩ |
| Input voltage range to maintain voltage gain | FWR | Cannot be directly tested | 0.1 | | 2.0 | Vppd FWR |

* Not externally measurable ** 32P3016 only

**SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER** (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rectification Error | RERR | | -10 | | +10 | % |
| FWR Voltage Gain from FWR Input to PKA-D Outputs | AFWR | 0.1 Vppd ≤ V(DP/DN) ≤ 1.0 Vppd<br>V(PKx) = 0.077 + 0.96V(DP/DN)<br>Fin = 4 MHz | -20 | | +20 | % |
| Servo Output Leakage Current | ISL | Channel disabled | | | 1 | µA |
| PKA-D Channel to Channel Offset | VCOS | 1 Vppd input to servo FWR | -10 | | +10 | mV |
| PKA-D Absolute Offset | VAOS | 1 Vppd input to servo FWR | -20 | | 20 | mV |

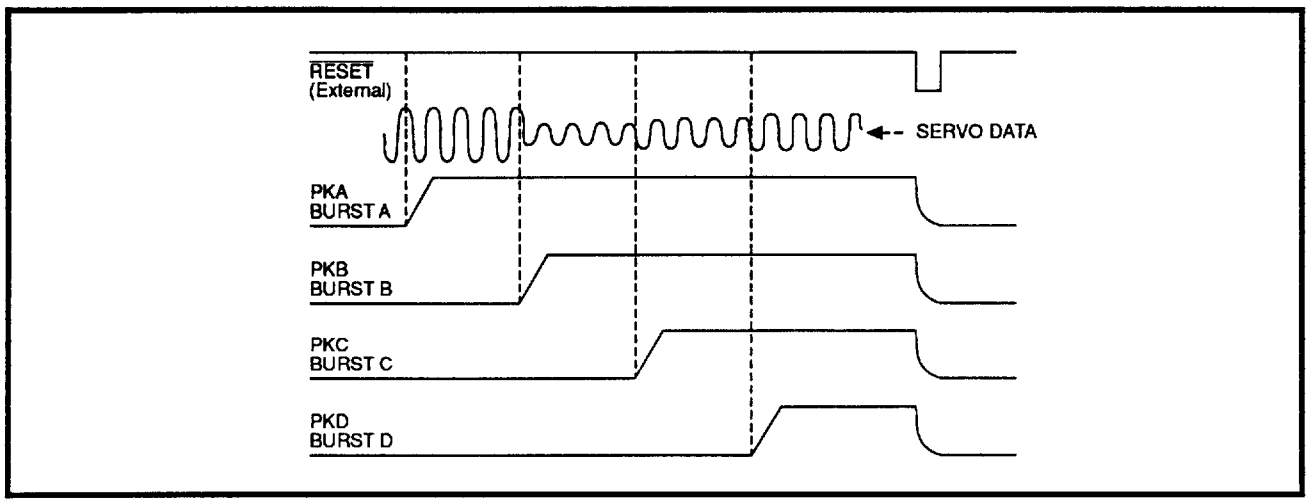



**FIGURE 2: Servo Gate Timing**

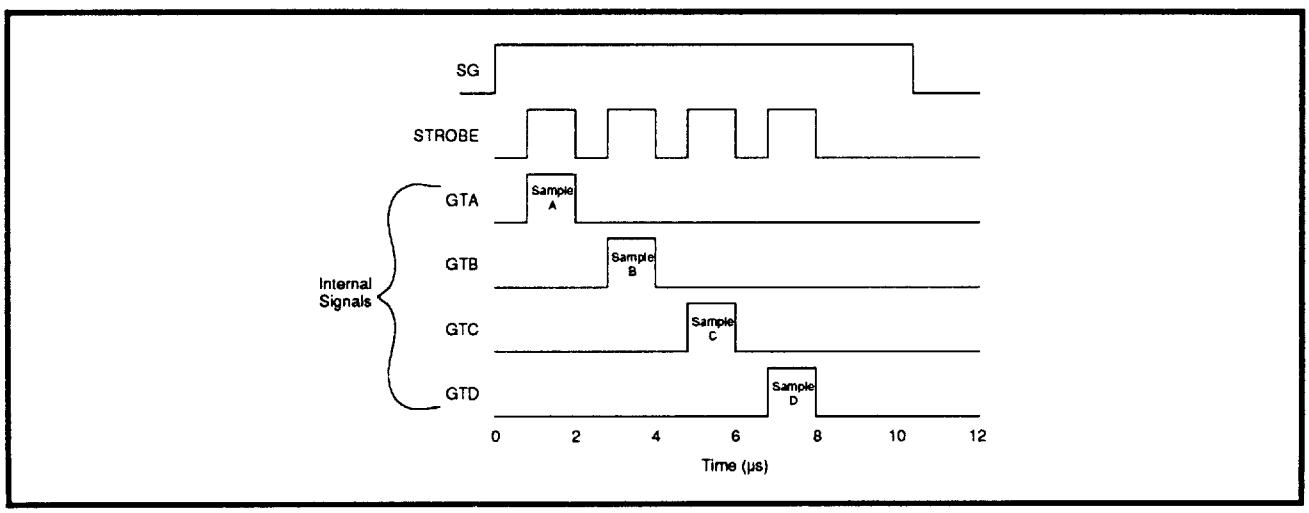
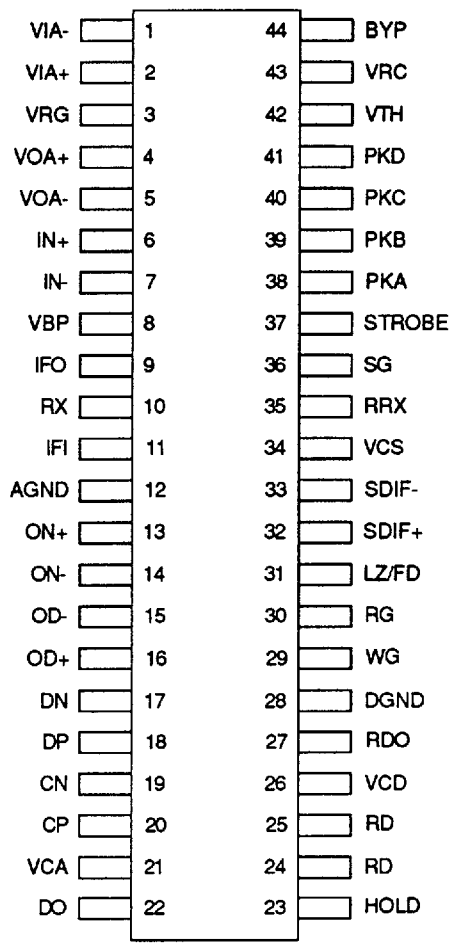



**FIGURE 3: Servo Capture Timing**

## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 44-Lead SOM | 70°C/W |

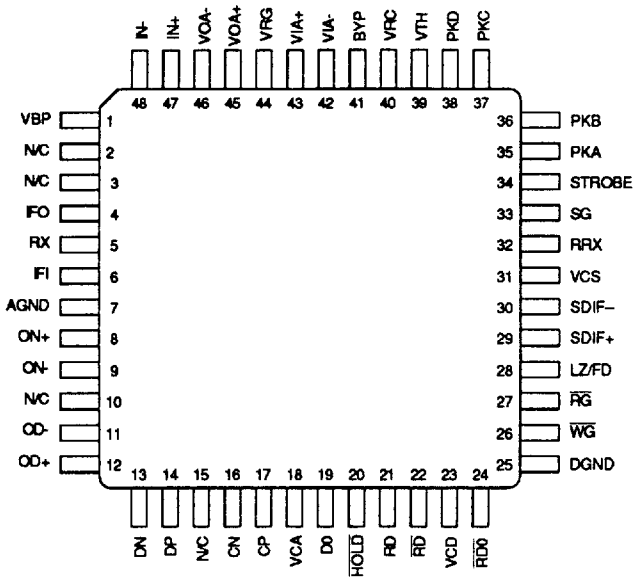



**44-Lead SOM**
**SSI 32P3015 only**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32P3015/3016
# Pulse Detector with Programmable Filter

## PACKAGE PIN DESIGNATIONS
(Top View)



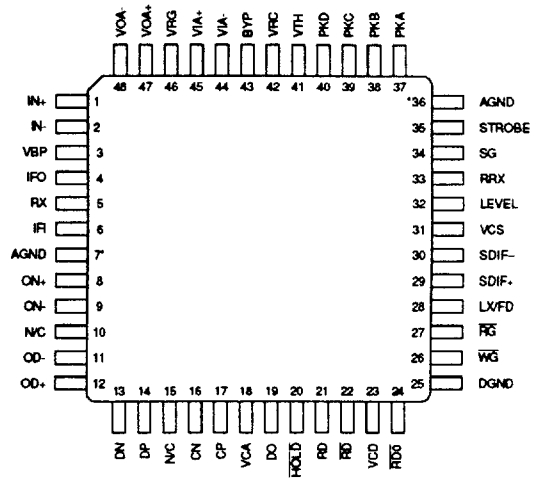

**SSI 32P3015**
**48-Lead TQFP**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 48-Lead TQFP | 81°C/W |

**THERMAL CHARACTERISTICS: θjc**

| | |
|---|---|
| 48-Lead TQFP | 28°C/W |




**SSI 32P3016**
**48-Lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

*Both Pin 7 and Pin 36 of the 32P3016 must be connected to PCB analog ground. Pin 36 is not connected to the chip's circuits. It is used as an electrostatic shield.

## ORDERING INFORMATION

| PART DESCRIPTION | | ORDER NUMBER | PACKAGE MARK |
|---|---|---|---|
| SSI 32P3015 | | | |
| | 44-Lead SOM | 32P3015-CM | 32P3015-CM |
| | 48-Lead TQFP | 32P3015-CGT | 32P3015-CGT |
| SSI 32P3016 | | | |
| | 48-Lead TQFP | 32P3016-CGT | 32P3016-CGT |



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