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SSI 32P4904
PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

May 1996

DESCRIPTION

The SSI 32P4904 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 24 to 80 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and FWR servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V power supply.

The SSI 32P4904 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 24 to 80 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **3-tap transversal filter for adaptive PR4 equalization**
- **8/9 GCR ENDEC**
- **Data scrambler/descrambler**
- **Programmable write precompensation**
- **Low operating power (0.75W typical at 5V)**
- **Register programmable power management**
- **Presettable precoder state**
- **Register programmable WG polarity**
- **Dual bit and byte wide bi-directional NRZ data interfaces**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5V ±10%)**
- **Small footprint 100-Lead TQFP and 100-Lead QFP packages**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, analog during acquisition, sampled during read data**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents during read data**
- **Charge pump currents track programmable data rate**
- **Low drift AGC hold circuitry**
- **Low-Z input switch**
- **AGC hold, fast recovery, and AGC input impedance control signals**
- **Wide bandwidth, precision full-wave rectifier**

FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter provides:**
  - **Channel filter and pulse slimming equalization for equalization to PR4**
  - **Programmable cutoff frequency, 3 to 24 MHz**
  - **Programmable boost/equalization, 0 to 12.75 dB**
  - **±0.6 ns group delay variation from 0.2 fc to fc, with fc = 24 MHz**
  - **Minimizes size and power**
  - **Low-Z input switch**
- **3-tap self adapting transversal filter for fine equalization to PR4**
- **No external components required**

(continued)

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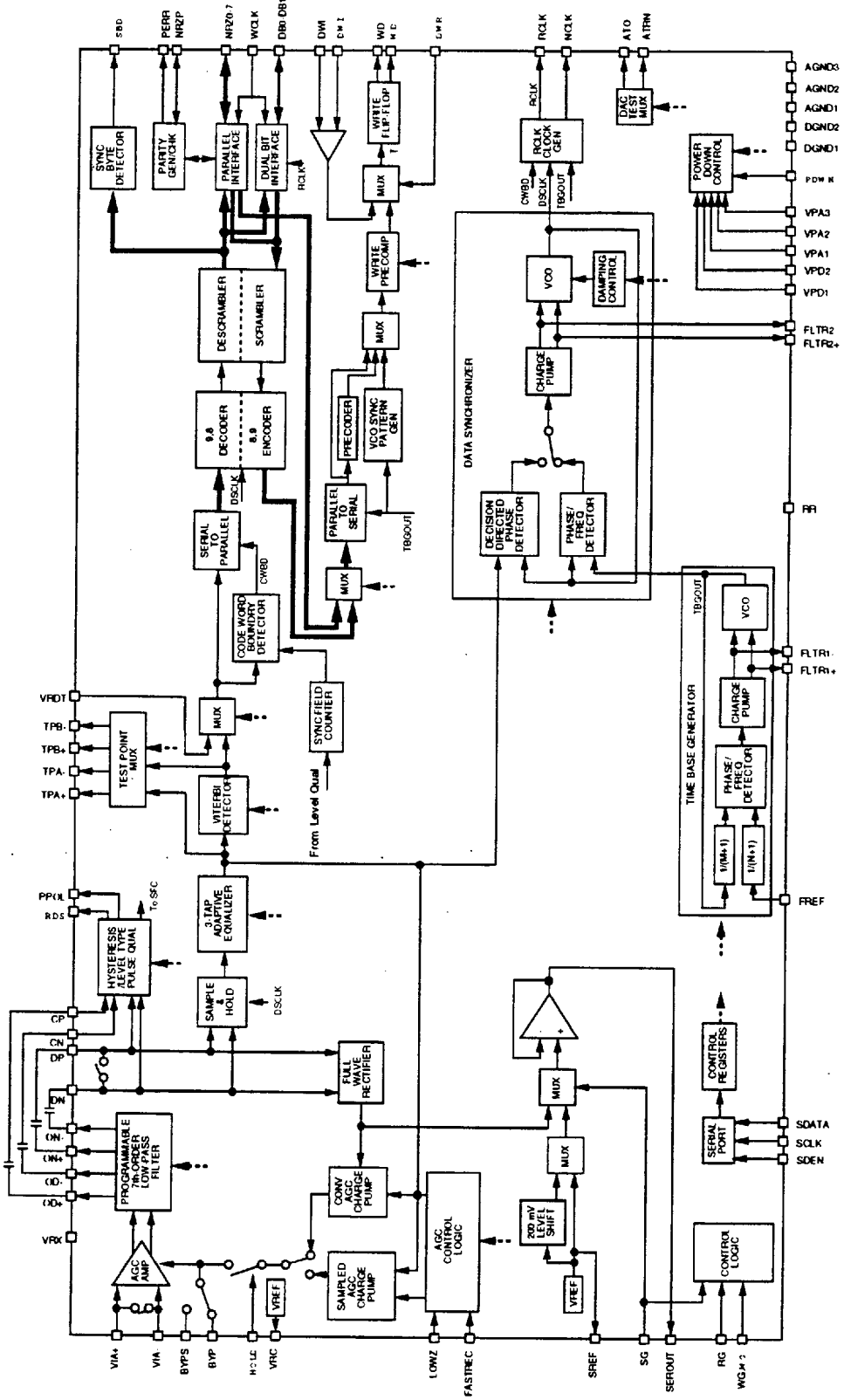
BLOCK DIAGRAM



FEATURES (continued)

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register selection between dual level pulse qualifier or hysteresis qualifier for servo reads

TIME BASE GENERATOR

- Less than 1% frequency resolution
- Up to 90 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 80 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive (+) and (-) clock recovery thresholds for use with asymmetrical amplitude signals (e.g. from MR heads)
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Dual bit and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection

SERVO

- Wide bandwidth, precision full-wave rectifier
- Buffered FWR analog servo output with selectable reference voltage
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Compatible with SSI 32H6521 Embedded Servo Controller

FUNCTIONAL DESCRIPTION

The SSI 32P4904 implements a complete high performance PR4 read channel, including an AGC, programmable filter/equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 8,9 ENDEC and scrambler/descrambler, and FWR servo, that supports data rates up to 80 Mbit/s.

A serial port is provided to write control data to the 16 internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input of the pulse detector while the input to the amplifier varies. The circuit consists of a loop that includes the AGC amplifier and charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. Depending on whether the read is of servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to noise.

During servo reads the loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (C_{BYPS}). The dual rate charge pump drives C_{BYPS} with currents that drive the differential voltage at DP/DN to 1.4 Vp-pd. Attack currents lower the V_{BYPS} which reduces the amplifier gain. The dual rate attack charge pump is included for fast transient recovery. The normal AGC attack current in servo mode is 150 µA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 8. The nominal decay current is 8.3 µA, and increases by a factor of 8 when the FASTREC input is high. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode.

AGC CIRCUIT DESCRIPTION (continued)

For data reads, the loop described above is used until the data synchronizer is locked to the incoming VCO preamble, except that to optimize recovery for constant density recording, both of the AGC charge pumps' currents track the data rate value loaded in the Data Rate Register and that the BYP hold capacitor (C_{BYP}) is now used. In addition, at the maximum data rate, the nominal AGC attack current is 360 µA and the nominal decay current is 20 µA. The fast attack and fast decay current factors are the same as in servo mode. After VCO lock (SFC), the loop is switched to include the AGC amplifier with a sampled dual rate charge pump, the programmable continuous time filter, full-wave rectifier, and the sampling 3-tap adaptive equalizer. This allows more accurate control of the signal amplitude into the Viterbi qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled and held and compared to a threshold to generate the error current. The maximum charge pump current value can be programmed from the Sample Loop Control Register to 0, 20, 40, or 60 µA.

For maximum application flexibility, all AGC mode control inputs are designed to be externally controlled. When the LOWZ input is high, Low-Z mode is activated. In the Low-Z mode, the AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. This mode should be activated during and for a short time after a write operation.

When the $\overline{\text{HOLD}}$ input is low, the dual rate attack charge pumps are disabled. This deactivates the AGC loop. The AGC amplifier gain will be held constant at a level set by the voltage at the BYP or BYPS pins.

In most applications, the BYP and BYPS pin voltages are stored on external capacitors. In applications where AGC action is not desired, the BYP and BYPS voltages can be set by resistor divider networks connected from VPA to VRC. If programmable gain is desired, the resistor network could be driven by a current DAC.

PULSE QUALIFICATION CIRCUIT DESCRIPTIONS

This device utilizes three different types of pulse qualification, two primarily for servo reads and the other for data reads.

Servo Qualifiers (Dual Level/Window & Hysteresis)

During servo reads (SG high) and when bit 6 of the Control Operating Register is set to 1, a dual level/ window type of pulse qualifier is used. The level qualification thresholds are set by a 7-bit DAC which is controlled by the Servo Level Threshold Register. The register value is relative to the peak voltage at the output of the continuous time filter, and the DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT Register does not affect this DAC's reference. The $\overline{\text{RDS}}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity of the pulse, respectively.

When bit 6 of the Control Operating Register is set to 0, a hysteresis type of pulse qualifier is used. The $\overline{\text{RDS}}$ output will recognize only alternating polarity qualified pulses. If a pulse exceeds the threshold and is of the same polarity of the previous qualified pulse, then it is ignored.

In data read mode (RG high), the same window mode qualifier is always used for ensuring pulse polarity changes during VCO sync field counting. It's qualification thresholds are set by a 7-bit DAC which is controlled by or the Data Level Threshold Register. The register value is relative to the peak voltage at output of the continuous time filter and the DAC is referenced to an fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT Register does not affect the DAC's reference until the sync field count has been achieved. The $\overline{\text{RDS}}$ and the PPOL outputs of the level qualifier are not active in data read mode.

Viterbi Qualifier

The second type of pulse qualification, the Viterbi qualifier, is only used during data read mode after the sync field count has been achieved. The Viterbi qualifier has two significant blocks, one that feeds the other. The first block is the sampled pulse detector and the second is the survival sequence register.

The sampled pulse detector performs the pulse acquisition/detection in the sampled domain. It acquires pulses by comparing the code clock sampled level of the analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The Viterbi threshold window is defined to be the difference between the positive and negative threshold levels. The threshold window, Vth, is set by a 7-bit DAC which is controlled by the Viterbi Detector Control Register. While the window size is fixed by the programmed Vth value, the actual positive and negative thresholds track the most positive and the most negative samples of the equalized input signal. For example, the Viterbi positive signal threshold, Vpt = Vpeak (+) max if the previous detected level was (+). If the previous detect level was (-), Vpt = Vpeak(-)max + Vth, where Vpeak(-)max is the maximum amplitude of the previously detected negative signal. Normally Vth is set to equal Vpeak (approx. 500 mV).

After the pulses have been detected they must be further qualified by the survival sequence registers and associated logic. This logic guarantees that for sequential pulses of the same polarity within the maximum run length, only the latest is qualified. By definition, this is the pulse of greatest amplitude.

The Viterbi qualifier is implemented as two parallel qualifiers that operate on interleaved samples. Each qualifier has a survival sequence register length of 5.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to 1.75 times the cutoff frequency. For pulse slimming two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. Both the boost and the filter cutoff frequency are programmed through internal 7-bit DACs, accessed via the serial port logic. The nominal boost range at the cutoff frequency is 0 to 12.75 dB at maximum fc and is controlled by the Data Boost Register or the Servo Boost Register in the servo mode. The cutoff frequency, fc is variable from 3 to 24 MHz and controlled by the Data Cutoff Register or Servo Cutoff Register in the servo mode. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The current reference for the filter DACs is set using a single 12.1 kΩ resistor, from the VRX pin to ground. The voltage at VRX is proportional-to-absolute-temperature (PTAT).

ADAPTIVE EQUALIZER CIRCUIT DESCRIPTION

Up to 7 dB of cosine equalization for fine shaping of the incoming read signal to the PR4 waveshape is provided by a 3-tap, sampled analog, transversal filter with an adaptive multiplier coefficient. The same multiplier coefficient (k_m) is used for both of the outside taps. The value of k_m is adjusted to force "zero" samples to zero volts. A special equalizer training pattern, located after the VCO sync field in the sector format, is used to provide an optimum signal for the equalizer to adapt to. The adaptive property of the equalizer is enabled or disabled by the AEE bit in the Sample Loop Register. If the adaptive property is enabled, whether adaptation occurs only during the training pattern or both during the training pattern and the user data is controlled by the AED bit in the Sample Loop Register.

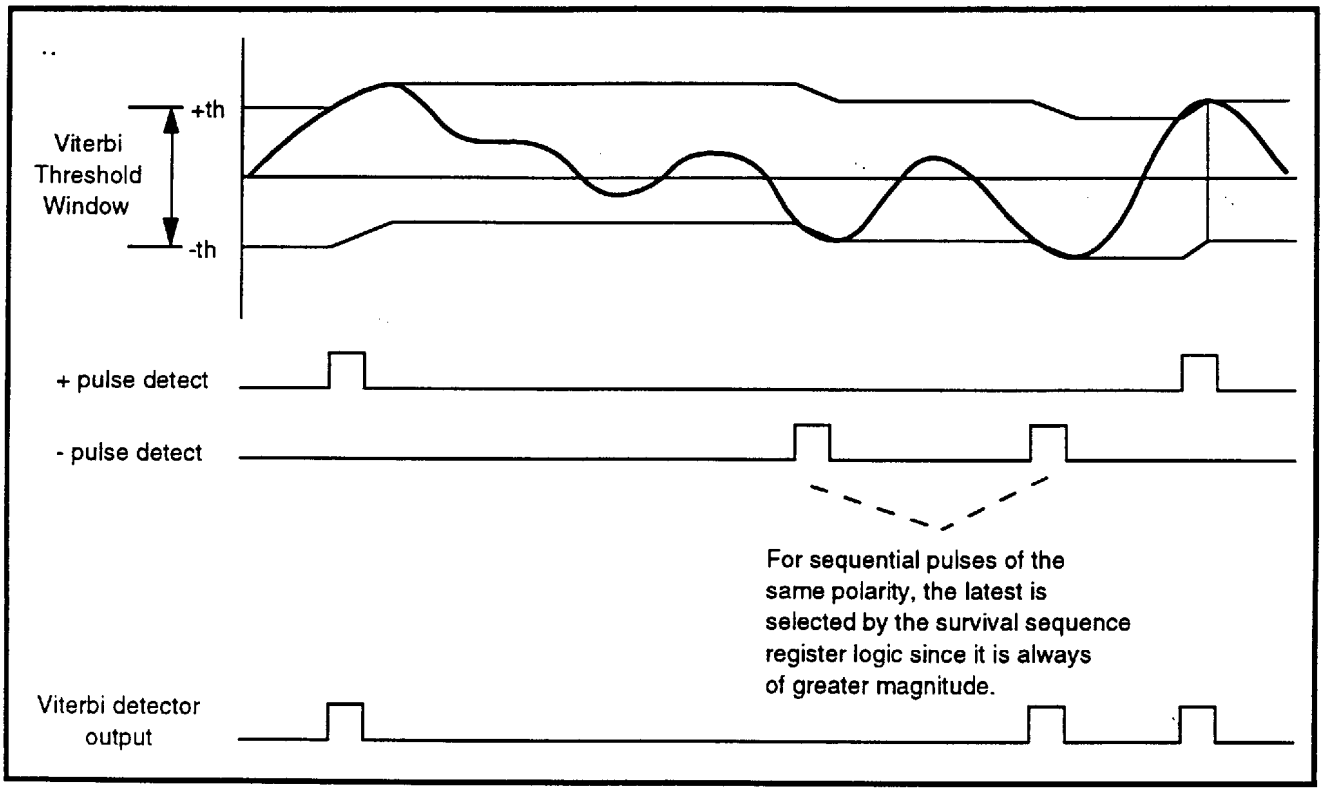


FIGURE 1: Viterbi Detection

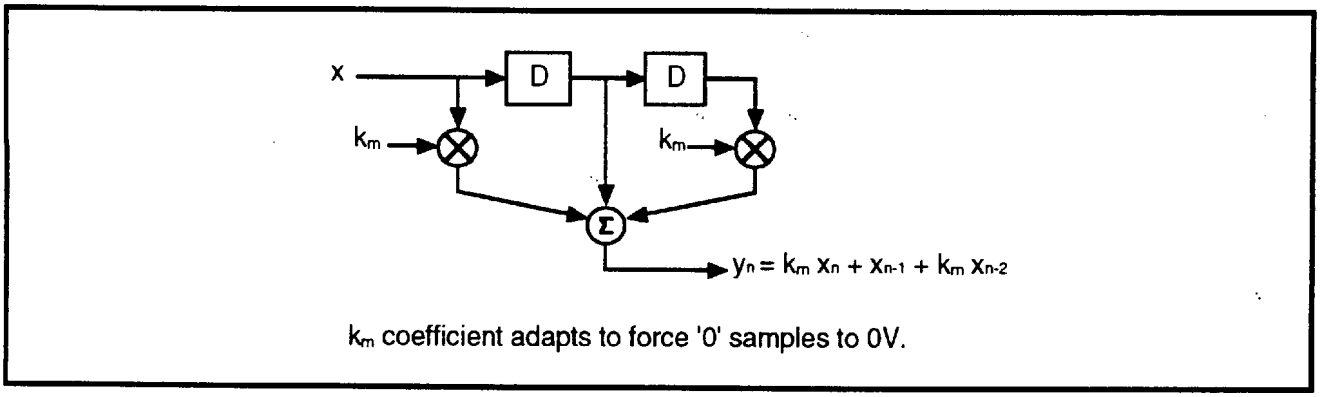


FIGURE 2: Block Diagram of 3-Tap Adaptive Equalizer

FUNCTIONAL DESCRIPTION (continued)

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator (TBG) is a PLL based circuit, that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N and DR Registers. The TBG output frequency, Fout, should be programmed as close as possible to ((9/8) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise.

In servo read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the write and idle modes, the time base generator output, when selected by the Control Test Mode Register, can be monitored at the TPA+ and TPA- test pins. In the read mode, the TBG output should not be selected for output on the test pins so that the possibility of jitter in the data separator PLL is minimized.

The reference frequency is programmed using the M and N Registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FTBG = FREF\ [(M + 1) \div (N + 1)]$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N Registers, only after the DR Register is updated.

The DR Register value, directly affects the following:

- center frequency of the time base generator VCO
- center frequency of the data separator VCO
- phase detector gain of the time base generator phase detector
- phase detector gain of the data separator phase detector
- write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the ground and RR pins.

$$RR = 12.1\ k\Omega$$

Note: SSI 32P4904 must have its VCO's trimmed for 80 Mbit/s

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for 8,9 (0,4,4) GCR data. In data read mode, the circuit performs address mark detect, clock recovery, code word synchronization, decoding, sync byte detection, descrambling, and NRZ interface conversion. In the write mode, the circuit generates address marks, generates the VCO sync field, scrambles and converts the NRZ data into 8,9 (0,4,4) GCR format, precodes the data, and performs write precompensation.

The circuit consists of five major functional blocks; the data synchronizer, 8,9 ENDEC, NRZ scrambler/descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

Data Synchronizer (continued)

In the read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent "one" samples or comparing the "zero" sample magnitude to ground for the entire sample period. A special (non IBM) algorithm is used to prevent "hang up" during the acquisition phase. The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, dual mode, threshold comparator. This comparator's threshold levels are determined by the value, Lth, programmed in the Data Threshold Register. The fixed level threshold before the sync field count (SFC) has been achieved will be 1.4 times the threshold level after SFC since this is the ratio of the peak signal to the sampled "1" signal amplitude for PR4. The dual mode nature of this comparator allows the selection of either symmetric fixed or independent self adapting (+) and (-) thresholds by programming the adaptive level enable (ALE) bit in the WP/LT Register.

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When adaptive mode is selected, the fixed thresholds are used until the sync field count (SFC) has been reached, then the adaptive levels are internally enabled. The time constant of a single-pole filter that controls the rate of adaptation, is programmable by bits TC3-1 in the WP/LT Register.

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, FTBG. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

The two phase detectors' outputs are muxed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6-0 in the Damping Ratio Control Register. The programmed damping ratio is independent of data rate.

In write mode, the TBG output is used to clock the encoder, precoder, and write precompensation circuits. The output of the precompensation circuit is then fed to the write data flip-flop which generates the write data (WD, $\overline{WD}$) outputs.

ENDEC

The ENDEC implements an 8,9 (0,4,4) group coded recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of four zeros between ones for the interleaved samples. During write operations the encoder portion of the ENDEC converts 8-bit parallel, scrambled or nonscrambled, data to 9-bit parallel code words that are then converted to serial format. In data read operation, after the code word boundary has been detected in the Viterbi qualified serial data stream, the data is converted to 9-bit parallel form and the decoder portion of the ENDEC converts the 9-bit code words to 8-bit NRZ format.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled by bit 2 of the Control Operating Register. In write mode, if enabled, the circuit scrambles the 8-bit internal NRZ data before passing it to the encoder. Only user data, i.e., the NRZ data following the sync byte, is scrambled. In data read mode, only the decoded NRZ data after the sync byte is descrambled. The scrambler polynomial is $H(X) = 1 \oplus X7 \oplus X10$.

NRZ Interface

The NRZ interface circuit provides the ability to interface with either a dual bit or byte wide controller. The NRZ interface type is specified by the programming of bit 4 of the Control Operating Register. If byte wide mode is selected, the circuit does not reformat the data before passing it to and from the internal 8-bit bus. If dual-bit mode is selected, the NRZ interface circuit converts the external dual-bit bus to the internal 8-bit bus. Only the selected NRZ interface is enabled and the other can be left floating. Both the byte wide and dual bit interfaces define the most significant bit of the interface as the most significant bit of the data and the dual bit interface defines the first pair clocked in or out as the most significant pair.

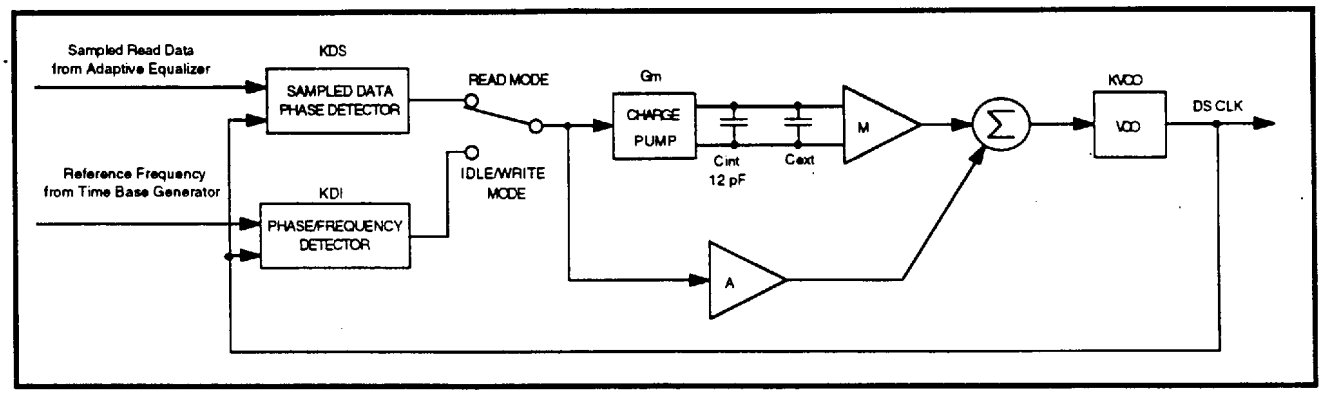


FIGURE 3: Data Synchronizer Phase Locked Loop

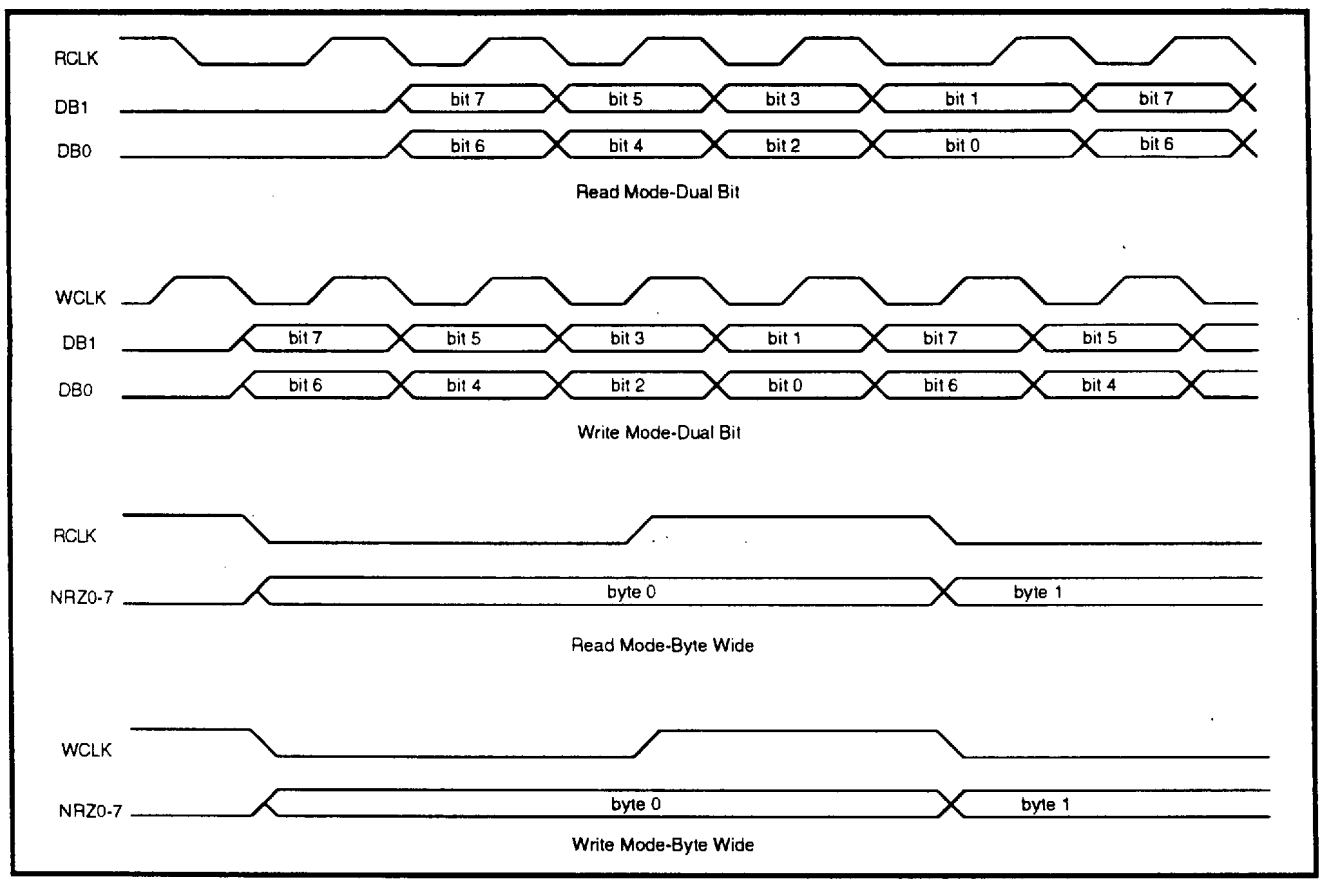


FIGURE 4: RCLK, WCLK vs. NRZ Data

NRZ Interface (continued)

For both byte wide and dual bit operation, the NRZ write data is latched by the SSI 32P4904 on the rising edge of the WCLK input. The WCLK frequency must be appropriate for the data rate chosen or else overflow/underflow will occur. It is recommended that WCLK be connected to RCLK to prevent this from occurring. In byte-wide mode, as each NRZ byte is input to the SSI 32P4904, its parity is checked against the controller supplied parity bit NRZP. If an error is detected, the PERR output pin goes high and remains high until WG goes low.

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte (96H). The NRZ interface is at a high impedance state when not in data read mode. In byte-wide mode, an even parity bit , NRZP, is generated for each output byte.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effect. The magnitude of the time shift, WPC, is programmable via the Write Precomp Register and is made proportional to the time base generator's VCO period (i.e., data rate). The circuit performs write precompensation only on the second of two consecutive "ones" and only shifts in the late direction. If more than two consecutive "ones" are written, all but the first are precompensated in the late direction.

SERVO CIRCUIT DESCRIPTION

Embedded servo capture is provided with a buffered full-wave rectified (FWR) output. The differential signal across the DP/DN inputs is applied to a full-wave rectifier. The output signal of the rectifier is the rectified servo burst signal, level-shifted above SREF (which is a bandgap reference from VPA). The output at the SEROUT pin is selectable between the FWR output and SREF. When the SG is high (active) the FWR output is selected for the SEROUT pin. When SG is low (i.e., during the data field) then the SEROUT pin is SREF.

The dual level pulse qualifier outputs $\overline{RDS}$ and PPOL are enabled when the servo gate input (SG) goes high and provide the indication of a qualified servo pulse and the polarity of the pulse, respectively.

SERIAL PORT CIRCUIT DESCRIPTION

The serial port interface is used to program the SSI 32P4904's sixteen internal registers. The serial port is enabled for data transfer when the serial data enable (SDEN) pin is high ("1"). SDEN must be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SDEN should be brought low ("0").

When SDEN is high, the data presented to the serial data (SDATA) pin will be latched into the SSI 32P4904 on each rising edge of the serial clock (SCLK). Rising edges of SCLK should only occur when the desired bit of address or data is being presented on the serial data line. Serial data transmissions must occur in 16-bit packets. During a serial data transmission, if SDEN is switched low before 16 SCLK pulses are received or if more than 16 SCLK pulses are received, that serial transmission will be aborted. For all valid transmissions, the data is latched into the internal register on the falling edge of SDEN.

Each 16-bit transmission consists of a R/$\overline{W}$ bit (R/$\overline{W}$ ="0") followed by 3 device select bits, 4 address bits and 8 data bits. The address bits select the internal register to be written to. The device select, address and data fields are input LSB first, MSB last, where LSB is defined as bit 0. The three device select bits select the device on the Silicon Systems serial bus to be communicated with and must set S0 = 0, S1 = 1, and S2 = 0 when communicating with the SSI 32P4904. Figure 7 shows the serial interface timing diagram.

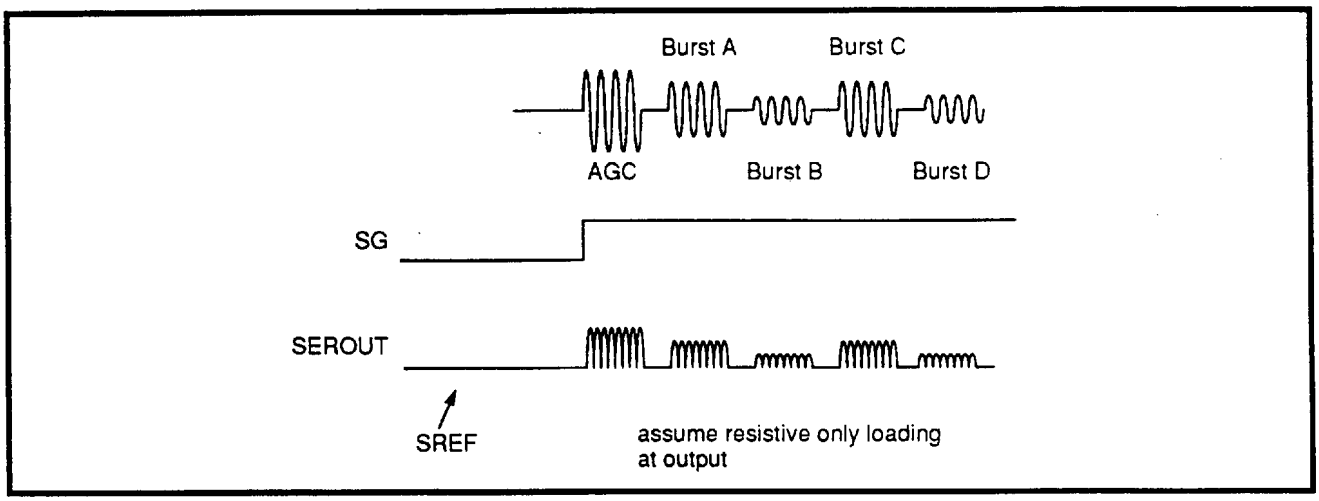


FIGURE 5: Servo Function Diagram

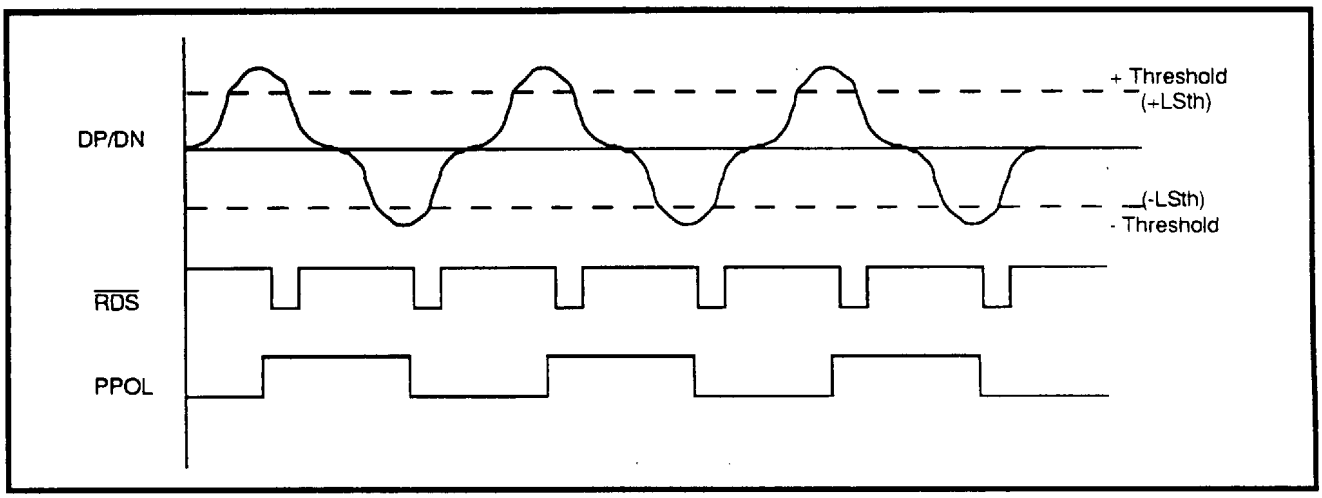


FIGURE 6: $\overline{RDS}$ and PPOL vs. DP/DN Relationship

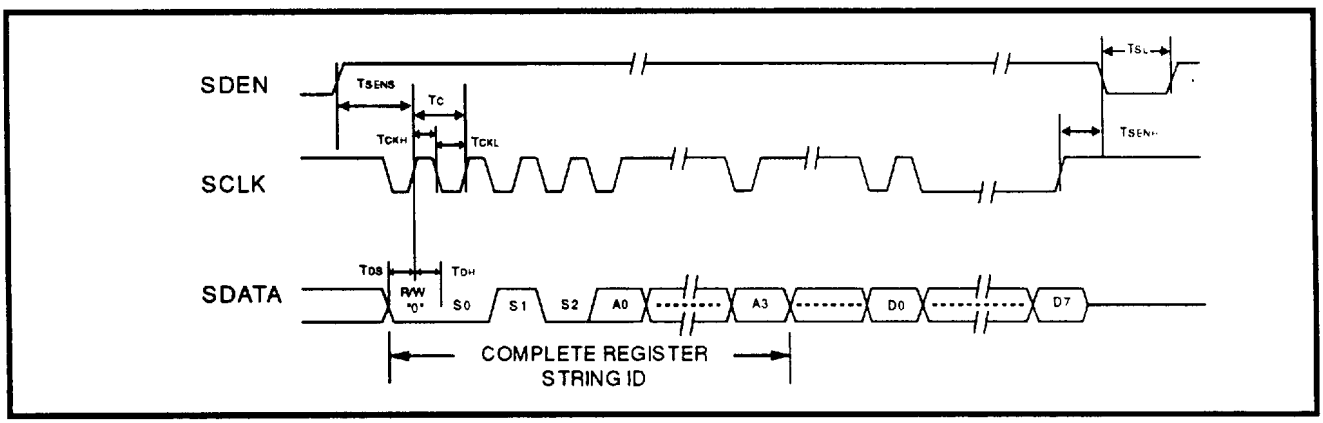


FIGURE 7: Serial Interface Timing

FUNCTIONAL DESCRIPTION (continued)

OPERATING MODES

The fundamental operating modes of the SSI 32P4904 are controlled by the servo gate (SG), read gate (RG), and write gate (WG/$\overline{WG}$) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in the idle mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data (WD/$\overline{WD}$) pulse.

IDLE MODE OPERATION

If SG, RG, and WG are not active, the SSI 32P4904 is in Idle mode. When in Idle mode, the time base generator and the data separator PLL are running and the data separator PLL is phase-frequency locked to the TBG VCO output. The AGC, continuous time filter, and pulse qualifiers are active but the outputs of the pulse qualifiers are disabled. The continuous time filter is using its programmed values for cutoff frequency and boost determined by the data mode registers. The AGC operation is the same as in the VCO preamble portion of a data read.

SERVO MODE OPERATION

If SG is high, the device is in the servo mode. This mode is the same as Idle except that the filter cutoff and boost settings are switched from those programmed for data read mode to those programmed for servo mode, the AGC is switched to servo mode, and the $\overline{RDS}$, PPOL, and SEROUT outputs are enabled. The assertion of SG causes read mode and write mode to be overridden.

WRITE MODE OPERATION

The SSI 32P4904 supports three different write modes; Normal write mode, direct write mode 1 and direct write mode 2. The direct write modes require that either the direct write bit , bit 0 of the Control Operating Register, or the $\overline{DWR}$ pin be active. All three write modes require that the data separator be powered on.

Normal Write Mode

The SSI 32P4904 is in the normal write mode if WG/$\overline{WG}$ is active (register bit selectable whether active high or active low), $\overline{DWR}$ is high, and the direct write bit in the Control Operating Register is low. A minimum of one NRZ time period must elapse after RG goes low before WG/$\overline{WG}$ can be set active. The data separator PLL is phase-frequency locked to the TBG VCO output in this mode.

In normal write mode, the circuit first auto generates the VCO sync pattern, and finally scrambles the incoming NRZ data from the controller, encodes it into 8,9 GCR formatted data, precodes it, precompensates it, feeds it to a write data toggle flip-flop, and outputs it to the preamp for storage on the disk. The write data flip-flop is reset when WG/WG goes inactive to ease testing. This causes WD to be low and $\overline{WD}$ to be high when not in write mode.

While the preamble is being written, WCLK must continue to clock in all "0" NRZ data . After the required sync field has been written (approx. 8 byte times, min.), the NRZ data must be changed to 93H for a minimum of 5 byte times to write the minimum 5 byte equalizer training pattern. The device will continue to autogenerate the sync field pattern until the first 93H is latched at the NRZ interface, and detected. The device encodes the 93H pattern and writes the result as the training sequence. Next, the NRZ data must be changed to 96H for 1 byte time to write the sync byte. The user data must be presented at the NRZ interface immediately following the sync byte. Finally, after the last byte of user data has been clocked in, the WG/WG must remain active for a minimum of 28 NRZ-bit times in byte-wide mode to ensure the that the device is flushed of data (The delay is 29 NRZ-bit times in dual bit mode). WG/WG can then go inactive. WD/WD stops toggling a maximum of 2 NRZ (RCLK) time periods after WG/WG goes inactive.

The SSI 32P4904 also allows the precoder to be preset when the first training byte arrives at the precoder. With the Power-Down Register bit 4 (PCDIS) set to 0, the SSI 32P4904 allows presetting of the precoder. When the PCDIS bit is set to 0, the Power-Down Register bit 5 (PCSPOL) allows the precoder to be preset if the PCSPOL bit is a 1 and reset if the PCSPOL bit is set to 0. This allows the state of the sync pattern to be determined depending on the amount of training bytes sent to the NRZ interface. If the PCSPOL bit is set at 0 (precoder reset), the low frequency sync byte pattern

(or its inverse) is output of WD/$\overline{WD}$. If an odd number of training bytes is sent. If an even number of training bytes are sent, then the high frequency sync byte is output from WD/$\overline{WD}$.

Direct Write Mode 1

In this direct write mode, the NRZ data from the byte-wide interface bypasses the scrambler, the 8,9 encoder and the precoder, but is precompensated before going to the write data flip-flop and then to the WD/$\overline{WD}$ output pins. The precomp should be set to zero in this mode. The purpose of routing the signal to the precomp circuit is to generate a return to zero pulse every time a "1" occurs in the data so that the write data flip-flop is toggled. WCLK is required to clock the byte-wide NRZ data into the NRZ interface. Direct write mode 1 is entered simply by setting the DW bit (bit 0) in the Control Operating Register. This mode is not valid when using the dual bit NRZ interface.

Direct Write Mode 2

In this direct write mode, the data presented at the DWI/$\overline{DWI}$ input pins directly toggles the write data flip-flop which drives the WD/$\overline{WD}$ output pins. No WCLK is required in this mode, and the WD/$\overline{WD}$ output is not resynchronized. Direct write mode 2 is entered simply by driving the $\overline{DWR}$ input low.

DATA READ MODE OPERATION

Data read mode is initiated by setting the read gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when the read gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

Acquisition of DS VCO Sync

When RG is asserted an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier given the polarity changes of the incoming 1,1,-1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches 4, the internal read gate is asserted and the DS PLL input is switched from the TBG's VCO output to the sampled data input. This is also the point at which the DS PLL's phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter is also used to determine whether the selected sync field count, SFC, has been achieved. When the

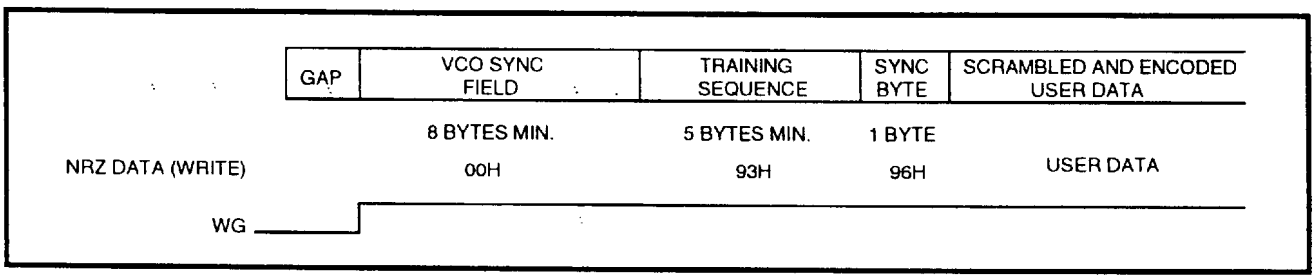


FIGURE 8: Hard Sector Write Sequence

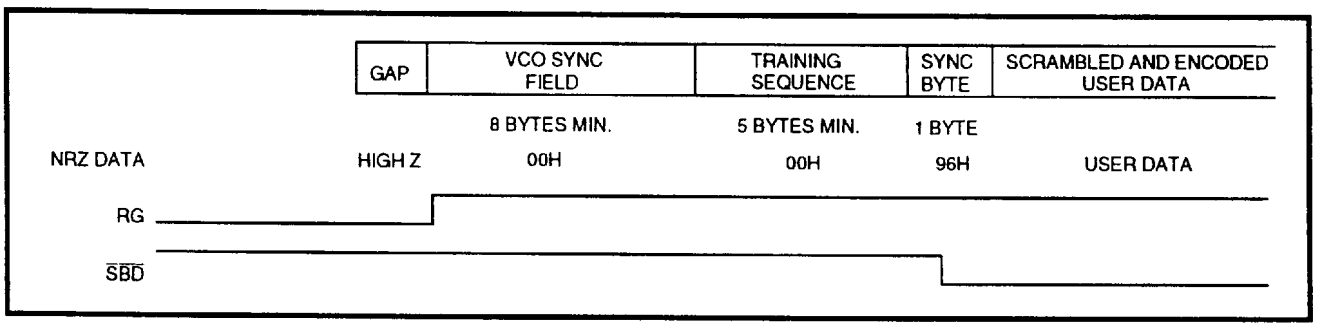


FIGURE 9: Hard Sector Read Sequence

Acquisition of DS VCO Sync (continued)

counter reaches the value specified by SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). Also at SFC, the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, the SFC can be set to 64, 80, 96 or 128 from the Sample Loop Control Register. These values for the SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundary Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the enable phase detector gain switching (GS) bit in the Control Operating Mode Register. When the GS bit is high, the phase detector gain is reduced by a factor of 5 after the SFC count is reached. When the GS bit is low, no phase detector gain switching takes place.

Also after SFC, the AGC feedback will be switched from the continuous time full-wave rectifier to sampled data feedback.

At SFC, the internal VCO lock signal activates the code word boundary detection circuitry to define the proper decode boundaries. Also, at count SFC, the RCLK generator source switches from the TBG's VCO output to the DS VCO clock signal which is phase locked to the incoming read data samples. The DS VCO is assumed locked to the incoming read samples at this point. A maximum of 1 RCLK time period may occur for the RCLK transition, however, no short duration glitches will occur. After the code word detection circuitry finds the proper code word boundary, the RCLK generator is resynchronized to guarantee that the RCLK is in sync with the data. The RCLK and NCLK outputs will not glitch and will not toggle during the RCLK generator resynchronization for up to 2 byte times maximum.

Also at the code word boundary detect, the internal 9-bit code words are allowed to pass to the ENDEC for decoding. This decoding will occur until read gate is deasserted.

Adaptive Equalizer Training Sequence

As was previously discussed, in a normal write sequence, a minimum of 5 bytes of NRZ 93H and one byte of 96H must be written between the end of the VCO sync field and the beginning of the user data. The 5 bytes of 93H are 8,9 encoded and precoded during write mode to produce the adaptive equalizer training pattern. During read mode, this sequence (100110011 read data sequence) is used to adaptively train the 3-tap transversal filter in a zero forcing manner. The error at the filter output is integrated to derive the tap weight multiplying coefficient, k_m. The filter input and output taps will have the same k_m. It is anticipated that the continuous time filter will be used for coarse equalization and that transversal filter will be used adaptively for fine tuning. This will reduce k_m's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during data mode can selected from the Sample Loop Control Register. After the training pattern, if the loop is active during data, the equalizer loop gain will be reduced by 4. The loop's integration time constant is made inversely proportional to the selected data rate.

Sync Byte Detect and NRZ Output

As the read data is 8,9 decoded, it is compared to an internally fixed sync byte (96H). When a match is found, the sync byte detect ($\overline{SBD}$) pin goes low and the NRZ output data that until now was held low, is changed to 96H. The next byte presented on the NRZ outputs is the first byte of user data. $\overline{SBD}$ will remain low and NRZ data will continue to be presented at the NRZ interface until the read gate is deasserted at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state.

POWER-DOWN OPERATION

The power management modes of the SSI 32P4904 are determined by the states of the Power-Down Register bits and the $\overline{\text{PDWN}}$ and SG inputs. The individual sections of the chip can be powered down or up using the Power-Down Register. A high level in a Power-Down Register bit disables that section of the circuit. The power-down information from the Power-Down Register takes effect immediately after the SDEN pin goes low.

When the $\overline{\text{PDWN}}$ input is low, the chip goes into full power-down mode regardless of the Power-Down Register settings or the state of the SG input.

When $\overline{\text{PDWN}}$ is high, SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the front end register bit. The back end Power-Down Register bits, which include the data separator and time base generator are not affected by the SG input.

The serial port is active in all power-down modes.

The time to restart from a full power-down is dependent on the PLL loop filter and the data rate.

The truth table for the various modes of operation is shown below:

SG, $\overline{\text{PDWN}}$	1,1	1,0	0,1	0,0
Front End	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Time Base Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON

R = Controlled by register bit. (Register bit =1 turns circuits OFF, Register bit = 0 turns circuits ON)

REGISTER DESCRIPTION

SERIAL PORT REGISTER DEFINITIONS

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Power-Down Register	0	0	0	0	0	1	0	0	04H
	Bit 7	ATO	Bit set to 1 enables ATO. Set bit to 0 for normal operation						
	Bit 6	PCD	Bit set to 1 disables precoder but does not initialize the flip-flop						
	Bit 5	PCSPOL	Precoder Force Polarity Bit 1 = initial precoder state is 1 (set) 0 = initial precoder state is 0 (reset)						
	Bit 4	PCSDIS	Precoder Force Disable Bit 1 = disable precoder force 0 = enable precoder force						
	Bit 3	FBYP	Filter Bypass Bit 1 = bypass filter 0 = normal operation						
	Bit 2	TB	Time base generator power-down when bit set to 1						
	Bit 1	DS	Data separator power-down when bit set to 1						
	Bit 0	PD	AGC, Filter, pulse detector, and servo power-down when bit set to 1						
Data Filter Cutoff Register	0	0	0	1	0	1	0	0	14H
	Bit 7	X	Don't Care						
	Bits 6-0	FC6-0	Filter cutoff frequency setting in non-servo mode fc (MHz) = 0.000122 • FC^2 + 0.1783 • FC - 0.6118, 20 ≤ FC ≤ 127 dec						
Servo Filter Cutoff Register	0	0	1	0	0	1	0	0	24H
	Bit 7	X	Don't Care						
	Bits 6-0	FCS6-0	Filter cutoff frequency setting in servo mode fc (MHz) = 0.000122 • FCS^2 + 0.1783 • FC - 0.6118, 20 ≤ FCS ≤ 127 dec						
Data Filter Boost Register	0	0	1	1	0	1	0	0	34H
	Bit 7	X	Don't Care						
	Bits 6-0	FB6-0	Filter boost setting in servo mode Boost (dB) = 20 • log [0.02083 • FB + 0.000056 • FB • FC - 0.000013 • FB^2 + 1] 0 ≤ FB ≤ 127 dec						
Servo Filter Boost Register	0	1	0	0	0	1	0	0	44H
	Bit 7	X	Don't Care						
	Bits 6-0	FBS6-0	Filter boost setting in servo mode Boost (dB) = 20 • log [0.02083 • FBS + 0.000056 • FBS • FCS - 0.000013 • FBS^2+ 1] 0 ≤ FBS ≤ 127 dec						

1 = power-down; 0 = power-up

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Viterbi Detector	0	1	0	1	0	1	0	0	54H
Threshold Register	Bit 7	X	Don't Care						
	Bits 6-0	VD6-0	Viterbi qualification threshold voltage V_{TH} (mV) = 7.42 • VD + 20 45 ≤ VD ≤ 127 dec						
Data Level Threshold	0	1	1	0	0	1	0	0	64H
Register	Bit 7	X	Don't Care						
	Bits 6-0	LD6-0	Data level qualification threshold voltage if WP/LT Register: ALE = 0 (Fixed levels) Prior to SFC: Lth (mV) = 4.784 • LD + 26 After SFC: Lth (mV) = 3.768 • LD + 18, 32 ≤ LD ≤ 127 dec if WP/LT Register: ALE = 1 (Adaptive levels) After SFC: Lth (%) = 0.787 • LD						
Servo Level Threshold	0	1	1	1	0	1	0	0	74H
Register	Bit 7	X	Don't Care						
	Bits 6-0	LDS6-0	Servo level qualification threshold voltage LSth (mV) = 4.784 • LDS + 26						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Control Test Mode Register	1	0	0	0	0	1	0	0	84H
	Bit 7	EFR	Sample Clock Source 0 = sample clock is from the DS VCO, normal operation 1 = sample clock is from the TBG output, a test mode						
	Bit 6	-	Factory reserved bit, must be set to 0 in application						
	Bits 5-3	TP3-1	Multiplexed test point selection						
	TP3	TP2	TP1	FUNCTION	TPA+, TPA-	TPB+, TPB-			
	0	0	0	Test Points Off	High Impedance	High Impedance			
	0	0	1	Equalizer Outputs	Equalizer A	Equalizer B			
	0	1	0	Eq Cont/Phase Det	Equalizer Control	Phase Detect Out			
	0	1	1	Viterbi Survival In	SSIN B+, B-	SSIN A+, A-			
	1	0	0	Survival Out/ In	Registers A, B	SSIN A+, A-			
	1	0	1	TBG /AGC Control	TBG Output	BYP (Buffered)			
	1	1	0	Eq Out/Viterbi In	Equalizer A	SSIN A+, A-			
	1	1	1	Eq Out/VCO ÷ 2	Equalizer A	DS VCO ÷ 2			
	Bit 2	VRDT	Enable VRDT Input 1 = digital input to the data decoder, used in testing only 0 = Viterbi survival outputs to the data decoder, normal use						
	Bit 1	DT	Enable TBG Pump-Down 1 = continuous pump-down, for test use only; FLTR1+ sinks current; FLTR1- sources current 0 = not in pump-down test mode						
	Bit 0	UT	Enable TBG Pump-Up 1 = continuous pump-up, for test use only; FLTR1+ sources current; FLTR1- sinks current 0 = not in pump-up test mode						
N Counter Register	1	0	0	1	0	1	0	0	94H
	Bit 7	X	Don't Care						
	Bits 6-0	N6-0	N Counter 2 < N < 127						
M Counter Register	1	0	1	0	0	1	0	0	A4H
	Bits 7-0	M7-0	M Counter 2 < M < 255 FTBG = FREF • [(M+1) ÷ (N+1)]						
Data Rate Register	1	0	1	1	0	1	0	0	B4H
	Bit 7	X	Don't Care						
	Bits 6-0	DR6-0	Fvco (MHz) = 9/8 Data Rate = 0.6685 •DR + 5.1 Write Precomp/Level Threshold Time Constant Register						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Write Precomp/Level Threshold Time Constant Register	1	1	0	0	0	1	0	0	C4H
	Bits 7-5	TC3-1	Adaptive level qualification threshold time constant for decision directed phase detector. (valid after SFC)						
	TC3	TC2	TC1	TIME CONSTANT					
	0	0	0	300 ns					
	0	0	1	400 ns					
	0	1	0	500 ns					
	0	1	1	600 ns					
	1	0	0	700 ns					
	1	0	1	800 ns					
	1	1	0	900 ns					
	1	1	1	1000 ns					
	Bit 4	ALE	Enable Adaptive Level Qualification in Decision Directed Phase Detector 1 = adaptive mode 0 = fixed level qualification						
	Bit 3	FSD	Fail Safe Disable Bit 1 = precomp fail safe off 0 = precomp fail safe on						
Write Precomp/Level Threshold Time Constant Register	1	1	0	0	0	1	0	0	C4H
	Bits 2-0	WPC2-0	Write Precomp Setting						
	WPC2	WPC1	WPC0	WRITE PRECOMP MAGNITUDE					
	0	0	0	No precomp					
	0	0	1	3.3% code period shift					
	0	1	0	6.6% code period shift					
	0	1	1	9.9% code period shift					
	1	0	0	13.2% code period shift					
	1	0	1	16.5% code period shift					
	1	1	0	19.8% code period shift					
	1	1	1	23.1% code period shift					

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Control Operating Register	1	1	0	1	0	1	0	0	D4H
	Bits 7	WGP	Write Gate Polarity 1 = positive (active high) 0 = negative (active low)						
	Bit 6	SPDM	Servo Peak Detect Mode 1 = dual comparator (window) 0 = hysteresis						
	Bit 5	BP	Enable Bypass of Write Precoder 1 = enabled 0 = disabled, (normal operation)						
	Bit 4	DB	Enable Dual Bit Interface 1 = dual bit DB1-0 interface enabled 0 = dual bit interface disabled, i.e. byte-wide interface enabled						
	Bit 3	BT	Bypass Time Base Generator 1 = data synchronizer reference frequency is FREF input 0 = data synchronizer reference frequency is TBG output, (normal operation)						
	Bit 2	SD	Disable Data Scrambler/Descrambler 1 = disabled 0 = enabled, (normal operation)						
	Bit 1	GS	DS Phase Detector Gain Switching 1 = disabled 0 = enabled, (normal operation)						
	Bit 0	DW	Enable Direct Write From Byte-Wide NRZ (bypasses scrambler & ENDEC) 1 = enabled 0 = disabled, (normal operation)						

SERIAL PORT REGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$	
Sample Loop Control Register	1	1	1	0	0	1	0	0	E4H
	Bit 7	WGH	Bit set to 1 enables hold while WG is active						
	Bits 6-5	SFC1-0	Sync Field Count						
	SFC1	SFC0	SYNC FIELD COUNT - CODE CLOCKS						
	0	0	64						
	0	1	80						
	1	0	96						
	1	1	128						
	Bit 4	AEGS	Adaptive Equalizer Loop Time Constant Shift 1 = equalizer loop time constant is increased to 4X in the data field relative to the preamble field, i.e. loop gain is reduced to 1/4 0 = equalizer loop time constant same in preamble & data fields						
	Bit 3	AED	Enable Adaptive Equalizer on Data Field 1 = adaptive equalizer in use after preamble field, if AEE bit = 1 0 = adaptive equalizer disabled after preamble field						
	Bit 2	AEE	Enable Adaptive Equalizer 1 = adaptive equalizer enabled for use in preamble field, and after the preamble field if AED bit = 1 0 = adaptive equalizer disabled						
	Bits 1-0	AGC1-0	AGC charge pump current in sampled AGC mode AGC charge/discharge current (μA) = 0.28 • AGC • data rate (Mbit/s) e.g., for data rate = 72 Mbit/s and AGC =10 = 2 dec charge pump current = 40.3 μA						
Damping Ratio Control Register	1	1	1	1	0	1	0	0	F4H
	Bit 7	X	Don't Care						
	Bits 6-0	D6-0	Damping Amplifier Gain A = D • (0.7/127) Damping Ratio = $\frac{A \cdot KVCO \cdot 0.25}{2 \cdot \omega_n}$						

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	I	AGC/Filter Analog Circuit Supply
VPF	I	Time Base Generator ECL Supply (connect to analog supply)
VPT	I	Time Base Generator PLL Analog Circuit Supply
VPP	I	Data Separator PLL Analog Circuit Supply
VPD	I	TTL Buffer I/O Digital Supply
VPC	I	Internal ECL, CMOS Logic Digital Supply
VPS (2)	I	Sampled Data Processor Supply
VNA	I	AGC/Filter Analog Circuit Ground
VNF	I	Time Base Generator ECL Ground (connect to analog ground)
VNT	I	Time Base Generator PLL Analog Circuit Ground
VNP	I	Data Separator PLL Analog Circuit Ground
VND	I	TTL Buffer I/O Digital Ground
VNC	I	Internal ECL, CMOS Logic Digital Ground
VNS (2)	I	Sampled Data Processor Ground

ANALOG INPUT PINS

VIA+, VIA-	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins
DP, DN		ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator

ANALOG OUTPUT PINS

TPA+, TPA-	O	TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the Test Point Control Register. The signals include the equalizer control voltage and output, various timing loop control signals and the Viterbi Survival Register outputs. The test points are provided to show how the signal is being processed. Internal "pull-down" resistors to ground are provided. To save power when not in test mode, the Control Test Register bits 3-5 must be set to "0".
TPB+, TPB-	O	TEST PINS: Emitter output test points similar to TPA+ and TPA-. The pins are used to look at the other phase of the interleaved signals.
ATO	O	ANALOG TEST OUT: A test point that is enabled by setting bit 7 in the Power-Down Register to "1". This test point is used to indicate the operation of controlled functions which cannot be easily determined by direct testing of the circuit pins. The selected output is determined by the address in the Serial Control Register.

ANALOG OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
ATRN	O	ANALOG TEST OUT RETURN: A test point used as the ATO return.
ON+, ON-	O	FILTER NORMAL OUTPUTS: These are the filter normal low pass output. They should be AC coupled to the data comparator in the pulse qualifier. Open emitter output with internal pull-down. If driving more than coupling cap, external pull-down resistor to GND may be required.
OD+, OD-	O	FILTER DIFFERENTIATED OUTPUTS: These are the filter time differentiated low pass output. They should be AC coupled, for low DC offset, to the clock comparator in the pulse qualifier. Open emitter output with internal pull-down. If driving more than coupling cap, external pull-down resistor to GND may be required.
SEROUT	O	MULTIPLEXED SERVO OUTPUT: Open Emitter. Full-wave rectified output referenced to SREF. Requires external pull-down to GND.
SREF	O	SERVO REFERENCE OUTPUT: +2 VDC reference voltage, baseline for servo bursts. Open Emitter. Requires external pull-down to GND.

ANALOG CONTROL PINS

BYP	-	The data AGC integrating capacitor, C_{BYP}, is connected between BYP and VPA. This pin is used when not in servo read mode (SG = 0).
BYPS	-	The servo AGC integrating capacitor, C_{BYPS}, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1+, FLTR1-	-	TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2+, FLTR2-	-	DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR	-	CURRENT REFERENCE RESISTOR INPUT: An external 1%, 12.1 kΩ resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs.
VRX	-	FILTER REFERENCE RESISTOR INPUT: An external 1%, 12.1 kΩ resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC	-	AGC REFERENCE VOLTAGE: VRC is derived by a bandgap reference from VPA.

PIN DESCRIPTION (continued)

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ	I	LOW-Z MODE INPUT: TTL compatible CMOS control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor. When pulled low, keeps the AGC amplifier and filter inut impedance high. An open pin is a logic high.
FASTREC	I	FAST RECOVERY: TTL compatible CMOS control pin which, when pulled high, puts the AGC charge pump in the fast decay mode. An open pin is a logic high.
$\overline{\text{PDWN}}$	I	POWER DOWN CONTROL: CMOS input power control pin. When set to logic low, the entire chip is in sleep mode with all circuitry, except serial port, shut down. This pin should be set to logic high in normal operating mode. Selected circuitry can also be shut down by the Power-Down Register but is overridden by this pin. Do not leave open.
$\overline{\text{HOLD}}$	I	AGC HOLD CONTROL INPUT: TTL compatible CMOS control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
FREF	I	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. When bits 2 or 7 of the Control Test Register are set, FREF replaces the VCO as the input to the data separator.
WCLK	I	WRITE CLOCK: TTL compatible CMOS input that latches in the data at the selected NRZ interface on the rising edge . Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG	I	READ GATE: TTL compatible CMOS input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the read data input and enables the read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG/$\overline{\text{WG}}$	I	WRITE GATE: TTL compatible CMOS input that enables the write mode. Register selection through serial port for active high or active low. An open pin is at logic high. Setting bit 7 in the Sample Loop Control Register to 1 enables hold on the AGC while write gate is active.
SG	I	SERVO GATE: TTL compatible CMOS input that, when pulled high, enables the servo read mode. An open pin is at logic high.

DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
VRDT	I	VITERBI READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the Control Test Register.
$\overline{DWR}$	I	DIRECT WRITE MODE 2 ENABLE: Enables DWI, $\overline{DWI}$ inputs to the write data flip-flop when input is low. TTL compatible CMOS levels. Open pin is at logic high. When active, overrides bit 0 selection in Control Operating Register.
DWI, $\overline{DWI}$	I	DIRECT WRITE INPUTS: Inputs connect to the toggle input of the write data flip-flop when $\overline{DWR}$ is low. PECL input levels. Can be left open.

DIGITAL BI-DIRECTIONAL PINS

NRZ0-7	I/O	BYTE-WIDE NRZ DATA PORT: TTL compatible CMOS bi-directional input/output. Input to the encoder when WG/$\overline{WG}$ is active. Output from the decoder when RG is high. Can be left open if not used. Active when Bit 4 of Control Operating Register is set to 0.
NRZP	I/O	NRZ DATA PARITY BIT: Active when in byte-wide mode. TTL compatible CMOS bi-directional input/output. Generates even read parity when RG is high, and accepts even write parity when WG/$\overline{WG}$ is active. Can be left open if not used.
DB0-1	I/O	DUAL BIT NRZ DATA PORT: TTL compatible CMOS bi-directional input/output. Input to the encoder when WG/$\overline{WG}$ is active. Output from the decoder when RG is high. Can be left open if not used. Active when bit 4 of Control Operating Register is set to 1.

DIGITAL OUTPUT PINS

RCLK	O	READ REFERENCE CLOCK: A multiplexed clock source used by the controller. When RG is low, RCLK is synchronized to the time base generator output, FTBG. When RG goes high, RCLK remains synchronized to FTBG until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. CMOS output levels. (Limited swing)
NCLK	O	NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the frequency of RCLK. NCLK is disabled in dual bit mode. CMOS output levels. (Limited swing)
$\overline{SBD}$	O	SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.

DIGITAL OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
PERR	O	PARITY ERROR: CMOS output that goes high if a parity error occurs. Active in byte wide mode only.
WD, $\overline{WD}$	O	WRITE DATA: Write data flip-flop output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock FTBG, except in direct write mode 2. Differential PECL output levels. Reset to WD is low and $\overline{WD}$ is high when write gate goes inactive.
$\overline{RDS}$	O	SERVO READ DATA: Read data pulse output for servo read data. Active low limited swing CMOS output. Output active when SG is high, and high when SG is low.
PPOL	O	SERVO READ DATA POLARITY: Read data pulse polarity output for servo read data. Active high limited swing CMOS output. A negative swing servo read data leads to a low output of PPOL and a positive swing servo read data leads to a high output of PPOL. Output active when SG is high.

SERIAL PORT PINS

SCLK	I	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input levels.
SDATA	I	SERIAL DATA: Input pin for serial data; the first bit is the R/$\overline{W}$ bit and is always set to 0. The next three bits are the device select bits and are always written S0 = 0, S1 =1, S2 = 0. The following four bits are the address bits A0 - A3 and the last 8 are the data bits D0 - D7. The bits are entered LSB first, MSB last. CMOS input levels.
SDEN	I	SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. CMOS input levels.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Positive 5 V Supply Voltage (Vp)	-0.5 to 7 V
Storage Temperature	-65 to 150° C
Solder Vapor Bath	215° C, 90 sec, 2 times
Junction Operating Temperature	+135° C
Output Pins	±10 mA
Analog Pins	±10 mA
Voltage Applied to other Pins	-0.3 V to Vp + 0.3 V

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5 V < positive supply voltage < 5.5 V, 0° C < T (ambient) < 70° C, and 25° C < T(junction) < 135° C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC (VP_N)	Outputs and test point pins open Ta = 27° C		150		mA
PWR Power Dissipation Normal Mode	Outputs and test point pins open, Ta = 27°C		750	1100	mW
PWR Data Separator Off	Power-Down Register = 2d		325	470	mW
PWR Data Separator & TBG Off	Power-Down Register = 6d		310	450	mW
PWR Idle Through Serial Port	Power-Down Register = 7d			15	mW
Idle	PDWN = low			5	mW

DIGITAL INPUTS

TTL Compatible CMOS Inputs

Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2			V
Input Low Current	I_{IL}	V_{IL} = 0.4 V	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.4 V			20	µA

FREF and VRDT Inputs

Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2			V
Input Low Current	I_{ILF}	V_{IL} = 0.4 V	-250			µA
Input High Current	I_{IHF}	V_{IH} = 2.4 V			500	µA

CMOS Inputs

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage	V_{ILC}	VPC = 5 V			1.5	V
Input High Voltage	V_{IHC}	VPC = 5 V	3.5			V

Pseudo ECL Compatible Inputs

Input Low Voltage	V_{IL}		VPD - 2		V_{IH} - 0.25	V
Input High Voltage	V_{IH}		VPD - 1.1		VPD - 0.4	V
Input Current			-100		+100	µA

DIGITAL OUTPUTS

CMOS Outputs

Output Low Voltage	I_{OL} = +2 mA			0.45	V
Output High Voltage	I_{OH} = -100 µA	0.7 • VPD			V
Rise Time	C_L =15 pF, 0.8 V to 2 V			10	ns
Fall Time	C_L =15 pF, 2 V to 0.8 V			15	ns

Digital Differential Outputs (WD, $\overline{WD}$)

Output Low Voltage	I_{OL} = 2 ma	VPD-1.9		VOH - 0.275	V
Output High Voltage	I_{OH} = 2 ma	VPD-1.4		VPD - 0.5	V
Output Sink Current			3.2		mA

TEST POINT OUTPUT LEVELS

Test Point Output TPA+, TPA- TPB+, TPB-			0.8		Vp-pd
ATO Test Point	Rload ≥ 10 MΩ	0		1	V

SERIAL PORT TIMING

Refer to Figure 7

SCLK Data Clock Period	T_C		100			ns
SCLK Low Time	T_{CKL}		40			ns
SCLK High Time	T_{CKH}		40			ns
Enable to SCLK	T_{SENS}		30			ns
SCLK to Disable	T_{SENH}		30			ns
Data Set-Up Time	T_{DS}		15			ns
Data Hold Time	T_{DH}		15			ns
SDEN Minimum Low Time	T_{SL}		200			ns

AGC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

AGC Amplifier

The input signals are AC coupled to VIA+ and VIA-. ON+ and ON- are ac coupled to DP and DN. Integrating capacitor CBYP = 1000 pF, is connected between BYP and VPA. Integrating capacitor CBYPS = 1000 pF, is connected between BYPS and VPA. Unless otherwise specified, the output is measured differentially at DP and DN, Fin = 5 MHz, the filter frequency fc = maximum and the filter boost at fc = 0 dB. All specifications apply equally to servo and read mode prior to SFC.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Range	Filter Boost = 0 dB @ fc 5 MHz ≤ fc ≤ 18 MHz, Fin = fc	20		250	mVp-pd
Input Range	Filter Boost = 11 dB @ fc 9 MHz ≤ fc ≤ 18 MHz, Fin = fc	20		200	mVp-pd
DP/DN Voltage	VIA+ = 0.1 Vp-pd 1,1,-1,-1,— pattern	1.27	1.55	1.87	Vp-pd
DP/DN Voltage Variation	20 mVp-pd < VIA+ < 250 mVp-pd			5	%
Gain	Low end maximum			1	V/V
Gain	High end minimum	64			V/V
Gain Sensitivity	BYP voltage change		38		dB/V
Differential Input Impedance	LOWZ = low	4	5.6	7.7	kΩ
	LOWZ = high		280		Ω
Single-Ended Input Impedance	LOWZ = low		1.9		kΩ
	LOWZ = high		100		Ω
Output Offset Voltage	Gain = 64 V/V	-400		400	mV
Input Noise Voltage	Gain = 64 V/V, FC = 127 Rs = 0 Ω		15	30	nV/√Hz
CMRR	Gain = 64 V/V, FC = 127 Fin = 5 MHz	30			dB
PSRR	Gain = 64 V/V, FC = 127 Fin = 5 MHz	35			dB
Gain Decay Time	VIA+ = 240 to 120 mVp-pd DP/DN > 0.9 final value data mode, max data rate		21		µs
Gain Attack Time	VIA+ = 120 to 240 mVp-pd DP/DN < 1.1 final value data mode, max data rate		3		µs

ELECTRICAL SPECIFICATIONS (continued)

AGC CONTROL

The input signals are AC coupled into DP/DN, CBYP = 1000 pF to VPA & CBYPS = 1000 pF to VPA.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Decay Current Normal I_D	FASTREC = low, SG = low data rate in Mbit/s 24 ≤ data rate < 80		$2.8 \cdot 10^{-7}$ • data rate		A
Servo Mode Decay Current Normal	FASTREC = low, SG = high		8.3		µA
Fast Discharge Current I_{DF}	FASTREC = high		8 • I_D		A
Charge Pump Attack, Current I_{CH}	TBD ≤ DP/DN ≤ TBD Vp-pd FASTREC = low		17 • I_D		A
Fast Attack I_{CHF}	IDP - DNI ≥ 0.65V AGC pin open		8 • I_{CH}		A
Sample Data AGC Peak Charge Current	0 ≤ AGC ≤ 3 data rate in Mbit/s		$2.8 \cdot 10^{-7}$ • AGC • data rate		A
Sample Data AGC Peak Discharge Current	0 ≤ AGC ≤ 3 data rate in Mbit/s		$2.8 \cdot 10^{-7}$ • AGC • data rate		A
BYP Pin Leakage Current	$\overline{HOLD}$ = low V_{BYP} = VRC	-50		+50	nA
BYPS Pin Leakage Current	$\overline{HOLD}$ = low V_{BYPS} = VRC	-50		+50	nA
VRC Reference Voltage	-100 µA (source) ≤ IO ≤ +500 (sink) µA	VPA - 2.45		VPA - 2.15	V

PULSE QUALIFIER CHARACTERISTICS

General

A 1 Vp-pd @ 5 MHz input signal is AC coupled into DP/DN.
A 1 Vp-pd @ 5 MHz input signal is AC coupled into CP/CN.

DP-DN Differential Input Resistance	LOWZ = low	6		13	kΩ
	LOWZ = high		0.8		kΩ
DP-DN Differential Input Capacitance				5	pF
CP-CN Differential Input Resistance		6		13	kΩ
CP-CN Differential Input Capacitance				5	pF

DUAL LEVEL QUALIFIER

See General for input conditions unless otherwise specified.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Data Level Threshold	L_{TH}	Prior to SFC L_{TH} (mV) = 4.784 • LDS + 26 32 ≤ LD ≤ 127		L_{TH}		V
Data Level Threshold	L_{TH}	After SFC L_{TH} (mV) = 3.768 • LD + 18 32 ≤ LS ≤ 127		L_{TH}		V
Servo Level Threshold	LS_{TH}	LS_{TH} (mV) = 4.784 • LDS + 26 32 ≤ LS ≤ 127	LS_{TH} - 9%	LS_{TH}	LS_{TH} + 9%	V
$\overline{RDS}$ Output Pulse Width	PW	DP-DN signal set to exceed amplitude threshold, -90° from CP-CN	18		48	ns
$\overline{RDS}$ Output Pulse Rising Edge Delay	PRD	From PPOL Edge Transition	18		55	ns
$\overline{RDS}$ Output Pulse Pairing	PP	Fin = 5 MHz, FCS = 40	- 2		+2	ns

VITERBI QUALIFIER

See General for input conditions unless otherwise specified.

Viterbi Threshold	V_{TH}	V_{TH}(mV) = 7.42 • VD + 20 45 ≤ VD ≤ 127	V_{TH} - 9%	V_{TH}	V_{TH} + 9%	V

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply. The input signals are AC coupled to VIA+ and VIA- . All specifications identical for identical data and servo register settings.

Data uses C_{BYP} from BYP to VPA and servo uses C_{BYPS} from BYPS to VPA. VBYP = VRC

Filter Cutoff Range	fc_R	fc (MHz) = 0.000122 • FC^2 + 0.1783 • FC - 0.6118 20 ≤ FC ≤ 127 0 dB Boost		3 - 24		MHz
Filter Cutoff Frequency	fc	fc = 127, 0 dB Boost		24		MHz
Filter fc Accuracy	fc_A	48 ≤ FC ≤ 127	-15.5		+15.5	%
		20 ≤ FC ≤ 47	-20		+20	%
OD Gain	A_D	Fin = 0.67 • fc 0 dB Boost	0.75 • A_N		1.2 • A_N	V/V

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Boost @ *fc*	FB = 127, FC = 127		12.75		dB
Boost Accuracy	FB = 127, 42 ≤ FC ≤ 127	-2		+2	dB
	FB = 67, 42 ≤ FC ≤ 127	-1.5		+1.5	dB
Group Delay Variation TGD	*fc* = 24 MHz F = 0.2 *fc* to *fc*, 0 dB boost	-600		+600	ps
	fc = 8 MHz to 24 MHz F = 0.2 *fc* to *fc* FB = 0 to 127	-3		+3	%
	fc = 3 MHz to 8 MHz F = 0.2 *fc* to *fc* FB = 0 to 127	-6.5		+6.5	%
	fc = 8 MHz to 24 MHz F = *fc* to 1.75 *fc* FB = 0 to 127	-4		+4	%
	fc = 3 MHz to 8 MHz F = *fc* to 1.75 *fc* FB = 0 to 127	-6		+6	%
Filter Output Dynamic Range ON+ - ON-	THD = 2.1% max, *fc* = 127 F = 0.67 *fc* CL = 15 pF	1.4			Vp-p
ON+ - ON- Output Noise Voltage, No Boost	BW = 100 MHz, Rs = 50 Ω FC = 127, boost = 0 dB AGC gain = min.		3.5	5.5	mV rms
ON+ - ON- Output Noise Voltage, Maximum Boost	BW = 100 MHz, Rs = 50 Ω FC = 127, FB = 127		7	13	mV rms
OD+ - OD- Output Noise Voltage, No Boost	BW = 100 MHz, Rs = 50 Ω FC = 127, boost = 0 dB AGC gain = min.		7.3	14	mV rms
OD+ - OD- Output Noise Voltage, Maximum Boost	BW = 100 MHz, Rs = 50 Ω FC = 127, FB = 127		18.3		mV rms
Filter Output Sink Current, IO-		0.8	3		mA
Filter Output Source Current, IO+		2	5		mA
Filter Output Resistance Ro	single-ended			200	Ω
Rx Pin Voltage V_{RX}	Ta = 27° C		600		mV
	Ta = 127° C		800		mV
Rx Resistance	1% fixed value		12.1		kΩ

TRANSVERSAL FILTER CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
k_m Range		-0.20		+0.20	

TIME BASE GENERATOR CHARACTERISTICS

FREF Input Range	Control Operating Register BT bit = 0	6		20	MHz
	Control Operating Register BT bit = 1 Control Test Register EFR bit =1			90	MHz
FREF Input Pulse Width	Control Operating Register BT bit = 0	10			ns
	Control Operating Register BT bit = 1 Control Test Register EFR bit =1	5			ns
FTBG Frequency Range				100	MHz
FTBG Jitter	> 10K samples DR < 100			250	psRMS
	DR > 100			200	psRMS
M Counter Range		2		255	
N Counter Range		2		127	
VCO Center Frequency FTBG	FLTR1+ - FLTR1- = 0 V FTBG = [(0.6685 • DR) + 5.1] MHz RR = 12.1 kΩ	0.80 FTBG		1.20 FTBG	MHz
VCO Dynamic Range	-2 V ≤ FLTR1+ - FLTR1- ≤ +2 V FTBG = 65 MHz	±25		±45	%
VCO Control Gain KVCO	ωi =2 π • FTBG -2 V ≤ FLTR1+ - FLTR1- ≤ 2 V	0.12 • ωi	0.18 • ωi	0.24 • ωi	rad/(V-S)
Phase Detector Gain KD	KD = (2.056 • DR) + 2.09	0.83 • KD		1.17 • KD	µA/rad
KVCO • KD Product Accuracy		-28		+28	%

ELECTRICAL SPECIFICATIONS (continued)

DATA SEPARATOR CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

Read Mode - Byte Wide

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read Clock Rise Time	TRRC	0.8 V to 2 V CL < 15 pF			10	ns
Read Clock Fall Time	TFRC	2 V to 0.8 V CL < 15 pF			10	ns
Nibble Clock Rise Time	TRNC	0.8 V to 2 V CL < 15 pF			10	ns
Nibble Clock Fall Time	TFNC	2 V to 0.8 V CL < 15 pF			10	ns
RCLK Pulse Width	TRD	Except during re-sync	4/9TORC-5		4/9TORC+5	ns
NCLK Pulse Width	TQD	Except during re-sync	2/9TORC-5		2/9TORC+5	ns
		During re-sync	No Glitch		2(TORC)	ns
NCLK Clock Period	TONC	Except during re-sync	4/9TORC-10		5/9 TORC+10	ns
		During re-sync	No Glitch		2(TORC)	ns
NCLK Skew	TQS		-10		+10	ns
RCLK Re-Sync Period	T_{DC2}	TORC = RCLK period	TORC		2(TORC)	ns
NCLK Re-Sync Period	T_{DC1}	TORC = RCLK period	TORC/2		TORC	ns
NRZx Out Set-Up and Hold Time	TNS, TNH		25			ns

Write Mode - Byte Wide

Write Data Position Accuracy	TWD	without precomp CL < 15 pF	TTBG-0.5		TTBG+0.5	ns
Write Data Rise Time	TRWD	20% to 80% points 2KΩ to GND CL < 15 pF			5	ns
Write Data Fall Time	TFWD	80% to 20% points 2 kΩ to GND CL < 15 pF			5	ns
Write Clock Rise Time	TRWC	0.8 V to 2 V CL < 15 pF			10	ns
Write Clock Fall Time	TFWC	2 V to 0.8 V CL < 15 pF			8	ns
NRZx Set-Up Time	TSNRZ		30			ns
NRZx Hold Time	THNRZ		10			ns

Read Mode - Dual Bit

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
RCLK Low Time	RCL	CL < 15 pF, ≤ 0.8 V	8			ns
RCLK High Time	RCH	CL < 15 pF, ≥ 2 V	7.5			ns
Read Clock Rise Time	TRRC	0.8 V to 2 V CL < 15 pF			3.5	ns
Read Clock Fall Time	TFRC	2 V to 0.8 V CL < 15 pF			2.5	ns
DBOUT (1:0) Set-Up Time	DBOS	CL < 15 pF	5			ns
DBOUT (1:0) Hold Time	DBOH	CL < 15 pF	5			ns

Write Mode - Dual Bit

WCLK Period	TWC	CL < 15 pF	22			ns
WCLK Low Time	WCL	CL < 15 pF, ≤ 0.8 V	7.5			ns
WCLK High Time	WCH	CL < 15 pF, ≥ 2 V	7.5			ns
DBIN (1:0) Set-Up Time	DBIS	CL < 15 pF	4			ns
DBIN (1:0) Hold Time	DBIH	CL < 15 pF	3			ns

Write Precompensation

Write Precomp Time Shift Magnitude	TPC	TPC = 0.033 • WPC • TTBG 0 ≤ WPC ≤ 7	0.8 • TPC - 0.5		1.2 • TPC + 0.5	ns

Data Synchronizer PLL

VCO Center Frequency FVCO	FLTR2+ - FLTR2- = 0 V FVCO = [(0.6685 • DR) + 5.1] MHz RR = 12.1 kΩ	0.8 FVCO		1.2 FVCO	MHz
VCO Dynamic Range in Each Direction	-2 V ≤ FLTR2+ - FLTR2- ≤ +2 V	±20			%

Data Synchronizer PLL (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO Control Gain & M, M • KVCO	$\omega i = 2\pi/TVCO$ M = 2.4 • (DR/127) -0.25 V ≤ FLTR2+ - FLTR2- ≤ +0.25 V	0.11 • ωi • M		0.35 • ωi • M	rad/(V-S)
Charge Pump Transconductance	Gm = 200 µA/V during synchronization	0.6 • Gm		1.58 • Gm	A/V
Idle Mode Phase Detector Gain KDI	KDI = 0.25 • Gm • M		KDI		µA/rad
Gm • M • KVCO Product Accuracy		-28		+28	%
A • KVCO Product Accuracy	A = 0.7 • (DRC/127)	-30		+30	%

SERVO CHARACTERISTICS

Servo Gain, (SEROUT-SREF)/(DP-DN)	DP/DN to SEROUT DP/DN = 1.4 Vp-pd Fin = 5 MHz	0.60	0.70	0.80	V/Vp-pd
200 mV Reference, SEROUT	SG = 0	175	195	215	mV
SEROUT Offset, SEROUT - SREF	SG = 0	0		55	mV
SREF Output Voltage	IL = 1 mA		2.15		V
SREF Switching Time	to ±10% of final value	1			µs

MODE CONTROL

WG/$\overline{WG}$	RG	DEVICE MODE	DESCRIPTION
0/1	0	Idle Mode	DS VCO locked to FTBG. NRZ7-0, DB1-0 tri-stated.
0/1	1	Data Read Mode	DS PLL acquisition, adaptive equalizer training, code word boundary search and detect, decode, sync byte detect, and NRZ data output. DS VCO switched from FTBG to read data after preamble detect. RCLK gen. input switched from FTBG to DS VCO. RCLK re-synchronized to read data at code word boundary detect. NRZ7-0, DB1-0 active.
1/0	0	Data Write Mode	Write mode preamble insertion and data write. DS VCO locked to FTBG. RCLK synchronized to FTBG. WD and $\overline{WD}$ active. NRZ7-0, DB1-0 tri-stated.
1/0	1	Read Override	RG overrides WG/$\overline{WG}$ which causes any write in progress to cease and data read mode to be entered.

WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write Precomp Register. The Write Precomp Register bits are as follows:

BIT	NAME	FUNCTION
0	WPC0	Write Precomp Bit 0
1	WPC1	Write Precomp Bit 1
2	WPC2	Write Precomp Bit 2
3	FSD	Fail Safe Disable
4	ALE	Adaptive Level Equalization enable
5	TC1	Level Time Constant Bit 1
6	TC2	Level Time Constant Bit 2
7	TC3	Level Time Constant Bit 3

WRITE PRECOMP CONTROL (continued)

T_{TBG} is the period of the reference frequency provided by the internal time base generator.

WPC2	WPC1	WPC0	WPC Value	Shift
0	0	0	0	None
0	0	1	1	3.3% T_{TBG}
0	1	0	2	6.6% T_{TBG}
0	1	1	3	9.9% T_{TBG}
1	0	0	4	13.2% T_{TBG}
1	0	1	5	16.5% T_{TBG}
1	1	0	6	19.8% T_{TBG}
1	1	1	7	23.1% T_{TBG}

BIT N-1	BIT N	BIT N+1	BIT N COMPENSATION
0	1	0	None
1	1	0	Late
1	1	1	Late (N and N + 1)

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude

TC3	TC2	TC1	NOMINAL FILTER TIME CONSTANT
0	0	0	300 ns
0	0	1	400 ns
0	1	0	500 ns
0	1	1	600 ns
1	0	0	700 ns
1	0	1	800 ns
1	1	0	900 ns
1	1	1	1000 ns

Adaptive threshold level filter time constant (Decision directed phase detector, after SFC)

TEST POINT CONTROL

The test points are controlled by the TP1, TP2, and TP3 bits of the Control Test Register.

TP3	TP2	TP1	FUNCTION	TPA+, TPA-	TPB+, TPB-
0	0	0	Test Outputs Powered Down	High Impedance	High Impedance
0	0	1	Equalizer Outputs	Equalizer A	Equalizer B
0	1	0	Equalizer/Phase Detector	Equalizer Control	Phase Detect Out
0	1	1	Viterbi Survival In	SSINB+, B-	SSINA+, A-
1	0	0	Survival Out/Survival In	Registers A, B	SSINA+, A-
1	0	1	TBG Fout/AGC CONTROL	TBG Fout	BYP (Buffered)
1	1	0	Equalizer Out/Viterbi Survival In	Equalizer A	SSINA+, A-
1	1	1	Equalizer Out/DS VCO ÷ 2	Equalizer A	DS VCO CLK ÷ 2

The test point functions are further described below:

1. Test 1, Equalizer Outputs. The equalizer output "1" and "0" values can be observed.

2. Test 2A, Equalizer Control. The integrated control voltage produced by the deviation of the "0" samples from ideal is observed.
   Test 2B, Phase Detect Out. The sampled data phase detector output is observed.

3. Test 3, Viterbi Survival In. The four inputs of the two interleaved Viterbi registers are observed by single ended probing TPA+, TPA-, TPB+, TPB-.

4. Test 4A, Viterbi Survival Out. The two outputs of the two interleaved Viterbi registers are observed by single ended probing TPA+, TPA-.
   Test 4B, Viterbi Survival In. Two inputs of one of the two interleaved Viterbi registers are observed by single ended probing TPB+, TPB-.

5. Test 5A, VCO Outputs. The TBG PLL outputs are observed.
   Test 5B, AGC Control. The integrated control voltage produced by the deviation of the "1" samples from the ideal is observed.

6. Test 6A, Equalizer Output. The equalizer output "1" and "0" values can be observed.
   Test 6B, Viterbi Survival In. Two inputs of one of the two interleaved Viterbi registers are observed by single ended probing TPB+, TPB-.

7. Test 7A, Equalizer Output. The equalizer output "1" and "0" values can be observed.
   Test 7B, VCO Outputs. The Data Separator VCO ÷ 2 output is observed.

   To save power in normal operation, the TEST POINTS SHOULD BE POWERED DOWN by selecting TP1 = TP2 = TP3 = "0" the Control Test Mode Register.

TEST POINT CONTROL (continued)

DAC Testing

A testing capability for some of the internal DACs has been incorporated. A DAC is selected by the Serial Port Address Register (The last register with DAC sent to serial port). The ATO pin is enabled by setting Bit 7 in the Power-Down Register to 1. The selected DAC output is buffered, then fed to the ATO pin. A measurement return pin ATRN is also provided. The ATO pin voltage is not a direct measure of the DAC output, so it cannot be used to measure the absolute value of the DAC output. The intention of the test point is to check DAC functionality and monotonicity. (The last register with DAC sent to serial port). The following DAC's functionality can be measured at ATO: FC (filter cutoff frequency), FB (filter boost), VD (Viterbi threshold), LDP (level positive threshold), LDN (level negative threshold), IDR (data rate), WP (write precomp), and DRC (damping ratio).

Diagnostic/Optimization Test Modes

Some disk drive diagnostic tests and operating optimization could be performed by observing the equalizer and AGC control voltages and measuring their change with different conditions. For example, the equalizer control voltage ("0" sample values) is affected by the continuous time filter/equalizer setting, the head flying height, and the head gap length. The AGC control voltage ("1" sample values) are also affected by the previously mentioned factors and by magnetic non-linearities. The effectiveness of write precomp compensating the non-linearities could be evaluated by observing the AGC control voltage difference of a maximum transition di-bit pattern with a pattern with minimum transitions.

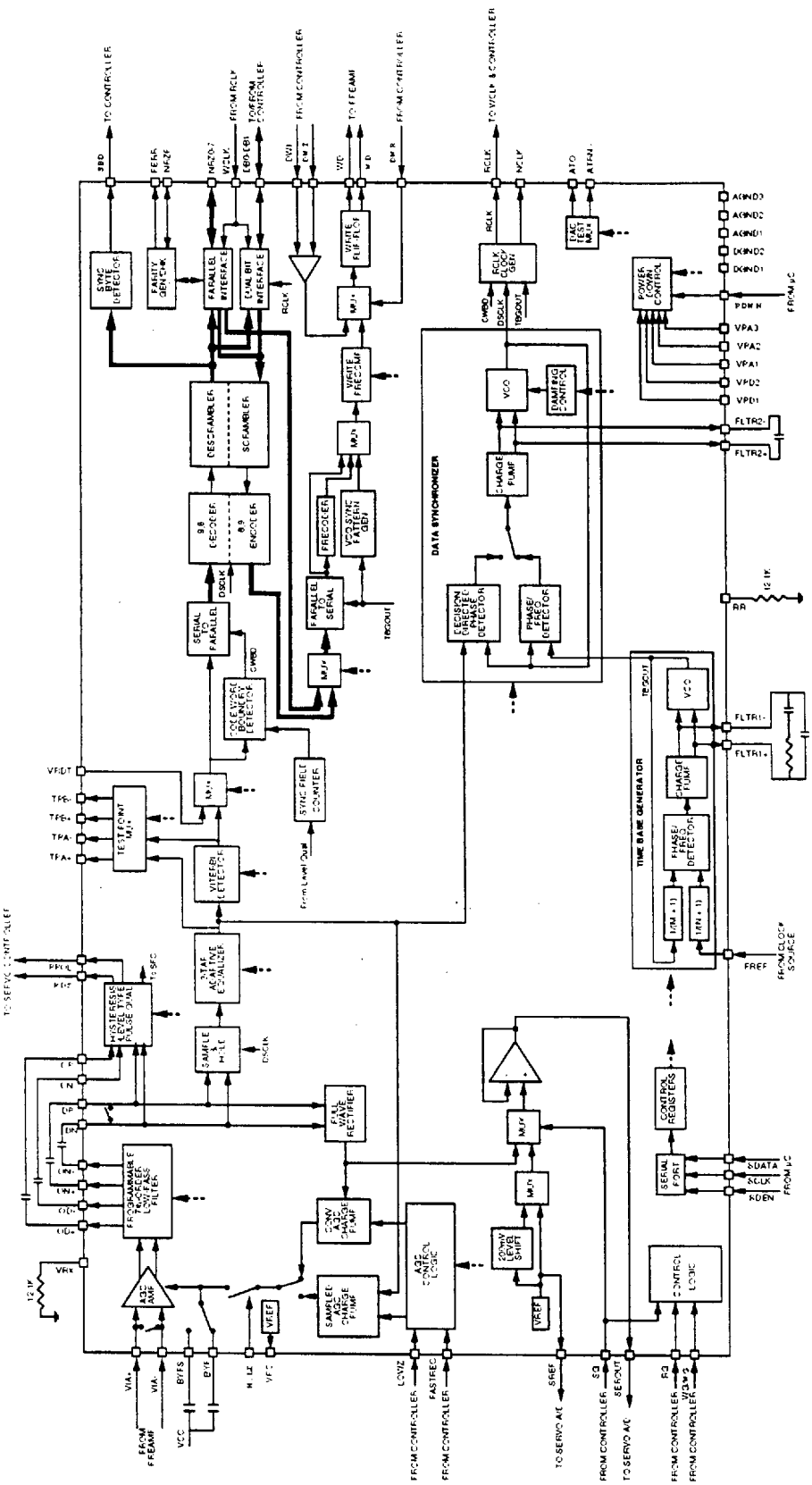
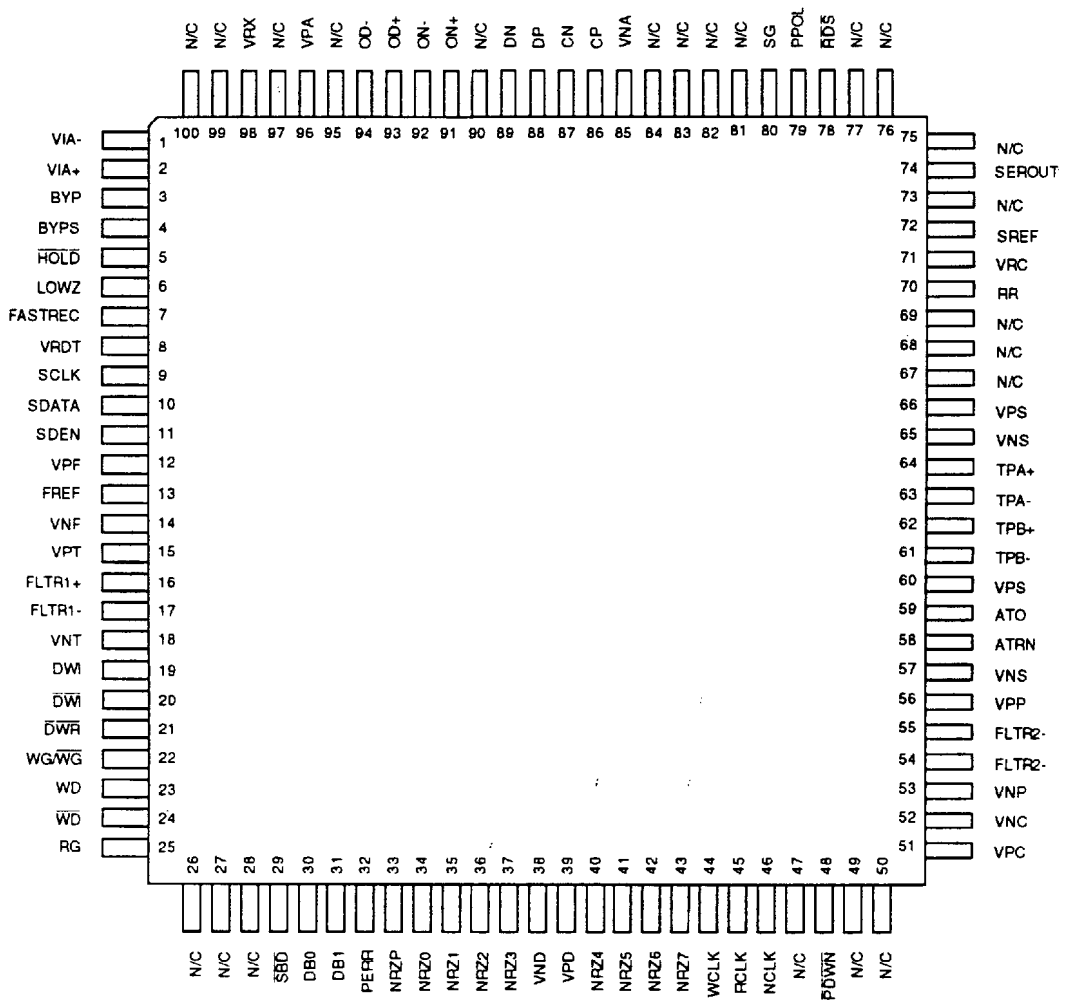


FIGURE 10: SSI 32P4904 Application Diagram

SSI 32P4904
PRML Read Channel with
PR4, 8/9 ENDEC, FWR Servo

PACKAGE PIN DESIGNATIONS
(Top View)

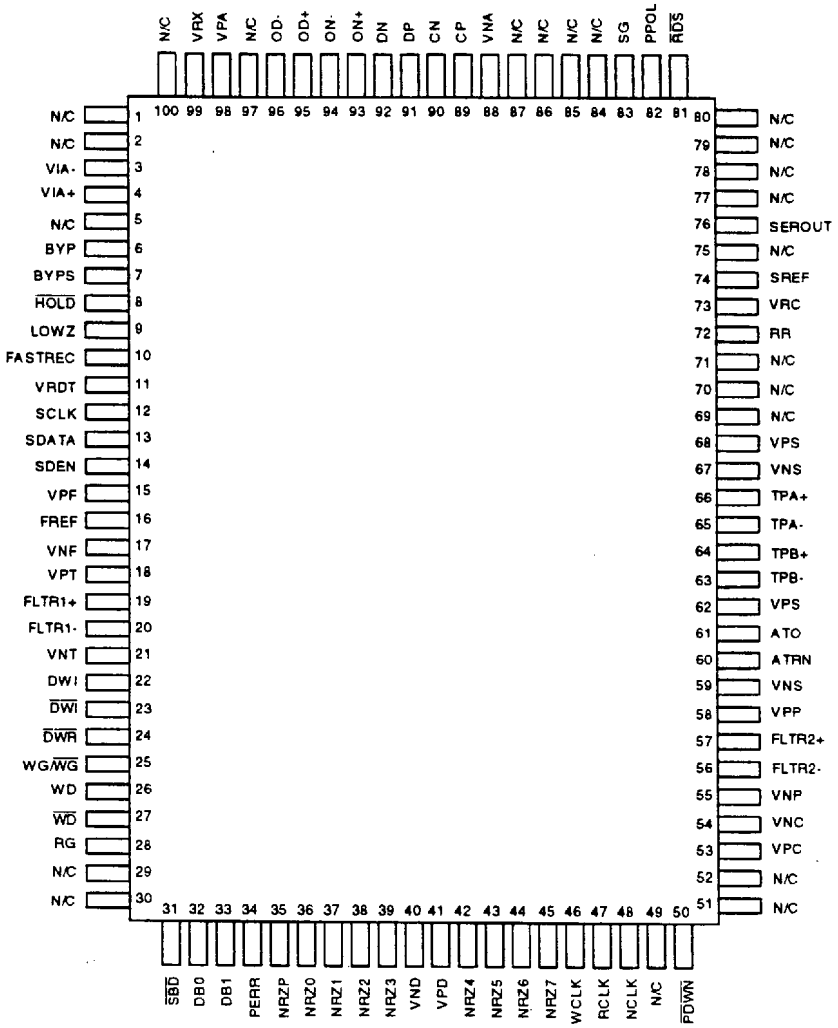


100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32P4904
PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

PACKAGE PIN DESIGNATIONS
(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P4904	100-Lead TQFP	32P4904-CGT	32P4904-CGT
	100-Lead QFP	32P4904-CG	32P4904-CG

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