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SSI 32P541B
Read Data Processor

T-52-38

July 1991

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DESCRIPTION

The SSI 32P541B is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

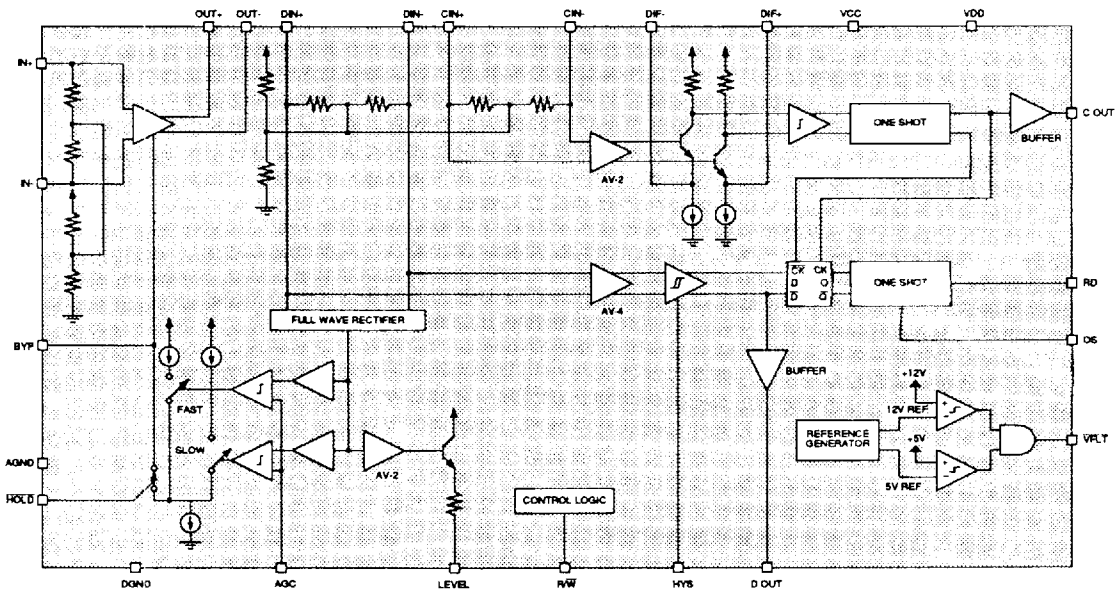
In read mode the SSI 32P541B provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P541B requires +5V and +12V power supplies and is available in a 28-pin PLCC, 24-pin DIP and 24-pin SOL.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard 12V ± 10% and 5V ± 10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **Internal voltage fault indicator**
- **≤ ±1.0 ns pulse pairing**
- **24 Mb/s operation**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp -\left(\frac{V2 - Vt}{5.8 + Vt}\right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

HYSTERESIS LEVEL

In level qualification, hysteresis comparator eliminates errors due to low level additive noise, see Figure 4B.

The 32P541B allows two implementations of hysteresis: fixed hysteresis threshold or DIN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by a setting a DC voltage at HYS pin, such as from a resistor divider from VCC to GND. The hysteresis threshold at the comparator can be computed as: Hysteresis Gain x V_{HYS}. For high performance system application, however, fixed hysteresis threshold is not recommended.

DIN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DIN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the HYS pin (see Figure 4b). The LEVEL output, amplified peak capture of DIN voltage, can be computed as: Level Gain x V(DIN+ - DIN-). With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The hysteresis threshold, as a function of DIN, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x V(DIN+ - DIN-). For a typical case of 1 Vpp differential at DIN± input, assume equal value resistors in the divider network, the hysteresis threshold is 1.95 x 0.50 x 0.19 x 1V = 0.185V. This represents 37% hysteresis on a 1 Vpp signal. While both the Level Gain and Hysteresis threshold vs. HYS bear a moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DIN tracking hysteresis threshold is specified as the Tracking Hysteresis Threshold Tolerance in the specification.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D-type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:
Where: C = external capacitor (20 pF to 150 pF)

$$AV = \frac{-2000Cs}{LCs^2 + (R+92)Cs + 1}$$

L = external inductor

R = external resistor

$s = j\omega = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip-flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541B and read/write preamplifier, such as the SSI 32R512.

Internal SSI 32P541B timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P541B is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541B and associated circuitry grounds from other circuits on the disk drive PCB.

LOW VOLTAGE FAULT DETECTION

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low when either supply drops below their trip point. This option is available only in the 28-pin PLCC package.

TABLE 1: Mode Control

R/$\overline{W}$	$\overline{HOLD}$	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC		5 volt power supply
VDD		12 volt power supply
AGND, DGND		Analog and Digital ground pins
R/$\overline{W}$	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-		Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS		Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output
$\overline{VFLT}$*	O	Open collector output that goes low when a low power supply fault is detected.

*$\overline{VFLT}$ output offered in 28-pin PLCC package only.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$, $\overline{VFLT}$	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

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POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			850	mW

LOGIC SIGNALS

VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5K		Ω
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ pin high		1.8		kΩ
(both sides)	R/$\overline{W}$ pin low		0.25		kΩ
Minimum Gain Range	1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Bandwidth	Gain set to maximum -3 dB point		30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage		3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND		±3.2			mA
Output Resistance			12		32	Ω
Output Capacitance					15	pF
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp ≤ V(IN+ – IN-) ≤ 550 mVpp;	@ 2.5 MHz	0.33		0.43	Vpp/V
		@ 9 MHz	0.44		0.69	Vpp/V
	0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp					
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-) ≤ 550 mVpp AGC Fixed, over supply & temp.	@ 2.5 MHz			4	%
		@ 9 MHz			12	%
		@ 9 MHz Cold			14	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a			50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b			4		µs
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V		1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge		0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$			1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode			4.5		µA
	Hold Mode		-0.2		+0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.		40			dB
PSRR (Input Referred)	ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max.		30			dB
Maximum AGC Amplifier Output Offset Variation	V(IN+ - IN-) = 0 Min to max gain				200	mV

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HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	kΩ
Differential Input Capacitance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 kΩ across DIN+, DIN-			10	mV
Hysteresis Gain (see figure 4c)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16	0.19	0.22	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Tracking Hysteresis Threshold Tolerance	V (Hys) = some % of *V (AGC) or V (LEVEL) 1V < V (Hys) < 3V; f = 0-9 MHz	-15		+15	% Peak
Level Gain (see figure 4d)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp, 10 kΩ from LEVEL pin to GND	1.7	1.95	2.2	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

*In an open loop configuration where reference is V(AGC) tolerance can be slightly higher

ACTIVE DIFFERENTIATOR

Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled sine wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 33 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 11.4 ns + 740 • Cos 50% - 50% 15 pF ≤ Cos ≤ 150 pF			±15	%
Pulse Pairing	|Td3 - Td4|			±1.0	ns
Output Rise Time	From 0.4V to 2.4V level			15	ns
Output Fall Time	From 0.4V to 2.4V level			9	ns

SUPPLY VOLTAGE FAULT DETECTION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Fault Threshold		9.1		10.3	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low Voltage	4.5 < VCC < 5.5V, IOL = 1.6 mA			0.4	V
	1.0 < VCC < 4.5V, IOL = 0.5 mA			0.4	V
IOH Output High Current				25	µA

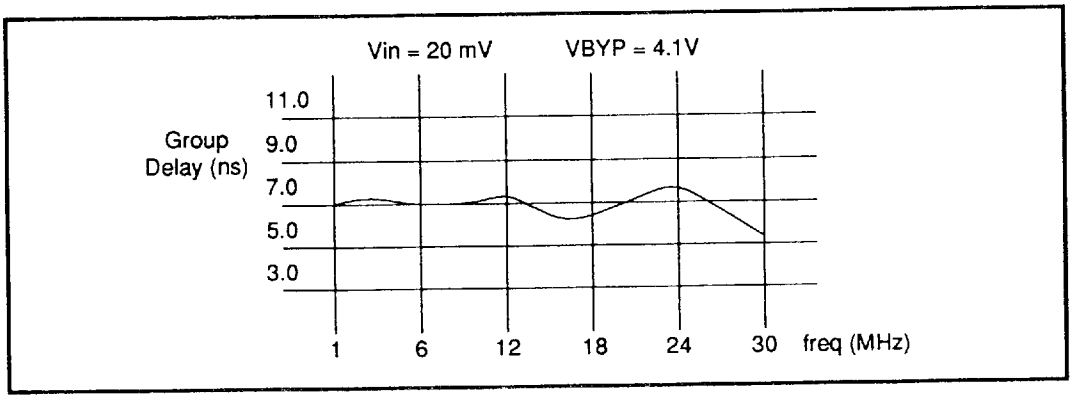


FIGURE 1: AGC Amplifier - Typical Group Delay Variation

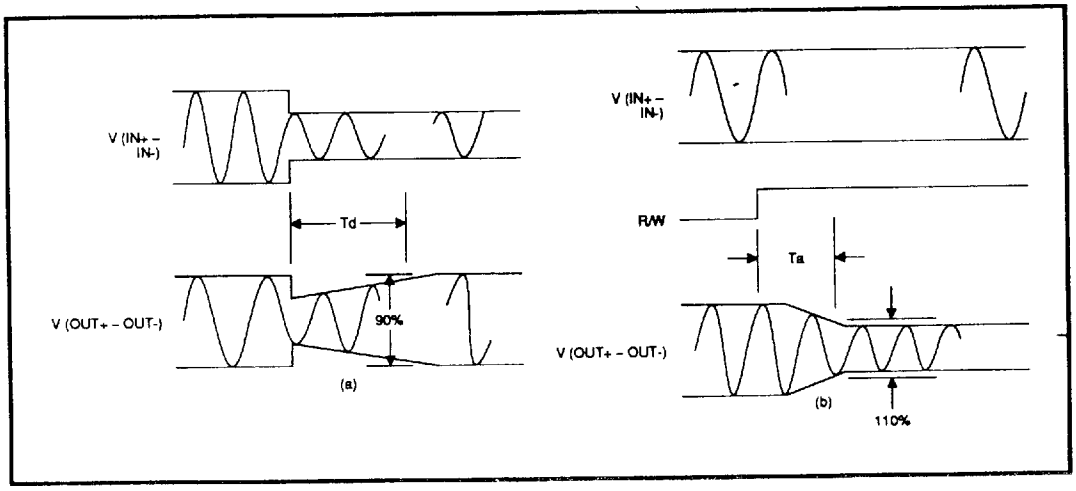


FIGURE 1(a), (b): AGC Timing Diagrams

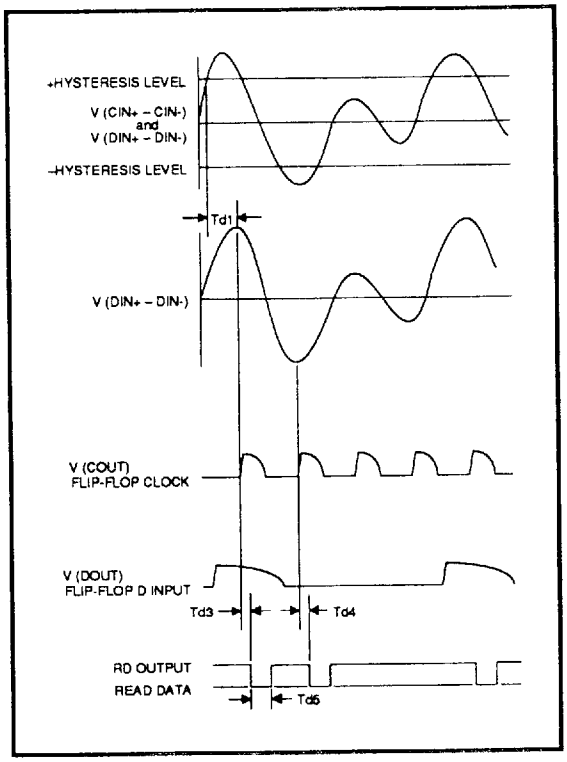
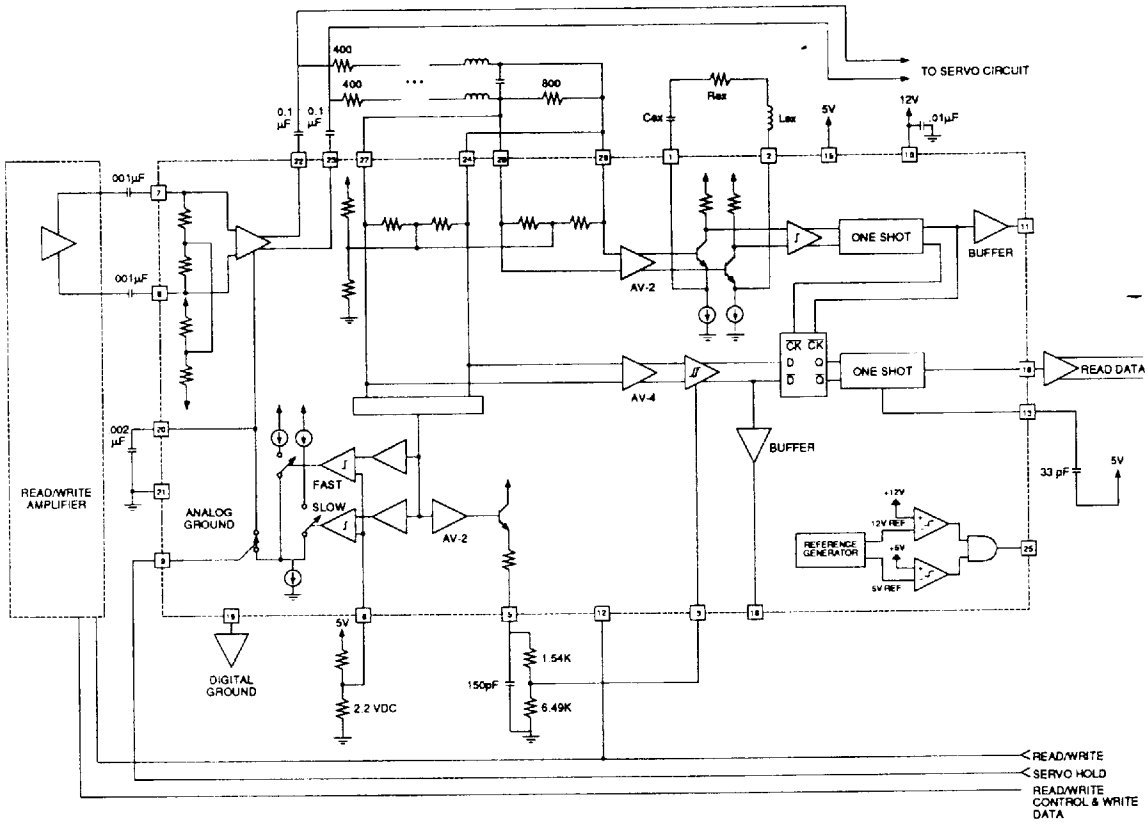


FIGURE 2: Timing Diagram



NOTE: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.
Component values, where given, are for a 24 Mbit/s System.
Above pin numbers are for the 28-pin PLCC package.

FIGURE 3: Typical Read/Write Electronics Set Up

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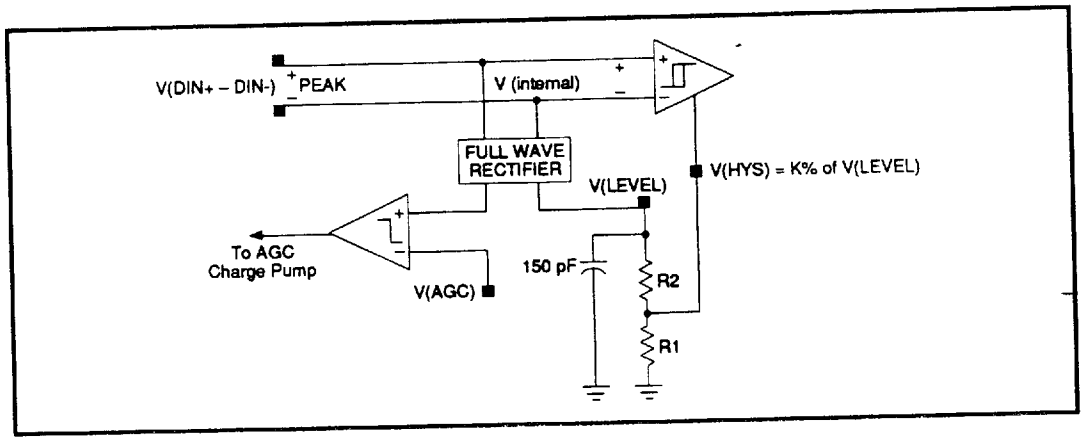

FIGURE 4a: Feed Forward Mode

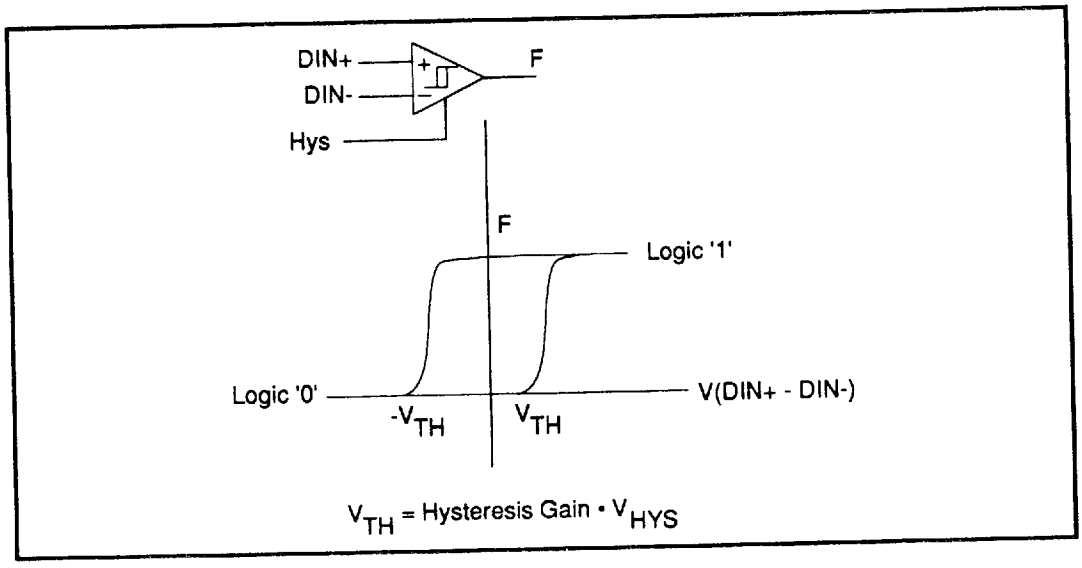

FIGURE 4b: Hysteresis Comparator Transfer Function

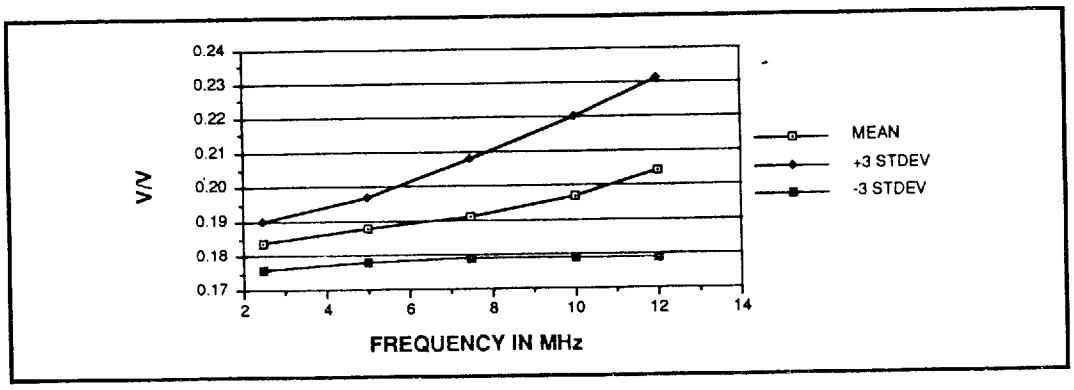

FIGURE 4c: Hysteresis Gain

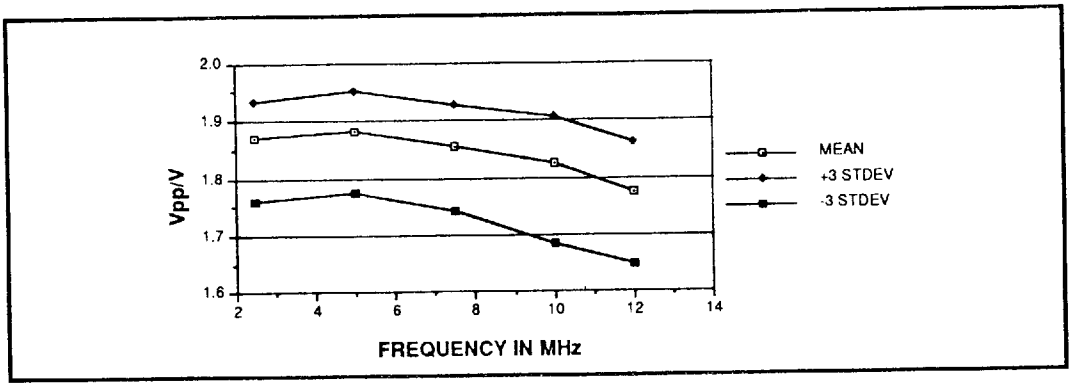

FIGURE 4d: Level Gain

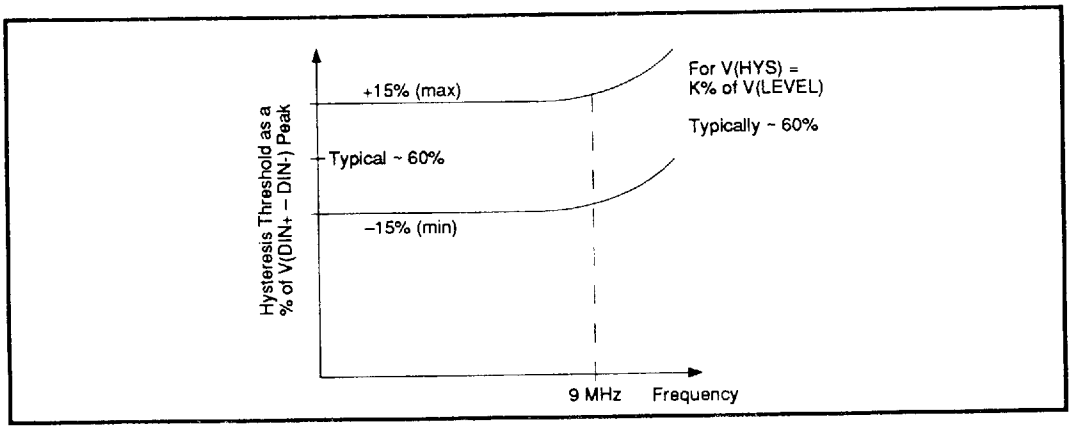

FIGURE 5: Percentage Threshold Versus Frequency

SSI 32P541B
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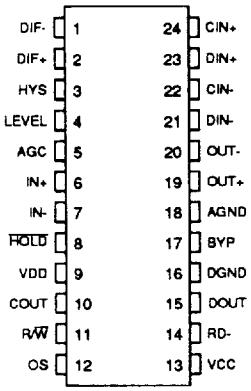
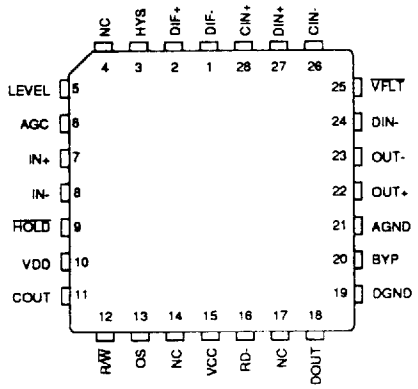
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: Ø ja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P541B Read Data Processor		
24-Lead PDIP	SSI 32P541B-P	SSI 32P541B-P
28-Lead PLCC	SSI 32P541B-CH	SSI 32P541B-CH
24-Lead SOL	SSI 32P541B-CL	SSI 32P541B-CL

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