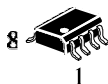
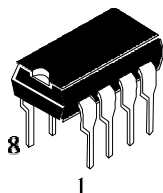


Description

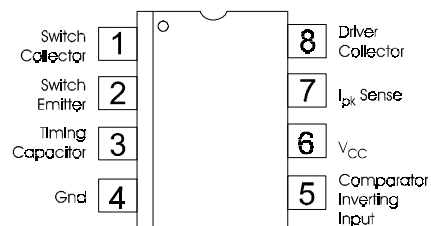
The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

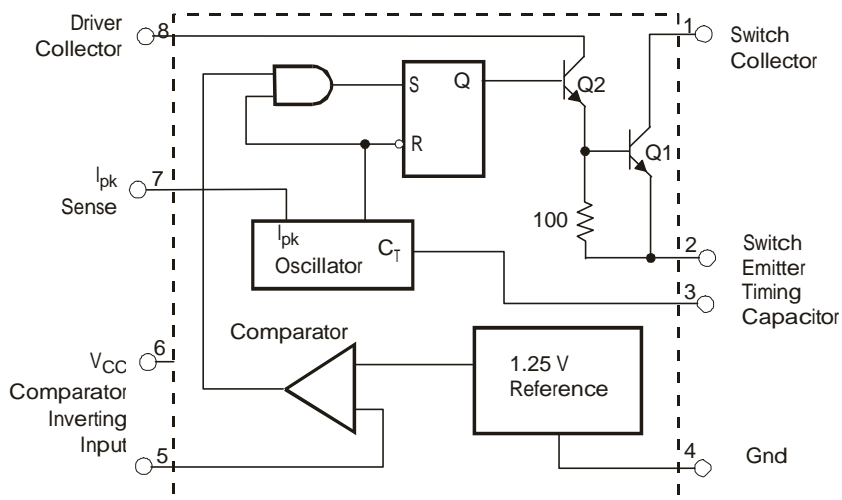


Plastic Package



Pin Connections

Internal Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Maximum	Units
V_{CC}	Power Supply Voltage	40	Vdc
V_{IR}	Comparator Input Voltage Range	-0.3 to +40	Vdc
$V_{C(switch)}$	Switch Collector Voltage	40	Vdc
$V_{E(switch)}$	Switch Emitter Voltage ($V_{PIN1} = 40\text{ V}$)	40	Vdc
$V_{CE(switch)}$	Switch Collector to Emitter Voltage	40	Vdc
$V_{C(driver)}$	Driver Collector Voltage	40	Vdc
$I_{C(driver)}$	Driver Collector Current (Note 1)	100	mA
I_{SW}	Switch Current	1.5	A
T_J	Operating Junction Temperature	+150	°C
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

Electrical Characteristics

($V_{CC}=5.0V$, $T_A=T_{low}$ to T_{high} , unless otherwise)

Characteristics	Symbol	Min	Typ	Max	Units
OSCILLATOR					
Frequency ($V_{pin5} = 0V$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0V$ to $40V$, $T_A = 25^\circ\text{C}$)	I_{chg}	24	35	42	μA
Discharge Current ($V_{CC} = 5.0V$ to $40V$, $T_A = 25^\circ\text{C}$)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25^\circ\text{C}$)	I_{dischg} / I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$)	$V_{ipk(sence)}$	250	300	350	mV
OUTPUT SWITCH (NOTE 2)					
Saturation Voltage, Darlington Connection ($I_{SW} = 1.0\text{ A}$, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection ($I_{SW} = 1.0\text{ A}$, $R_{pin8} = 82\Omega$ to V_{CC} , Forced $\beta \approx 20$)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain ($I_{SW} = 1.0\text{ A}$, $V_{CE} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	h_{FE}	50	75	–	–
Collector Off-State Current ($V_{CE} = 40\text{ V}$)	$I_{C(off)}$	–	40	100	μA
COMPARATOR					
Threshold Voltage ($T_A=25^\circ\text{C}$) ($T_A=T_{low}$ to T_{high})	V_{th}	1.225 1.21	1.25 –	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC}=3.0\text{ V}$ to 40 V)	Reg_{line}	–	1.4	5.0	mV
Input Bias Current ($V_{in}=0\text{ V}$)	I_{IB}	–	-20	-400	nA
TOTAL DEVICE					
Supply Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{pin5} > V_{th}$, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES : 1. Maximum package power dissipation limits must be observed.

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible

Typical Performance Characteristics

Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

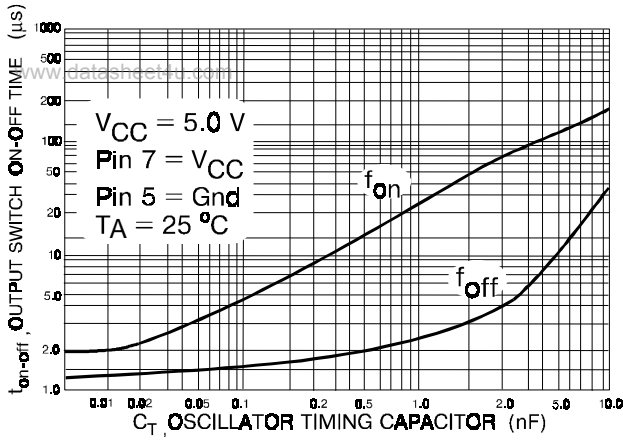


Figure 2. Timing Capacitor Waveform

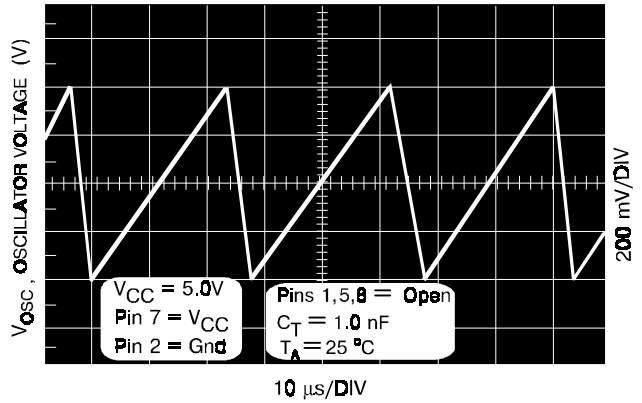


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current versus

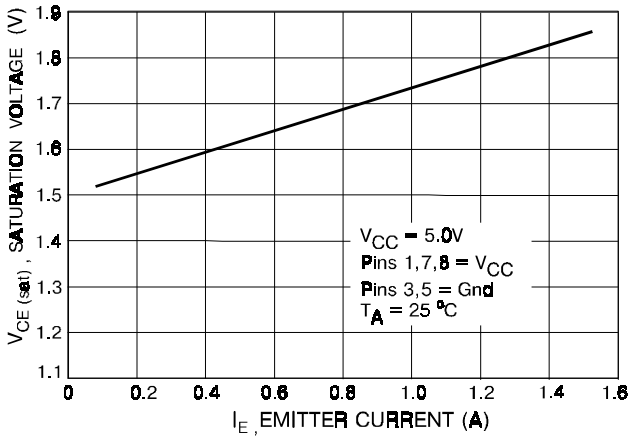


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus

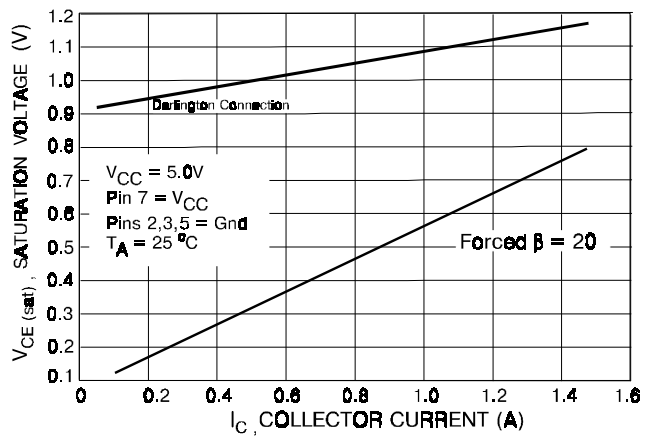


Figure 5. Current Limit Sense Voltage versus Temperature

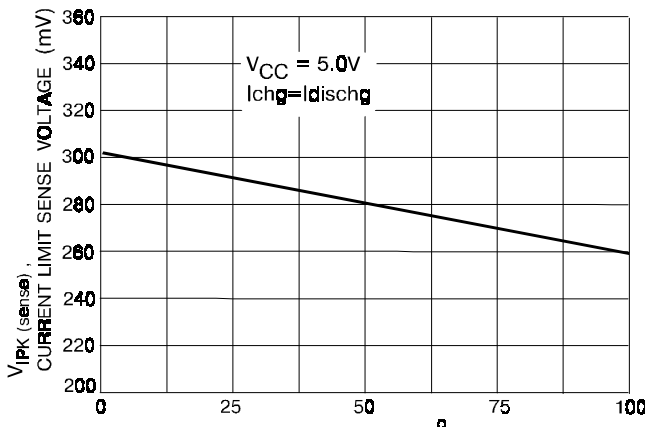
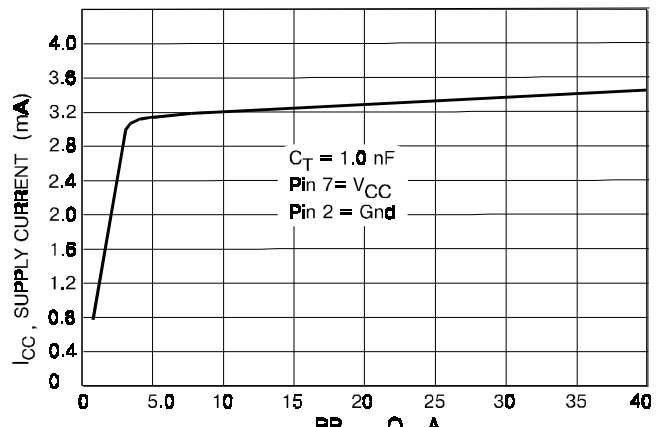


Figure 6. Standby Supply Current versus Supply Voltage



Typical Applications Circuit

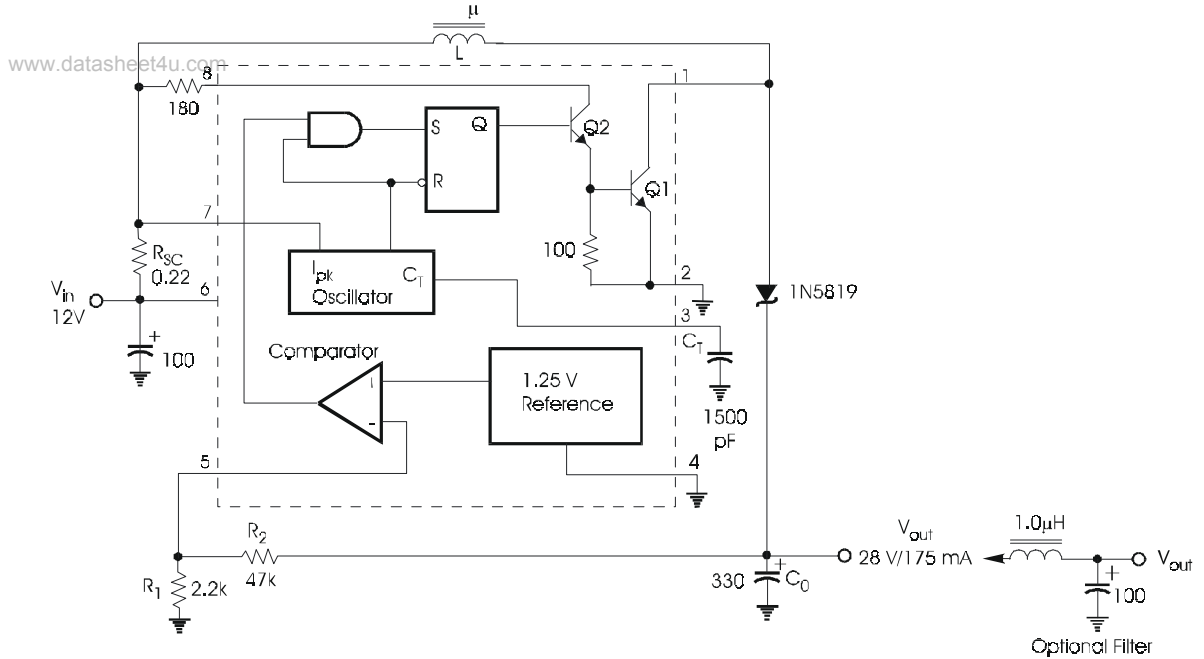


Figure 1. Step-Up Converter

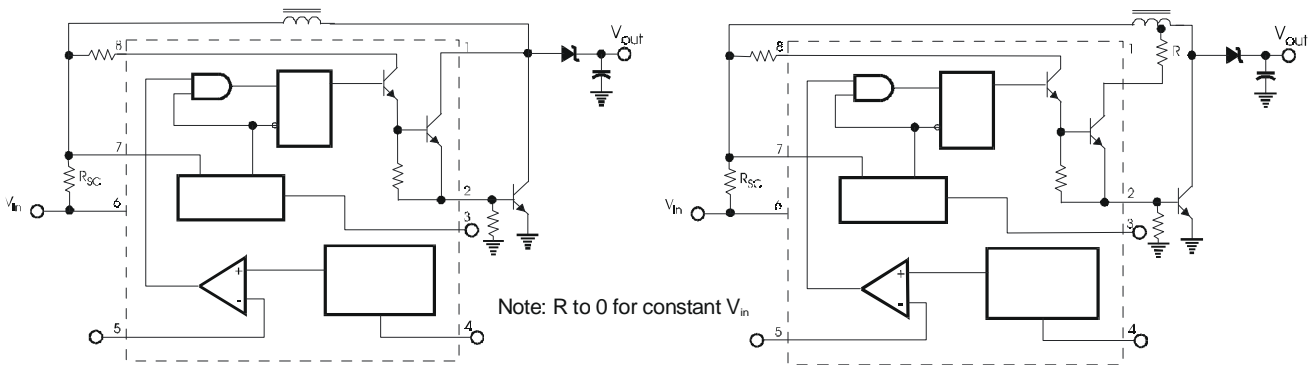


Figure 2a. External NPN Switch.

Figure 2b. External NPN Saturated Switch.

Figure 2. External Current Boost Connections for Load Current Greater than 100mA

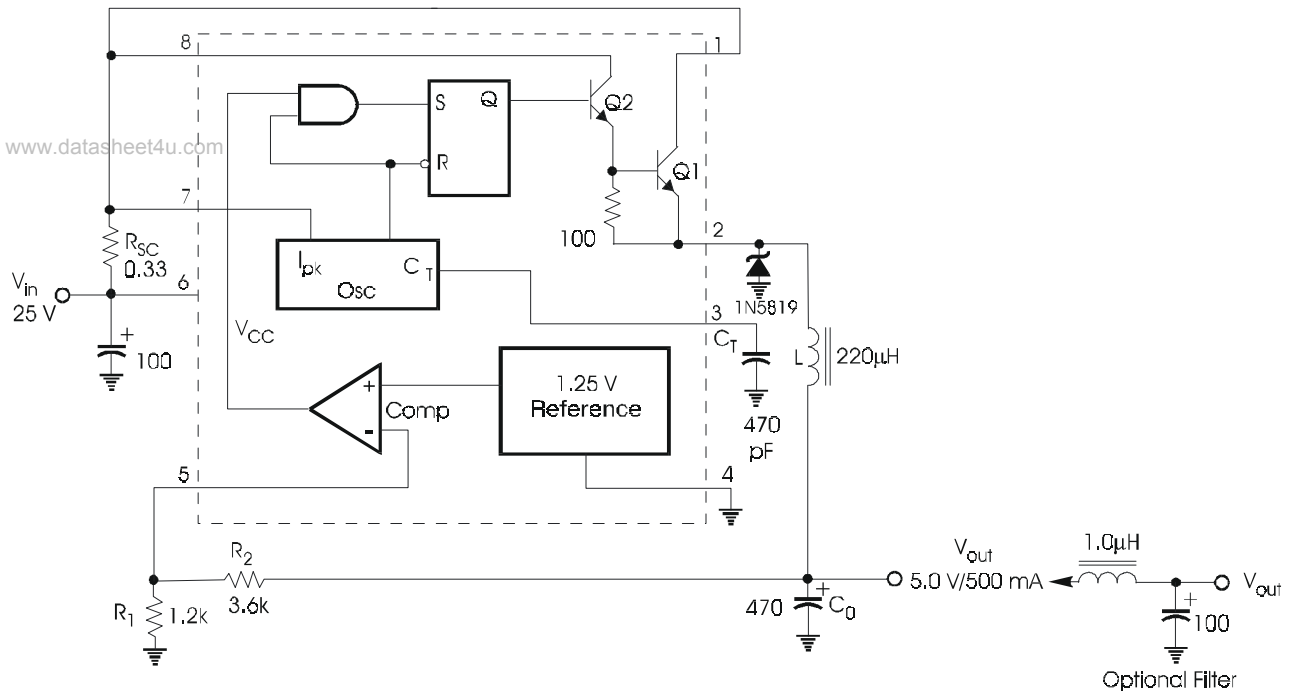


Figure 3. Step-Down Converter

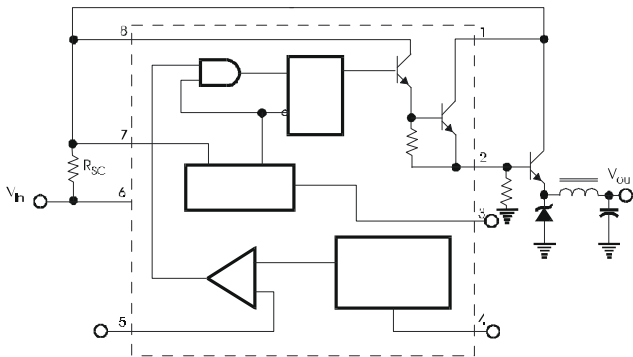


Figure 4a. External NPN Switch.

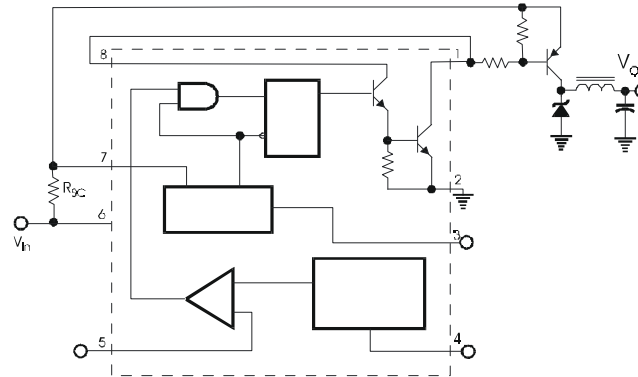


Figure 4b. External PNP Saturated Switch.

Figure 4. External Current Boost Connections for Peak Greater than

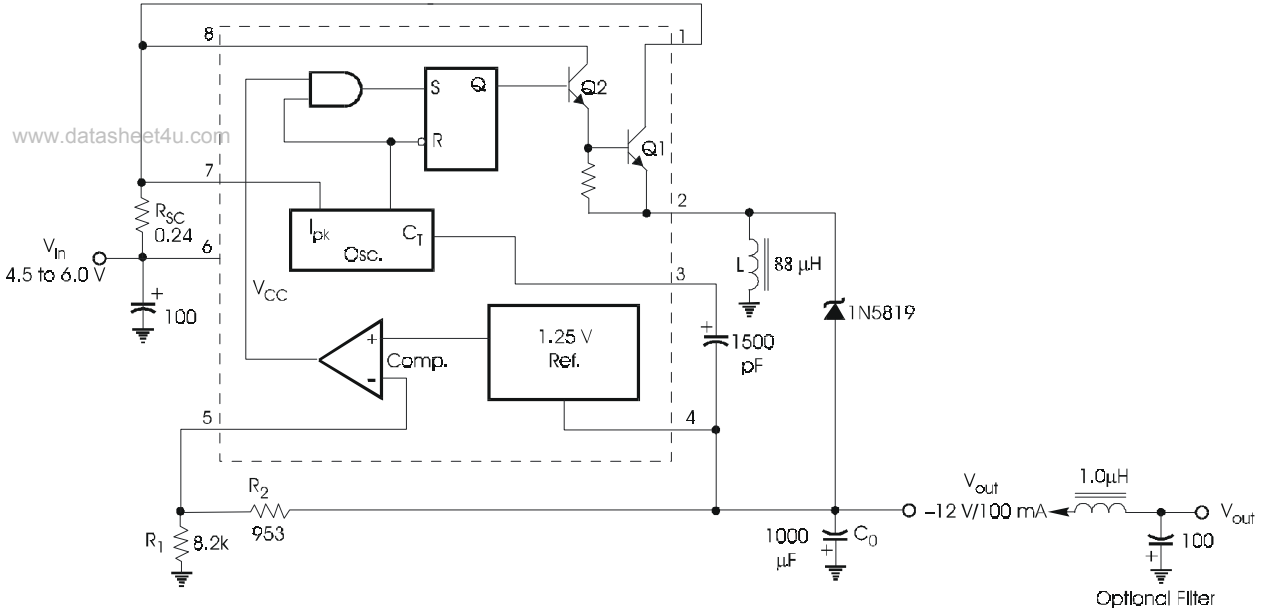


Figure 5. Voltage Inverting Converter

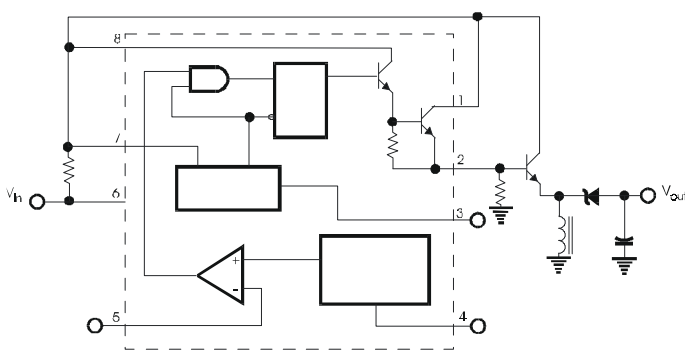


Figure 6a. External NPN Switch.

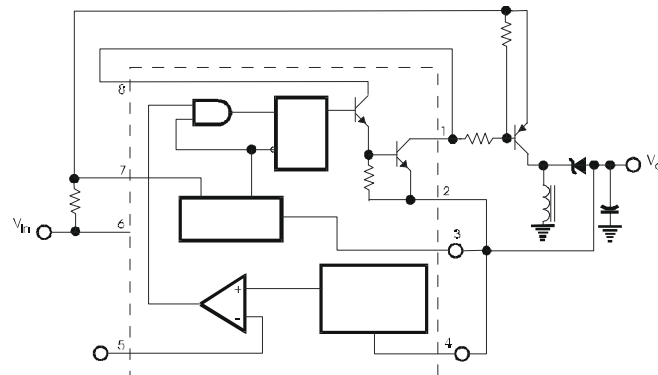


Figure 6b. External PNP Saturated Switch.

Figure 6. External Current Boost Connections for Load Current Greater than

Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off} <small>www.datasheet4u.com</small>	$\frac{V_{in} - V_{sat}}{V_{sat}} \times \frac{I_{out}}{I_{pk(switch)}}$	$\frac{V_{in} - V_{sat}}{V_{sat}} \times \frac{I_{out}}{I_{pk(switch)}}$	$\frac{V_{in} - V_{sat}}{V_{sat}} \times \frac{I_{out}}{I_{pk(switch)}}$
$(t_{on}+t_{off})_{max}$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	4.0×10^{-5}
$I_{pk(switch)}$	$2 I_{out(max)} + I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} + I_{pk(switch)}$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\frac{V_{in} - V_{sat}}{I_{pk(switch)}} \times t_{on(max)}$	$\frac{V_{in} - V_{sat}}{I_{pk(switch)}} \times t_{on(max)}$	$\frac{V_{in} - V_{sat}}{I_{pk(switch)}} \times t_{on(max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$9 \frac{I_{pk(switch)} t_{on}}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

TERMS AND DEFINITIONS

V_{sat} - Saturation voltage of the output switch.

V_F - Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

$$|V_{out}| = 1.25 \frac{R}{R}$$

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage,

I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_{out} .

$V_{ripple(pp)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Ordering Information

ORDERING NUMBER	PACKAGE	MARKING
34063A	SOP-8/DIP-8	MC34063A

Address : 北京市海淀区永定路 88 号长银大厦 6A06--6A07

Rm 6A07,Changyin Office Building ,No.88,Yong Ding Road,Hai Dian District ,Beijing

Postalcode:100039

Tel: 86-010-58895780 / 81 / 82 / 83 / 84 Fax : 010-58895793

Http://www.estek.com.cn

Email:sales@estek.com.cn

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