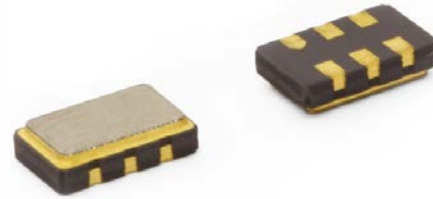


# Model 345

## HFF LVPECL VCXO

### Features

- Ceramic Surface Mount Package
- Ultra-Low Phase Jitter Performance
- High Frequency Fundamental Crystal Design
- Frequency Range 100 – 250MHz \*
- +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:  
5.0 × 3.2 × 1.2mm • 62.28mg

### Applications

- Small Cells
- Wireless Communication
- Broadband Access
- SONET/SDH/DWDM
- Base Stations
- Ethernet/GbE/SyncE
- Digital Video
- Test and Measurement

#### Standard Frequencies

- 100.00MHz
- 122.88MHz
- 125.00MHz
- 153.60MHz
- 155.52MHz
- 156.25MHz
- 160.00MHz
- 166.00MHz
- 200.00MHz
- 204.80MHz
- 240.00MHz
- 245.76MHz

\* Check factory for availability of frequencies not listed.

### Description

CTS Model 345 is a low cost, small size, high performance VCXO. Employing the latest IC technology, coupled with a high frequency fundamental crystal, M345 has excellent stability and low jitter/phase noise performance.

### Ordering Information

Model	Supply Voltage	Absolute Pull Range	Frequency Stability	Temperature Range	Frequency Code [MHz]	Packaging
345	L	B	3	I	XXX or XXXX	T
	Code Voltage L +3.3V ±5%	Code APR B ±50ppm <sup>3</sup>	Code Stability 5 ±25ppm <sup>1</sup> 4 ±30ppm 3 ±50ppm	Code Temp. Range C -20°C to +70°C I -40°C to +85°C	Code Frequency Product Frequency Code <sup>2</sup>	Code Packing T 1k pcs./reel

Notes:

- 1] Check factory availability with "I" temperature range.
- 2] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 3] Frequencies ≥200MHz, APR is ±30ppm.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.

## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.3	-	5.0	V
Maximum Control Voltage	$V_C$	-	-0.5	-	$V_{CC}$	V
Supply Voltage	$V_{CC}$	±5%	3.14	3.3	3.47	V
Supply Current	$I_{CC}$	Typical @ LVPECL Load, $T_A = +25^\circ\text{C}$	-	65	80	mA
Output Load	$R_L$	Terminated to $V_{CC} - 2.0\text{V}$	-	50	-	Ohms
Operating Temperature	$T_A$	-	-20 -40	+25	+70 +85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-	-40	-	+100	$^\circ\text{C}$

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	$f_O$	-		100 - 250		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	±25ppm stability, -20 $^\circ\text{C}$ to +70 $^\circ\text{C}$ only		25, 30 or 50		±ppm
Absolute Pull Range [Note 2]	APR	Frequencies <200MHz	50	-	-	±ppm
	APR	Frequencies ≥200MHz	30	-	-	±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25 $^\circ\text{C}$ , nominal $V_{CC}$ and $V_C$	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

2.] Minimum guaranteed frequency shift from  $f_O$  over variations in temperature, aging, power supply and load.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Voltage Levels	$V_{OH}$	LVPECL Load, -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	$V_{OL}$	LVPECL Load, -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	V
Output Duty Cycle	SYM	@ $V_{CC} - 1.3\text{V}$	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels	-	0.3	1.0	ns
Start Up Time	$T_S$	Application of $V_{CC}$	-	5	10	ms
Enable Function						
Enable Input Voltage	$V_{IH}$	Pin 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Standby Current	$I_{STB}$	Pin 2 Logic '0', Output Standby	-	-	10	μA
Enable Time	$T_{PLZ}$	Pin 2 Logic '1'	-	-	20	μs
Phase Jitter, RMS	$t_{jrms}$	Bandwidth 12kHz - 20MHz	-	90	200	fs
Phase Noise	-	See Typical Plots	-	-	-	-

### Enable Truth Table

Pin 2	Pin 4 & 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

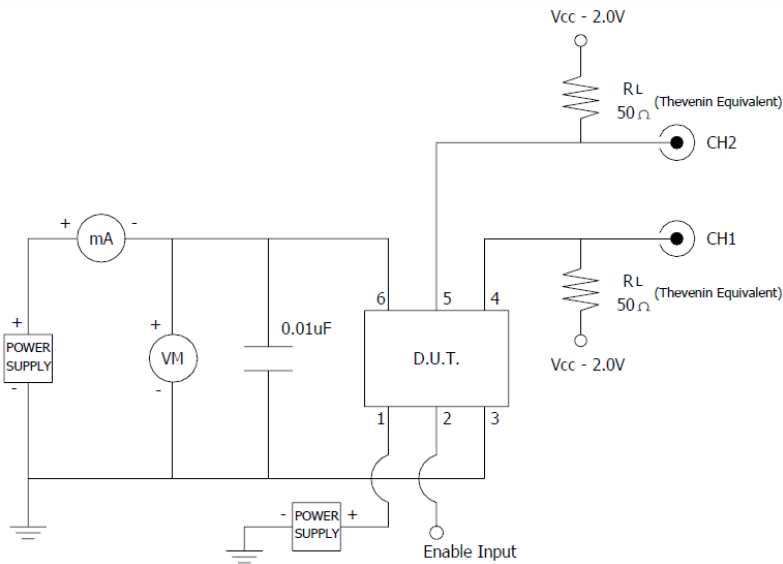
## Electrical Specifications

### Control Voltage

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Control Voltage	$V_C$	-	0.00	1.65	3.30	V
Frequency Deviation	$\Delta f/f_0$	$V_C = 0.0V$ $V_C = 3.3V$		-155 to -75 75 to 155		ppm
Linearity	L	Best Straight Line Fit	-	5	10	%
Gain Transfer	$K_V$	Pull Sensitivity; @ +1.65V, +25°C	-	75	-	ppm/V
Input Impedance	$Z_{Vc}$	-	10	-	-	MOhms
Modulation Roll-off	-	@ -3dB	25	-	-	kHz
Transfer Function	-	-		Positive		-

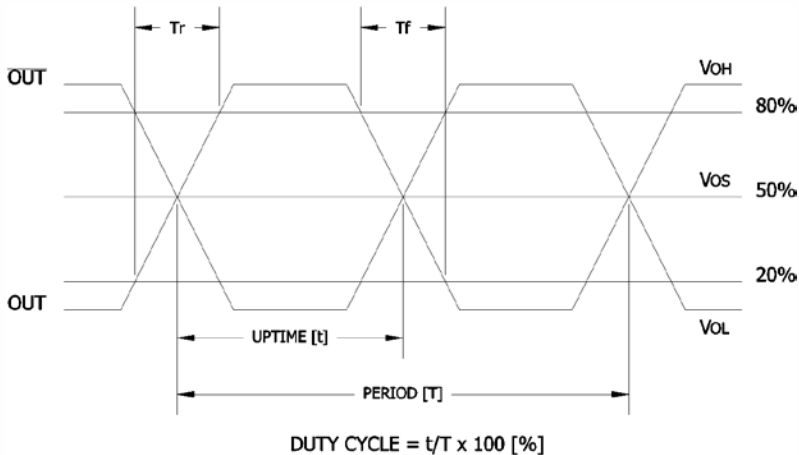
### Test Circuit

LVPECL



### Output Waveform

LVPECL

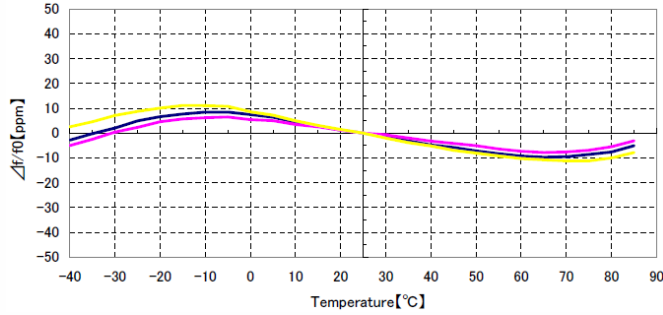


## Electrical Specifications

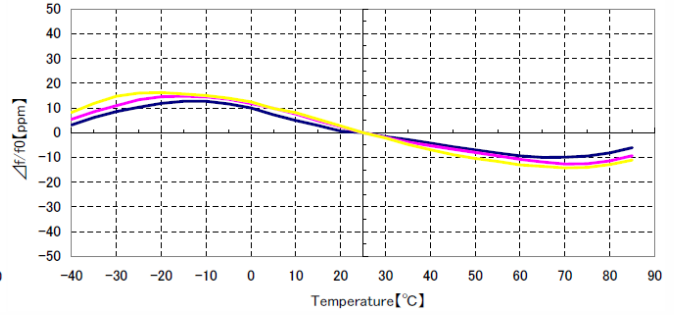
### Performance Data

#### Frequency Deviation – Over Temperature [typical]

122.88MHz,  $V_{CC} = 3.3V$ ,  $V_C = 1.65V$



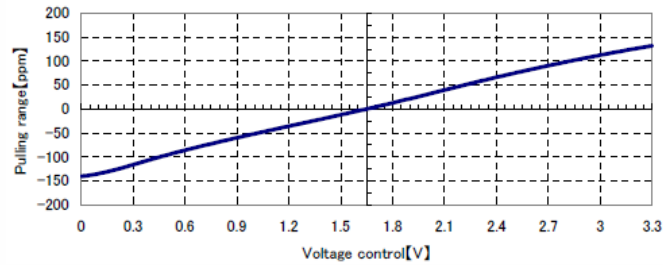
156.25MHz,  $V_{CC} = 3.3V$ ,  $V_C = 1.65V$



#### Frequency Deviation – Pulling Range [typical]

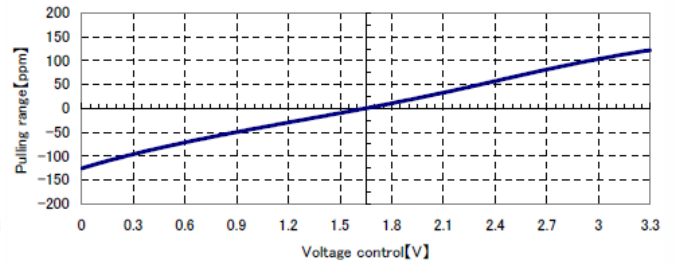
122.88MHz,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ V$

*Pulling range*



156.25MHz,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ V$

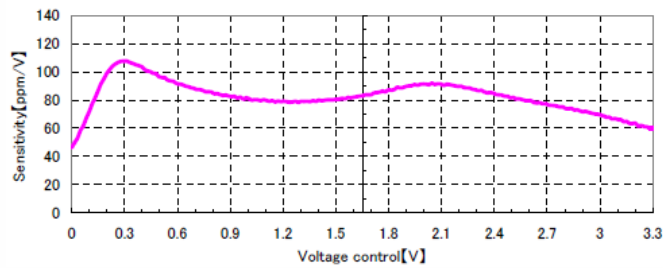
*Pulling range*



#### Frequency Deviation – Gain Transfer [typical]

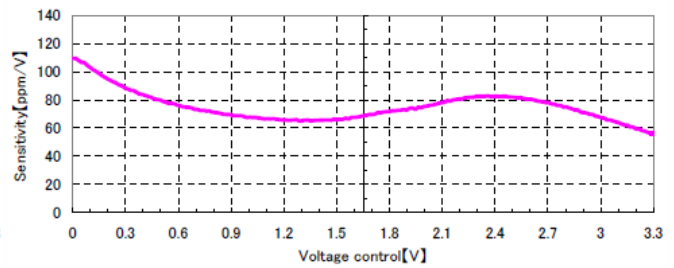
122.88MHz,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ V$

*Sensitivity*



156.25MHz,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ V$

*Sensitivity*

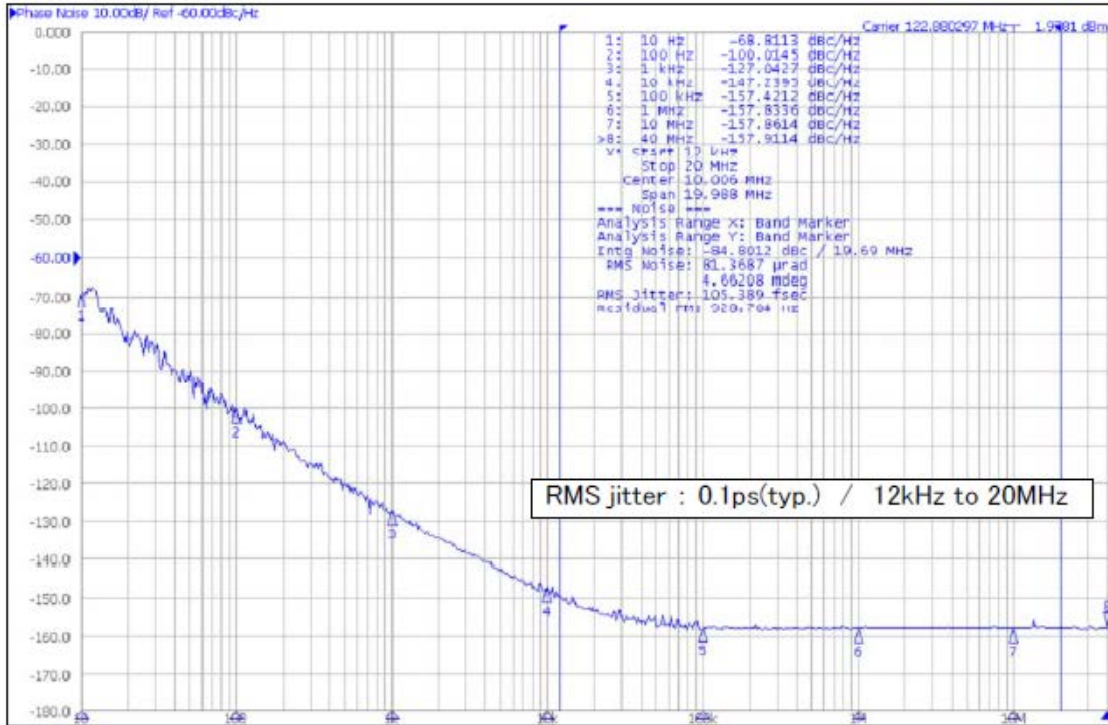


### Electrical Specifications

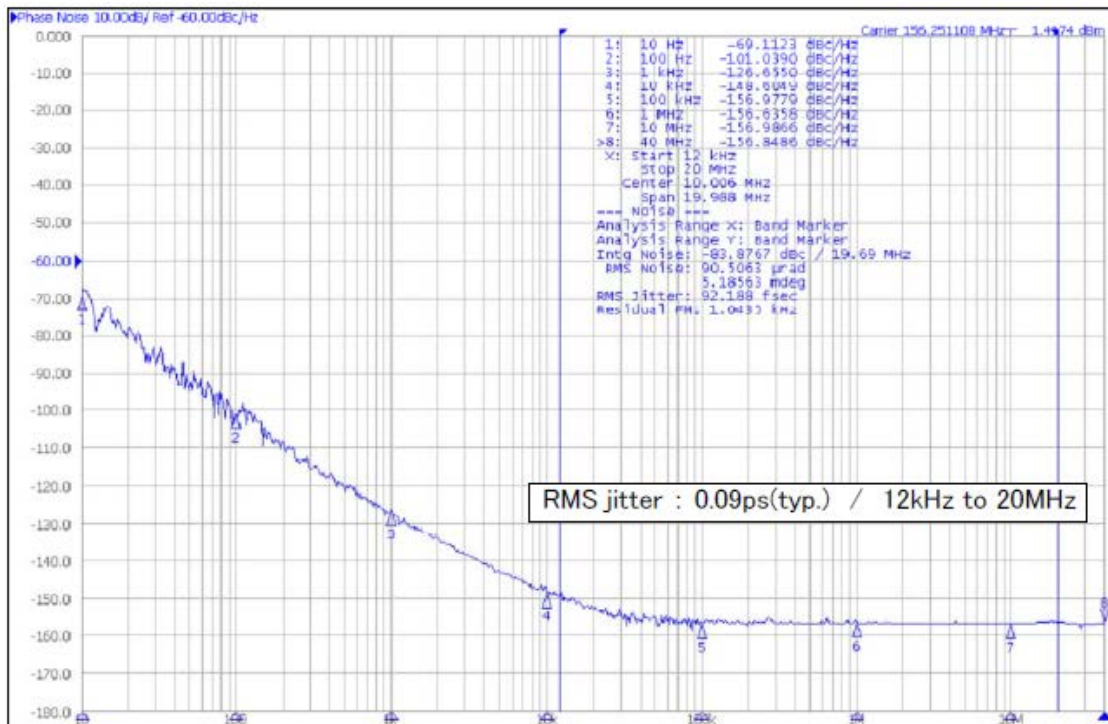
#### Performance Data

##### Phase Noise [typical]

122.88MHz,  $V_{CC} = 3.3V$ ,  $V_C = 1.65V$ ,  $T_A = +25^\circ C$

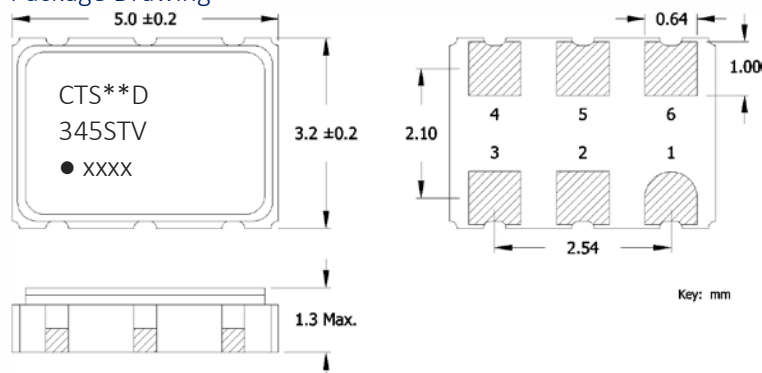


156.25MHz,  $V_{CC} = 3.3V$ ,  $V_C = 1.65V$ ,  $T_A = +25^\circ C$



## Mechanical Specifications

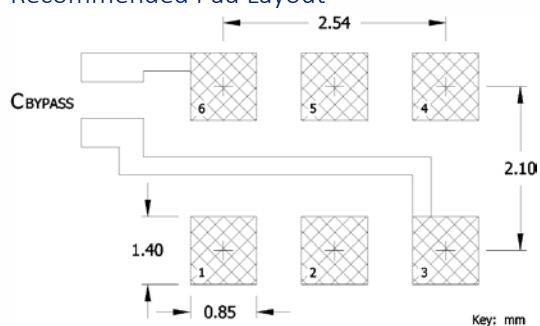
### Package Drawing



### Marking Information

- \*\* - Manufacturing Site Code.
- D - Date Code. See Table I for codes.
- ST - Frequency Stability/Temperature Code. [Refer to Ordering Information]
- V - Voltage Code. L = 3.3V
- xxxx - Frequency Code. 4-digits required for frequencies 100MHz and above. [See document 016-1454-0, Frequency Code Tables.]

### Recommended Pad Layout



### Notes

- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

### Pin Assignments

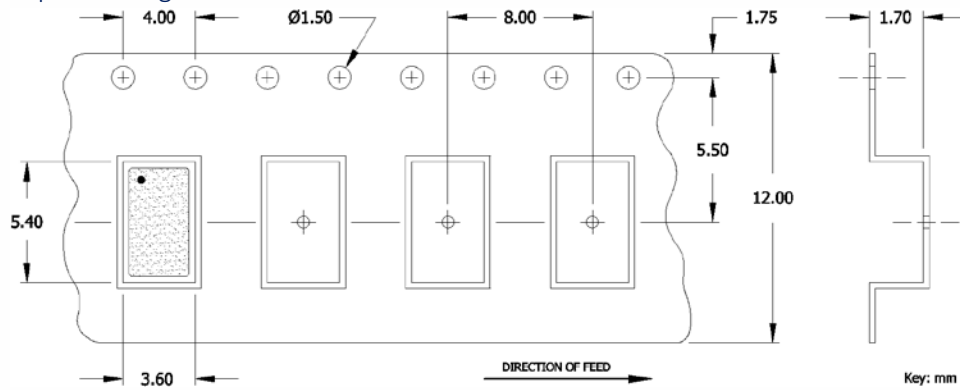
Pin	Symbol	Function
1	$V_C$	Control Voltage
2	EOH	Enable
3	GND	Circuit & Package
4	Output	RF Output
5	Output	RF Output, Complementary
6	$V_{CC}$	Supply Voltage

Table I - Date Code

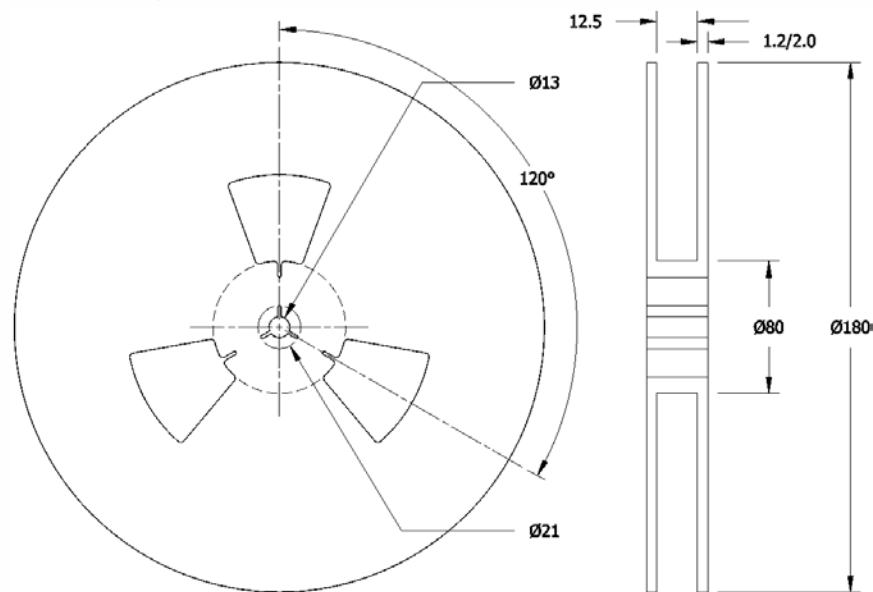
YEAR		MONTH														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC			
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

### Packaging - Tape and Reel

#### Tape Drawing



#### Reel Drawing



#### Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.