MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Rev 0, 05/2003

Preliminary Information

34923

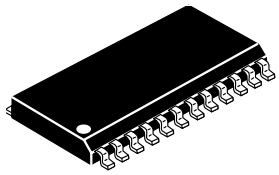
Full-Bridge PWM Motor Driver

FULL-BRIDGE PWM MOTOR DRIVER

Designed with Motorola's advanced SMARTMOS, the 34923 is designed for pulse-width modulated (PWM) current control of DC motors. It is capable of continuous output currents up to 2.0 A and operating voltages of up to 45 V. Internal fixed off-time PWM current-control timing circuitry can be programmed via a serial interface to operate in slow, fast, and mixed current-decay modes.

DIR and PWM/ENABLE input pins are provided for use in controlling the speed and direction of a DC motor with externally applied PWM-control signals. The PWM/ENABLE input can be programmed via the serial port to PWM the bridge in fast or slow current decay. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis and crossover-current protection. A special power-up sequencing is not required.



DW SUFFIX
24-LEAD SOICW
CASE 751E-04

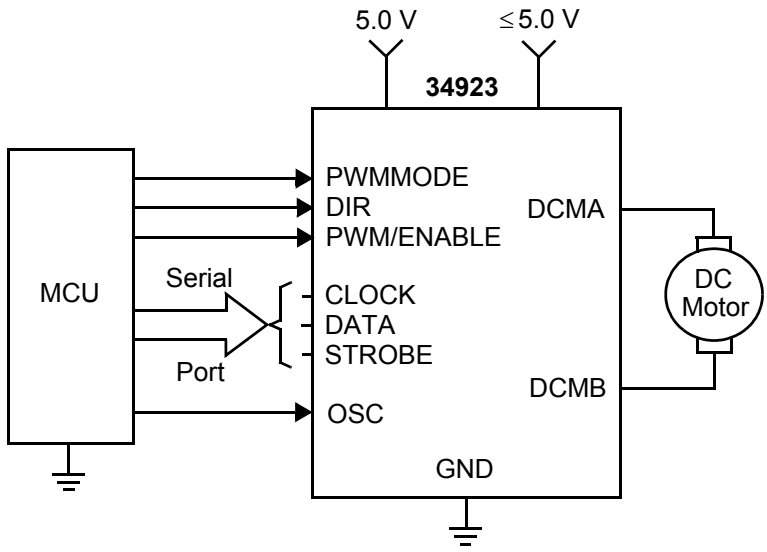
Features

- ±2.0 A, 45 V Continuous Output Rating
- Low $R_{DS(ON)}$ Outputs (270 mΩ, typical)
- Programmable Mixed, Fast, and Slow Current-Decay Modes
- Serial Interface Controls Chip Functions
- Synchronous Rectification for Low Power Dissipation
- Internal Undervoltage Lockout Thermal Shutdown Circuitry
- Crossover-Current Protection

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC34923DW/R2	-40 to 125°C	24 SOICW

34923 Simplified Application Diagram



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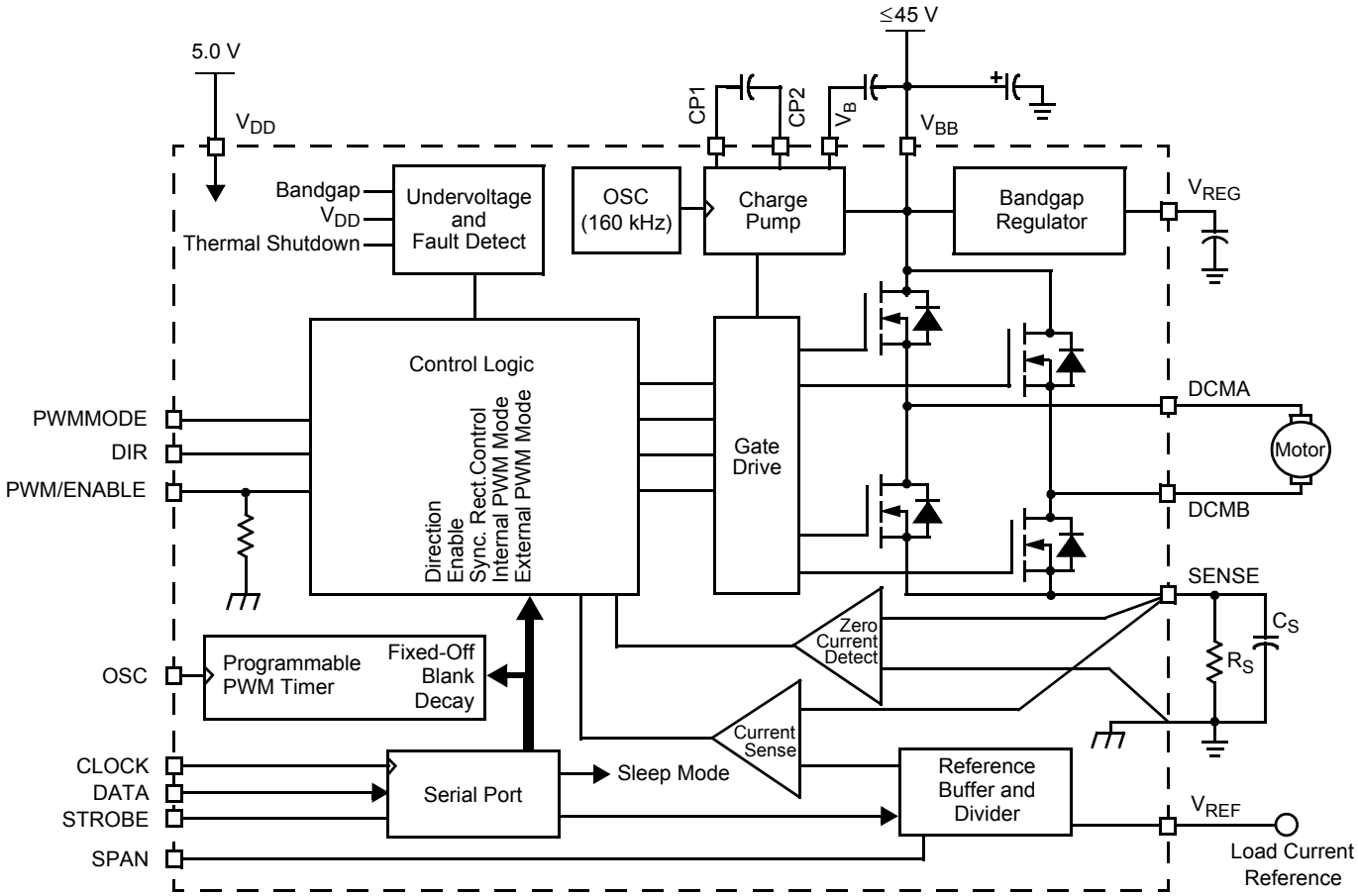
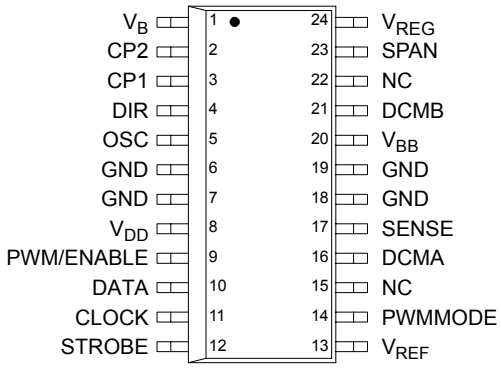


Figure 1. 34923 Simplified Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1	V_B	Boost Voltage	Boost voltage storage node.
2	CP2	Switching Capacitor 2	Charge pump capacitor connection 2.
3	CP1	Switching Capacitor 1	Charge pump capacitor connection 1.
4	DIR	Direction	Logic-level input for direction control.
5	OSC	Oscillator	Logic-level oscillator (square wave) input.
6, 7, 18, 19	GND	Ground	Ground.
8	V_{DD}	Logic Voltage	Low voltage (typically 5.0 V) logic supply.
9	PWM/ENABLE	H-Bridge Enable	Logic-level input for enabling the H-bridge driver.
10	DATA	Serial Data	Logic-level input for serial interface.
11	CLOCK	Serial Data Clock	Logic-level input for serial port (data is entered on rising edge).
12	STROBE	Serial Data Latch Strobe	Logic-level input for serial port (active on rising edge).
13	V_{REF}	Current Limit Reference Voltage	Load current reference input voltage.
14	PWMMODE	PWM Mode Control	Logic-level input for PWM mode control when in internal PWM mode.
15, 22	NC	No Connect	No internal connection to this pin.
16	DCMA	H-Bridge Output A	One of two bridge outputs to the motor.
17	SENSE	Current Sense	Sense resistor.
20	V_{BB}	H-Bridge Voltage Supply	High-current (20 V to 45 V) load supply.
21	DCMB	H-Bridge Output B	One of two bridge outputs to the motor.
23	SPAN	Current Limit Reference Range	Logic-level input for V_{REF} range control.
24	V_{REG}	Bandgap Voltage	Bandgap decoupling capacitor.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Load Supply Voltage	V_{BB}	48	V
Logic Supply Voltage	V_{DD}	7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Sense Voltage	V_S	0.5	V
Reference Voltage	V_{REF}	2.7	V
Output Current (Note 1)	I_{OUT}	±2.0	A
Storage Temperature	T_S	-55 to 150	°C
Ambient Temperature	T_A	-20 to 85	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Power Dissipation (T_A = 25°C) (Note 2)	P_D	1.6 (Note 3)	W
ESD Voltage Human Body Model (Note 4) Machine Model (Note 5)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Lead Soldering Temperature (Note 6)	T_{SOLDER}	260	°C
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	56	°C/W

Notes

1. Output current rating may be limited by duty cycle, ambient temperature, and heatsinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.
2. Maximum power dissipation at indicated ambient temperature in free air with no heatsink used.
3. Per SEMI G42-88 specification.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. Lead soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{BB} = 45 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, and f_{PWM} < 50 kHz unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVERS					
Load Supply Voltage Range	V_{BB}				V
Operating		20	–	45	
During Sleep Mode		0	–	45	
Output Leakage Current	I_{DSS}				µA
V_{OUT} = V_{BB}		–	<1.0	20	
V_{OUT} = 0 V		–	<-1.0	-20	
Output On Resistance	$R_{DS(ON)}$				mΩ
Source Driver, I_{OUT} = -2.0 A @ 25°C		–	300	450	
Source Driver, I_{OUT} = -2.0 A @ 150°C		–	–	700	
Sink Driver, I_{OUT} = 2.0 A @ 25°C		–	300	450	
Sink Driver, I_{OUT} = 2.0 A @ 150°C		–	–	700	
Body Diode Forward Voltage	V_F				V
Source Diode, I_F = -2.0 A		–	1.2	1.6	
Sink Diode, I_F = 2.0 A		–	1.2	1.6	
Load Supply Current	I_{BB}				
f_{PWM} < 50 kHz		–	4.0	7.0	mA
Charge Pump On, Outputs Disabled		–	2.0	5.0	mA
Sleep Mode		–	–	20	µA
CONTROL LOGIC					
Logic Supply Voltage Range (Operating)	V_{DD}	4.5	5.0	5.5	V
Logic Input Voltage					V
	$V_{IN(1)}$	2.0	–	–	
	$V_{IN(0)}$	–	–	0.8	
Input Current					µA
All Logic Inputs Except PWM/ENABLE					
V_{IN} = 2.0 V	$I_{IN(1)}$	–	<1.0	20	
V_{IN} = 0.8 V	$I_{IN(0)}$	–	<-2.0	-20	
PWM/ENABLE Only					
V_{IN} = 2.0 V	$I_{IN(1)}$	–	40	100	
V_{IN} = 0.8 V	$I_{IN(0)}$	–	16	40	
Input Hysteresis					mV
All Digital Inputs Except OSC	$\Delta V_{IN(LOGIC)}$	50	–	100	
OSC (Operating)	$\Delta V_{IN(OSC)}$	200	–	400	
Reference Input Voltage Range (Operating)	V_{REF}	0	–	2.6	V
Reference Input Current	I_{REF}				µA
V_{REF} = 2.5 V		–	–	±0.5	
Input Offset Voltage	V_{IO}				mV
Comparator V_{REF} = 0 V		–	0	±5.0	
Buffer		–	0	±15	

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions $T_A = 25°C$, V_{BB} = 45 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, and f_{PWM} < 50 kHz unless otherwise noted.

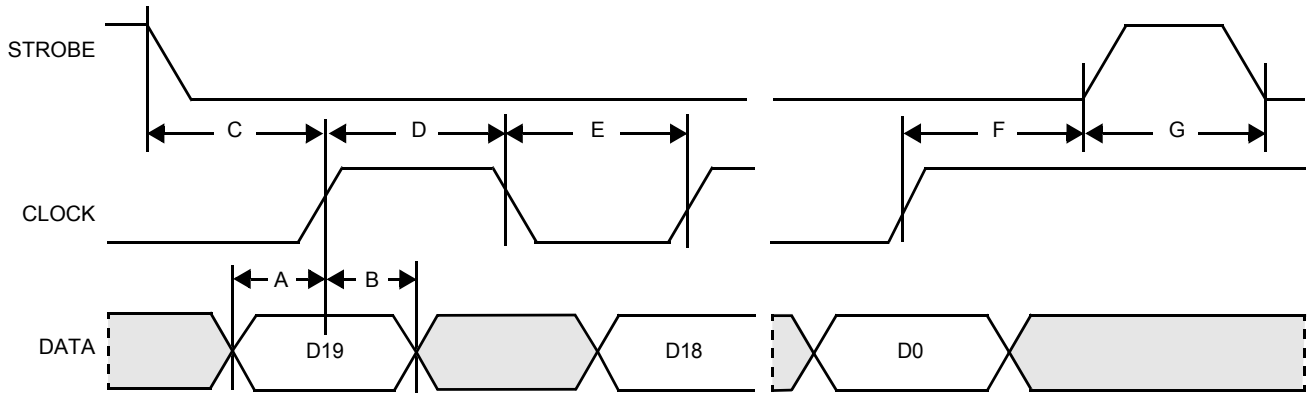
Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL LOGIC (continued)					
Reference Divider Ratio	–				–
Bit D14 = High		9.9	10	10.2	
Bit D14 = Low		4.95	5.0	5.05	
Thermal Shutdown Temperature	T_J	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J	–	15	–	°C
Undervoltage Lockout Enable Threshold	UVLO				V
Increasing V_{DD}		3.90	4.2	4.45	
Undervoltage Lockout Hysteresis	ΔUVLO	0.05	0.10	–	V
Logic Supply Current	I_{DD}				mA
f_{PMW} < 50 kHz		–	6.0	10	
Sleep Mode, Inputs <0.5 V		–	–	2.0	

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{BB} = 45 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, and f_{PWM} < 50 kHz unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL LOGIC					
OSC Input Frequency (Operating)	f_{OSC}	2.9	–	6.1	MHz
OSC Input Duty Cycle (Operating)	dc_{OSC}	40	–	60	%
Propagation Delay Times	t_{pd}				ns
PWM Change to Source ON		–	600	–	
PWM Change to Source OFF		–	100	–	
PWM Change to Sink ON		–	600	–	
PWM Change to Sink OFF		–	100	–	
Direction Change to Sink ON		–	600	–	
Direction Change to Sink OFF		–	100	–	
Direction Change to Source ON		–	600	–	
Direction Change to Source OFF		–	100	–	

Timing Diagram



Legend

ID	Description	Value (ns)
A	DATA Setup Time	15
B	DATA Hold Time	10
C	Setup STROBE-to-CLOCK Rising Edge	50
D	CLOCK High Pulse Width	50

ID	Description	Value (ns)
E	CLOCK Low Pulse Width	50
F	Setup CLOCK Rising Edge-to-STROBE	50
G	STROBE Pulse Width	50

Figure 2. Serial Port Write Timing

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 34923 is designed for pulse-width modulated (PWM) current control of DC motors. It is capable of continuous output currents up to 2.0 A and operating voltages of up to 45 V. Internal fixed off-time PWM current-control timing circuitry can be programmed via a serial interface to operate in slow, fast, and mixed current decay modes.

DIR and PWM/ENABLE input pins are provided for use in controlling the speed and direction of a DC motor with externally applied PWM-control signals. The PWM/ENABLE input can be programmed via the serial port to PWM the bridge in fast or slow current decay. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis and crossover-current protection. Special power-up sequencing is not required.

FUNCTIONAL PIN DESCRIPTION

V_B

This pin provides a node for charge storage at the boost voltage. Internal circuitry will draw V_B current from this node, and the charge pump will deliver charge to this node.

CP1 and CP2

These pins are the connections to the switching capacitor in the charge pump. These pins swing between ground and V_B, drawing charge from V_{BB} and delivering it to the V_B node.

DIR

This is the direction input for the H-bridge driver.

PWM/ENABLE

This pin is the enable input for the H-bridge driver. When asserted this will bring the H-bridge out of tri-state mode so that it can drive a load.

PWMMODE

This logic input controls the H-bridge output mode when the PWM is deasserted. The H-bridge can have an active or passive output state when the PWM input is deasserted.

OSC

This logic input is the clock for the on-board decay time generator used only when in internal PWM mode. The decay time can be slow or mixed fast and slow.

V_{DD}

This is the power supply input for the internal logic and several other functions.

DATA

This logic input is the serial data used by the serial interface.

CLOCK

This logic input is the clock for the serial interface. Data is shifted in synchronously with this clock.

STROBE

This logic input is used to latch data from the serial interface into the internal logic.

V_{REF}

This input provides a reference voltage for the current limit comparator threshold.

DCMA and DCMB

These are the high-current, high-voltage drive signals for the motor.

V_{BB}

This is the motor drive voltage input. The H-bridge will deliver this voltage to the motor.

SPAN

This logic-level input controls the current limit comparator threshold that is generated from V_{REF}.

V_{REG}

This output is a decoupling node for the internal bandgap reference voltage generator.

FUNCTIONAL DESCRIPTION

Serial Interface

The 34923 is controlled via a 3-wire (clock, data, strobe) serial port. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is clocked in starting with bit D19.

Bit	Function
D0	Blank Time LSB
D1	Blank Time MSB
D2	Fixed Off-Time LSB
D3	Fixed Off-Time Bit 1
D4	Fixed Off-Time Bit 2
D5	Fixed Off-Time Bit 3
D6	Fixed Off-Time MSB
D7	Fast Decay Time LSB
D8	Fast Decay Time Bit 1
D9	Fast Decay Time Bit 2
D10	Fast Decay Time MSB
D11	Synchronous Rectification Mode
D12	Synchronous Rectification Enable
D13	External PWM Decay Mode
D14	Enable Logic
D15	Direction Logic
D16	Divisor SPAN Select
D17	Internal PWM Mode
D18	Test Mode
D19	Sleep Mode

D0–D1, Blank Time

The current-sense comparator is blanked when any output driver is switched on in accordance with the table below. f_{osc} is the oscillator input frequency.

D0	D1	Blank Time
0	0	$4/f_{osc}$
1	0	$6/f_{osc}$
0	1	$12/f_{osc}$
1	1	$24/f_{osc}$

D2–D6, Fixed Off-Time

A five-bit word sets the fixed off-time for internal PWM current control. The off time is defined as follows:

$$t_{off} = (8[1 + N]/f_{osc}) - 1/f_{osc}$$

where N = 0 to 31.

For example, with an oscillator frequency of 4.0 MHz, the off-time is adjusted from 1.75 μs to 63.75 μs in increments of 2.0 μs.

D7–D10, Fast Decay Time

A four-bit word sets the fast decay portion of the fixed off-time for the internal PWM control circuitry. This will only have impact if the mixed current decay mode is selected (via bit D17 and the PWMMODE input pin). For $t_{fd} > t_{off}$, the device will effectively operate in the fast decay mode. The fast decay portion is defined as follows:

$$t_{fd} = (8[1 + N]/f_{osc}) - 1/f_{osc}$$

where N = 0 to 15.

For example, with an oscillator frequency of 4.0 MHz, the fast decay time is adjusted from 1.75 μs to 31.75 μs in increments of 2.0 μs.

D11–D12, Synchronous Rectification Control

The active mode prevents reversal of load current by turning off synchronous rectification when a zero current level is detected. The passive mode will allow reversal of current but will turn off the synchronous rectifier circuit if the load current inversion ramps up to the current limit set by V_{REF}/R_S.

D11	D12	Synchronous Rect. Control
0	0	Disabled
0	1	Active
1	0	Disabled
1	1	Passive

D13, External PWM Decay Mode

Bit D13 determines the current decay mode when using PWM/ENABLE chopping for external PWM current control.

D13	Current Decay Mode
0	Fast
1	Slow

D14, Enable Logic

Bit D14, in conjunction with the PWM/ENABLE pin, determines if the output drivers are in the chopped (OFF) or ON state.

PWM/ ENABLE	D14	Operating Mode
0	0	Chopped
1	1	
1	0	ON
0	1	

D15, Direction Logic

Bit D15, in conjunction with the DIR pin, determines if the device is operating in the forward or reverse state.

State	DIR	D15	DCMA	DCMB
Reverse	0	0	Low	High
	1	1		
Forward	1	0	High	Low
	0	1		

D16, Divisor SPAN Select

Bit D16, in conjunction with the SPAN pin, determines if V_{REF} is divided by 5 or 10.

Divisor	SPAN	D16
÷5	1	0
	0	1
÷10	0	0
	1	1

D17, Internal PWM Mode

Bit D17, in conjunction with the PWMMODE pin, selects mixed or slow current decay.

PWMMODE	D17	Current Decay Mode
0	0	Mixed
1	1	
1	0	Slow
0	1	

D18, Test Mode

Bit D18 low (default) operates the device in normal mode. D18 is only used for testing purposes. The user should never change this bit.

D19, Sleep Mode

Bit D19 selects a Sleep mode to minimize power consumption when not in use. This disables much of the internal circuitry, including the regulator and charge pump. On power-up the serial port is initialized to all zeros. Bit D19 should be programmed high for 1.0 ms before attempting to enable any output driver.

D19	Sleep Mode
0	Sleep
1	Normal

Serial Port Write Timing Operations

Data is clocked into the shift register on the rising edge of the CLOCK signal. Normally STROBE will be held high, only brought low to initiate a write cycle. Refer to Figure 2, Serial Port Write Timing, page 8, for the minimum timing requirements.

V_{REG}

This internally generated voltage is used to operate the sink-side outputs. The V_{REG} pin should be decoupled with a 0.22 μF capacitor to ground. V_{REG} is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

Charge Pump

The charge pump is used to generate a gate supply voltage greater than V_{BB} to drive the source-side gates. A 0.22 μF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.22 μF ceramic capacitor should be connected between V_B and V_{BB} to act as a reservoir to operate the high-side devices. The V_B voltage is internally monitored and, in the case of a fault condition, the source outputs of the device are disabled.

Shutdown

In the event of a fault (excessive junction temperature or low voltage on V_B or V_{REG}), the outputs of the device are disabled until the fault condition is removed. At power-up, and in the event of low V_{DD}, the Undervoltage Lockout circuit disables the drivers and resets the data in the serial port to all zeros.

PWM Timer Function

The PWM timer is programmable via the serial port (bits D2–D10) to provide off-time PWM signals to the control circuitry. In the mixed current-decay mode, the first portion of the off time operates in fast decay, until the fast decay time count (serial bits D7–D10) is reached, followed by slow decay for the rest of the off-time period (bits D2–D6). If the fast decay time is set longer than the off time, the device effectively operates in fast decay mode. Bit D17, in conjunction with PWMMODE, selects mixed or slow decay.

PWM Blank Timer

When a source driver turns on, a current spike occurs owing to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source-enable latch, the sense comparator is blanked. The blank timer runs after the off-time counter (see bits D2–D6) to provide the programmable blanking function. The blank timer is reset when PWM/ENABLE is chopped or DIR is changed. For external PWM control, a DIR change or PWM/ENABLE on will trigger the blanking function.

Synchronous Rectification

When a PWM off cycle is triggered, either by an PWM/ENABLE chop command or internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The 34923 synchronous rectification feature will turn on the opposite pair of outputs during the current decay and effectively short out the body diodes with the low $R_{DS(ON)}$ driver. This will reduce power dissipation significantly and can eliminate the need for external Schottky diodes.

Synchronous rectification can be configured in active mode, passive mode, or disabled via the serial port (bits D11 and D12).

The active or passive mode selection has no impact in slow-decay mode. With synchronous rectification enabled, the slow-decay mode serves as an effective brake mode.

Current Regulation

Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the H-bridge are turned on, the current increases in the motor winding until it reaches a trip value determined by the external sense resistor (R_S), the applied analog reference voltage (V_{REF}), the SPAN logic level, and serial data bit D16:

$$\text{When SPAN} = \text{D16},\ I_{TRIP} = V_{REF}/10R_S$$
$$\text{When SPAN} \neq \text{D16},\ I_{TRIP} = V_{REF}/5R_S$$

At the trip point, the sense comparator resets the source-enable latch, turning off the source driver. The load inductance then causes the current to recirculate for the serial-port-programmed fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed current-decay mode (D17) and the synchronous rectification control bits (D11 and D12).

Internal PWM (Current Mode) PWM Frequency

The internal PWM opeating frequency is set by the sum of “Off Time”, as determined by bits D2 through D6, “Blank Time”, as determined by bits D0 and D1, and the time constant of the motor.

APPLICATIONS

Current Sensing

To minimize inaccuracies in sensing the I_{TRIP} current level, which may be caused by ground trace IR drops, the sense resistor should have an independent ground return to the ground pin of the device. For low-value sense resistors, the IR drops in the PCB sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided because they can introduce variation in R_S owing to their contact resistance.

The maximum value of R_S is given as $R_S \leq 0.5/I_{TRIP}$.

Braking

The braking function is implemented by driving the device in slow-decay mode via serial port bit D13, enabling synchronous rectification via bit D12, and chopping with the combination of D14 and the PWM/ENABLE input pin. Because it is possible to drive current in either direction through the drivers, this configuration effectively shorts out the motor-generated back EMF (BEMF) as long as the PWM/ENABLE chop mode is asserted. It is important to note that the internal PWM current-control circuit will not limit the current when braking, because the current does not flow through the sense resistor. The maximum brake current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations of high-speed and high-inertial loads.

Thermal Protection

Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures owing to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout

The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance (see following Note), the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to the ground pins of the device. This path should be as short as is possible physically and should not have any other components connected to it. It is recommended that a 0.1 μF capacitor be placed between SENSE and ground as close to the device as possible; the load supply pin, V_{BB}, should be decoupled with an electrolytic capacitor (>47 μF is recommended) placed as close to the device as is possible.

Note The thermal resistance and absolute maximum allowable package power dissipation specified in the MAXIMUM RATINGS table, page 4, is measured on typical two-sided PCB with minimal copper ground area. For the 34923, $R_{\theta JA}$ can be reduced to 56°C/W with 3.57-in^2 copper ground area, as shown in Figure 3.

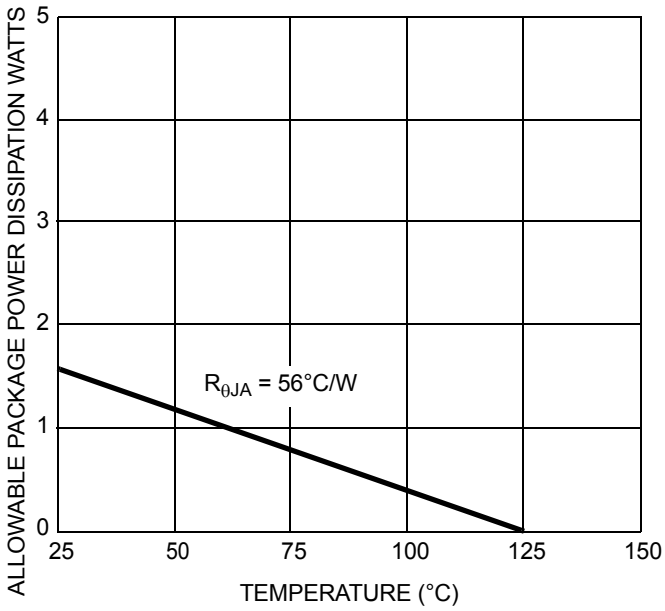
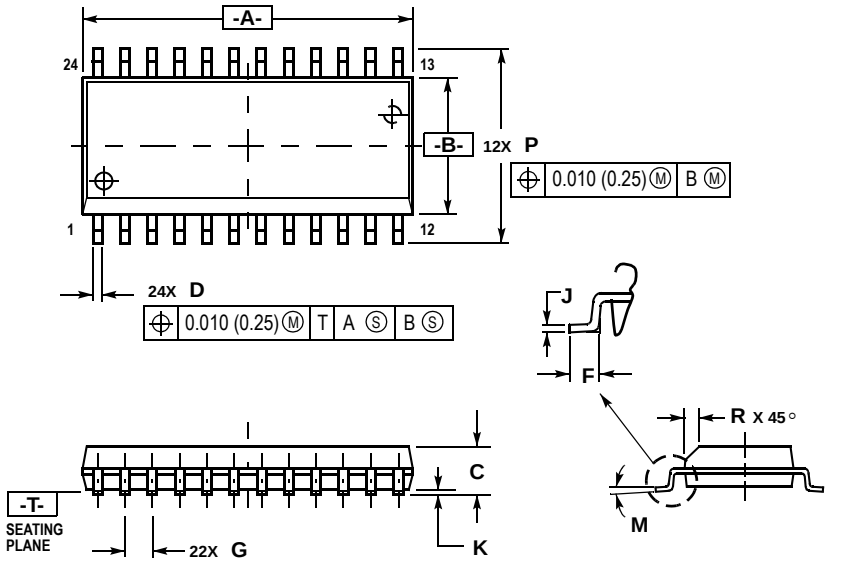


Figure 3. Package Dissipation Temperature Derating

PACKAGE DIMENSIONS

DW SUFFIX
24-LEAD SOIC WIDE BODY
PLASTIC PACKAGE
CASE 751E-04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES

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