

# MITSUBISHI MICROCOMPUTERS

## 3802 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

### DESCRIPTION

The 3802 group is the 8-bit microcomputer based on the 740 family core technology.

The 3802 group is designed for controlling systems that require analog signal processing and include two serial I/O functions, A-D converters, and D-A converters.

The various microcomputers in the 3802 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3802 group, refer to the section on group expansion.

### FEATURES

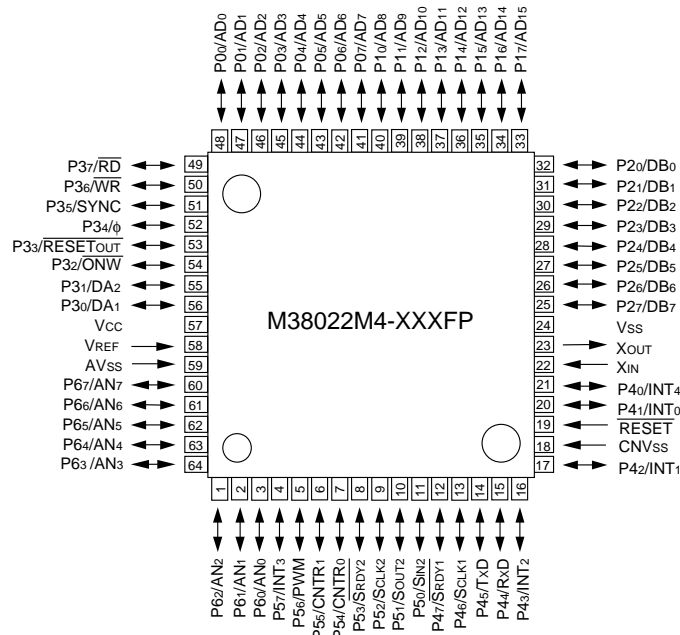
- Basic machine-language instructions ..... 71
- The minimum instruction execution time ..... 0.5  $\mu$ s  
(at 8 MHz oscillation frequency)
- Memory size
  - ROM ..... 8 K to 32 K bytes
  - RAM ..... 384 to 1024 bytes

- Programmable input/output ports ..... 56
- Interrupts ..... 16 sources, 16 vectors
- Timers ..... 8 bit X 4
- Serial I/O1 ..... 8-bit X 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit X 1 (Clock-synchronized)
- PWM ..... 8-bit X 1
- A-D converter ..... 8-bit X 8 channels
- D-A converter ..... 8-bit X 2 channels
- Clock generating circuit ..... Internal feedback resistor  
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage ..... 3.0 to 5.5 V  
(Extended operating temperature version : 4.0 to 5.5 V)
- Power dissipation ..... 32 mW
- Memory expansion possible
- Operating temperature range ..... -20 to 85°C  
(Extended operating temperature version : -40 to 85°C)

### APPLICATIONS

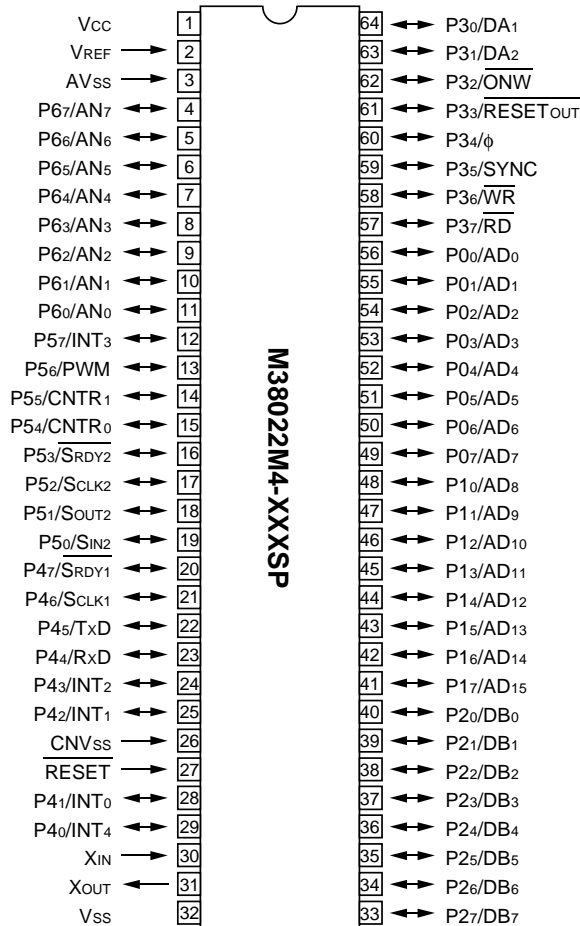
Office automation, VCRs, tuners, musical instruments, cameras, air conditioners, etc.

### PIN CONFIGURATION (TOP VIEW)



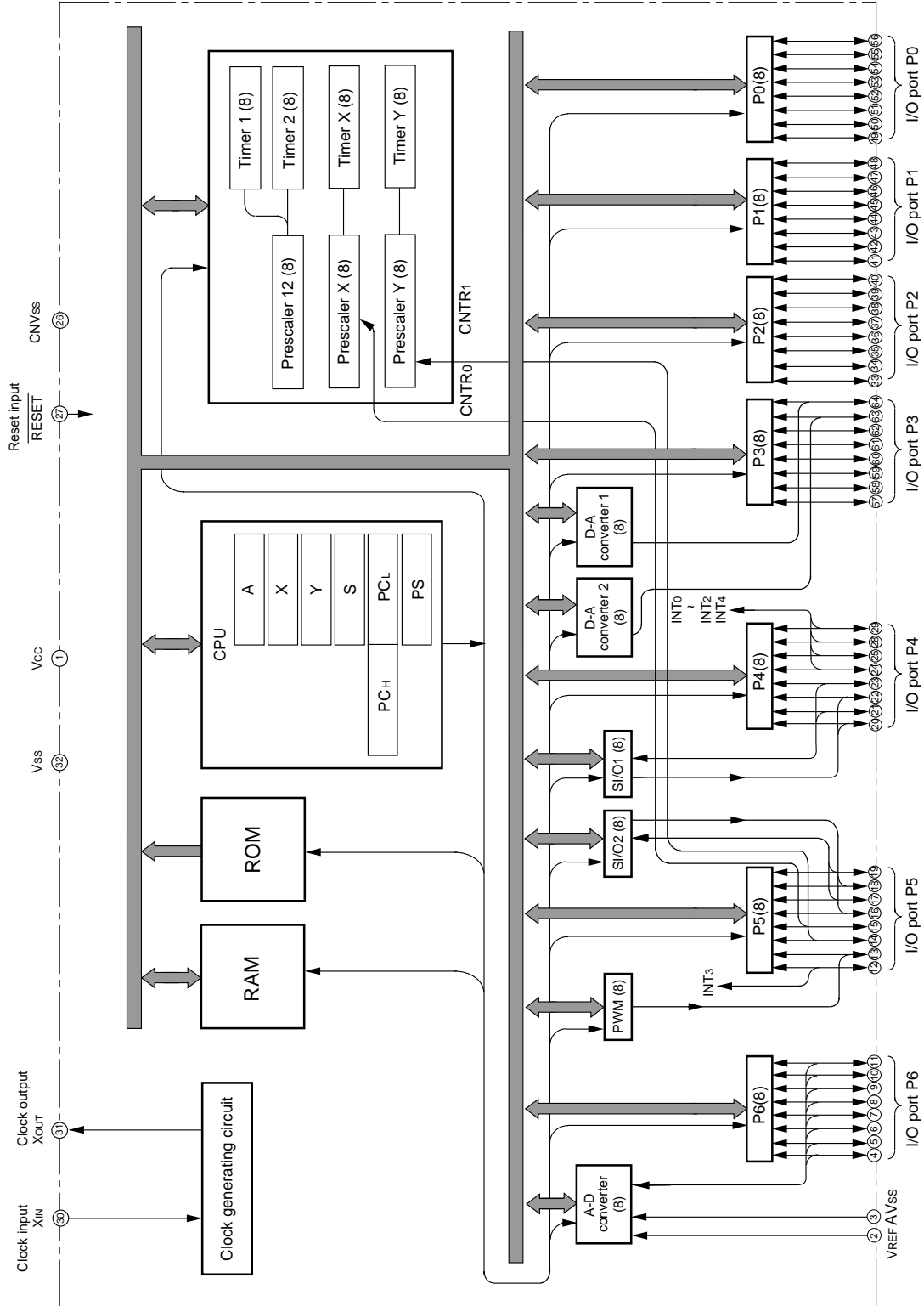
Package type : 64P6N-A  
64-pin plastic-molded QFP

**PIN CONFIGURATION (TOP VIEW)**



**Package type : 64P4B**  
**64-pin shrink plastic-molded DIP**

FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



**PIN DESCRIPTION**

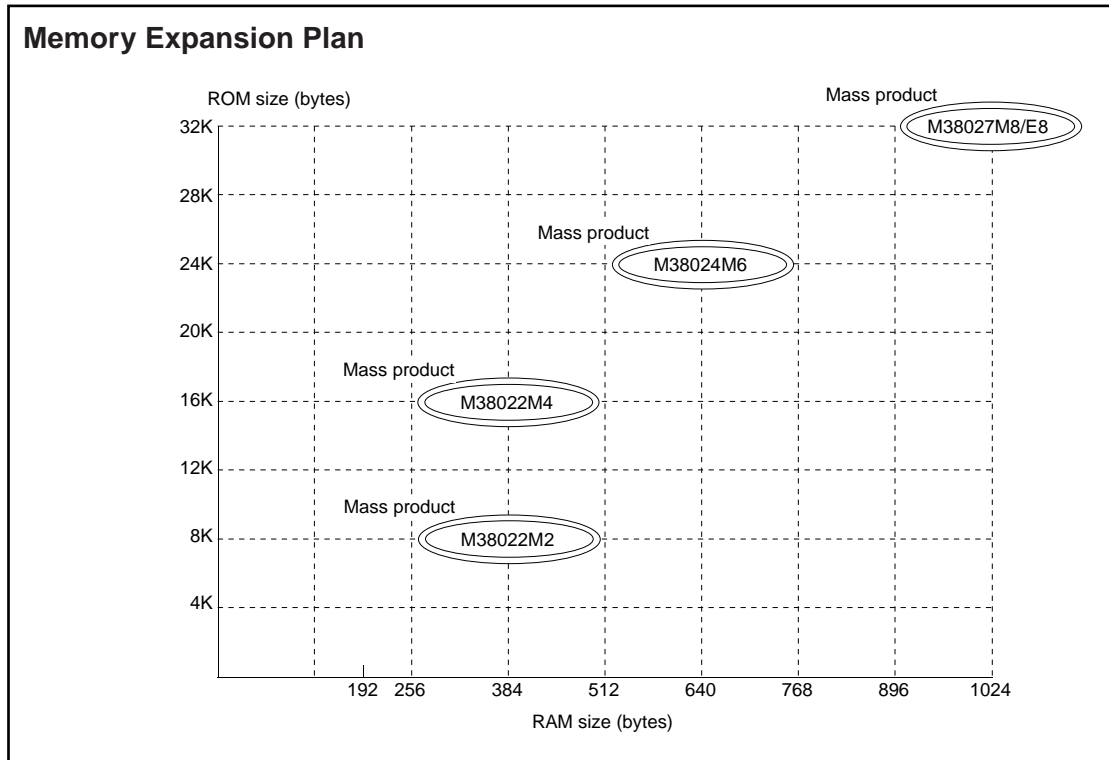
| Pin   | Name                     | Function   |  |  |
|---|--------------------------|--|--|--|
|   |                          |  | Function except a port function  |  |
| Vcc, Vss  | Power source             | <ul style="list-style-type: none"> <li>Apply voltage of 3.0 V–5.5 V to Vcc, and 0 V to Vss.<br/>(Extended operating temperature version : 4.0 V to 5.5 V)</li> </ul>   |  |  |
| CNVss   | CNVss                    | <ul style="list-style-type: none"> <li>This pin controls the operation mode of the chip.</li> <li>Normally connected to Vss.</li> <li>If this pin is connected to Vcc, the internal ROM is inhibited and external memory is accessed.</li> </ul>   |  |  |
| VREF  | Analog reference voltage | <ul style="list-style-type: none"> <li>Reference voltage input pin for A-D and D-A converters</li> </ul>   |  |  |
| AVSS  | Analog power source      | <ul style="list-style-type: none"> <li>GND input pin for A-D and D-A converters</li> <li>Connect to Vss.</li> </ul>  |  |  |
| $\overline{\text{RESET}}$   | Reset input              | <ul style="list-style-type: none"> <li>Reset input pin for active "L"</li> </ul>   |  |  |
| XIN   | Clock input              | <ul style="list-style-type: none"> <li>Input and output signals for the clock generating circuit.</li> <li>Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.</li> <li>If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.</li> <li>The clock is used as the oscillating source of system clock.</li> </ul> |  |  |
| XOUT  | Clock output             |  |  |  |
| P00–P07   | I/O port P0              | <ul style="list-style-type: none"> <li>8 bit CMOS I/O port</li> <li>I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>At reset this port is set to input mode.</li> <li>In modes other than single-chip, these pins are used as address, data, and control bus I/O pins.</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>           |  |  |
| P10–P17   | I/O port P1              |  |  |  |
| P20–P27   | I/O port P2              |  |  |  |
| P30/DA <sub>1</sub> ,<br>P31/DA <sub>2</sub>  | I/O port P3              |  |  | <ul style="list-style-type: none"> <li>D–A conversion output pins</li> </ul> |
| P32–P37   |                          |  |  |  |
| P40/INT <sub>4</sub> ,<br>P41/INT <sub>0</sub> ,<br>P42/INT <sub>1</sub> ,<br>P43/INT <sub>2</sub>    | I/O port P4              | <ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>  | <ul style="list-style-type: none"> <li>External interrupt input pin</li> </ul> |  |
| P44/RxD,<br>P45/TxD,<br>P46/SCLK <sub>1</sub> ,<br>P47/SRDY <sub>1</sub>                              |                          |  | <ul style="list-style-type: none"> <li>Serial I/O1 I/O pins</li> </ul>         |  |
| P50/SIN <sub>2</sub> ,<br>P51/SOUT <sub>2</sub> ,<br>P52/SCLK <sub>2</sub> ,<br>P53/SRDY <sub>2</sub> | I/O port P5              | <ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>  | <ul style="list-style-type: none"> <li>Serial I/O2 I/O pins</li> </ul>         |  |
| P54/CNTR <sub>0</sub> ,<br>P55/CNTR <sub>1</sub>  |                          |  | <ul style="list-style-type: none"> <li>Timer X and Timer Y I/O pins</li> </ul> |  |
| P56/PWM   |                          |  | <ul style="list-style-type: none"> <li>PWM output pin</li> </ul>               |  |
| P57/INT <sub>3</sub>  |                          |  | <ul style="list-style-type: none"> <li>External interrupt input pin</li> </ul> |  |
| P60/AN <sub>0</sub> –<br>P67/AN <sub>7</sub>  | I/O port P6              | <ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>  | <ul style="list-style-type: none"> <li>A-D conversion input pins</li> </ul>    |  |

**GROUP EXPANSION**

Mitsubishi plans to expand the 3802 group as follows:

- (1) Support for mask ROM, One Time PROM, and EPROM versions
  - ROM/PROM capacity ..... 8 K to 32 K bytes
  - RAM capacity ..... 384 to 1024 bytes

- (2) Packages
  - 64P4B ..... Shrink plastic molded DIP
  - 64P6N-A ..... Plastic molded QFP
  - 64S1B-E ..... Shrink ceramic DIP
  - 64D0 ..... Ceramic LCC



Currently supported products are listed below

As of May 1996

| Product        | (P) ROM size (bytes)<br>ROM size for User in ( ) | RAM size (bytes) | Package | Remarks                       |
|----------------|--|------------------|---------|-------------------------------|
| M38022M2-XXXSP | 8192<br>(8062)                                   | 384              | 64P4B   | Mask ROM version              |
| M38022M2-XXXFP |  |                  | 64P6N-A | Mask ROM version              |
| M38022M4-XXXSP | 16384<br>(16254)                                 | 384              | 64P4B   | Mask ROM version              |
| M38022M4-XXXFP |  |                  | 64P6N-A | Mask ROM version              |
| M38024M6-XXXSP | 24576<br>(24446)                                 | 640              | 64P4B   | Mask ROM version              |
| M38024M6-XXXFP |  |                  | 64P6N-A | Mask ROM version              |
| M38027M8-XXXSP | 32768<br>(32638)                                 | 1024             | 64P4B   | Mask ROM version              |
| M38027E8-XXXSP |  |                  |         | One Time PROM version         |
| M38027E8SP     |  |                  |         | One Time PROM version (blank) |
| M38027M8-XXXFP |  |                  | 64P6N-A | Mask ROM version              |
| M38027E8-XXXFP |  |                  |         | One Time PROM version         |
| M38027E8FP     |  |                  |         | One Time PROM version (blank) |
| M38027E8SS     |  |                  |         | 64S1B-E                       |
| M38027E8FS     |  |                  | 64D0    | EPROM version                 |

# 3802 Group

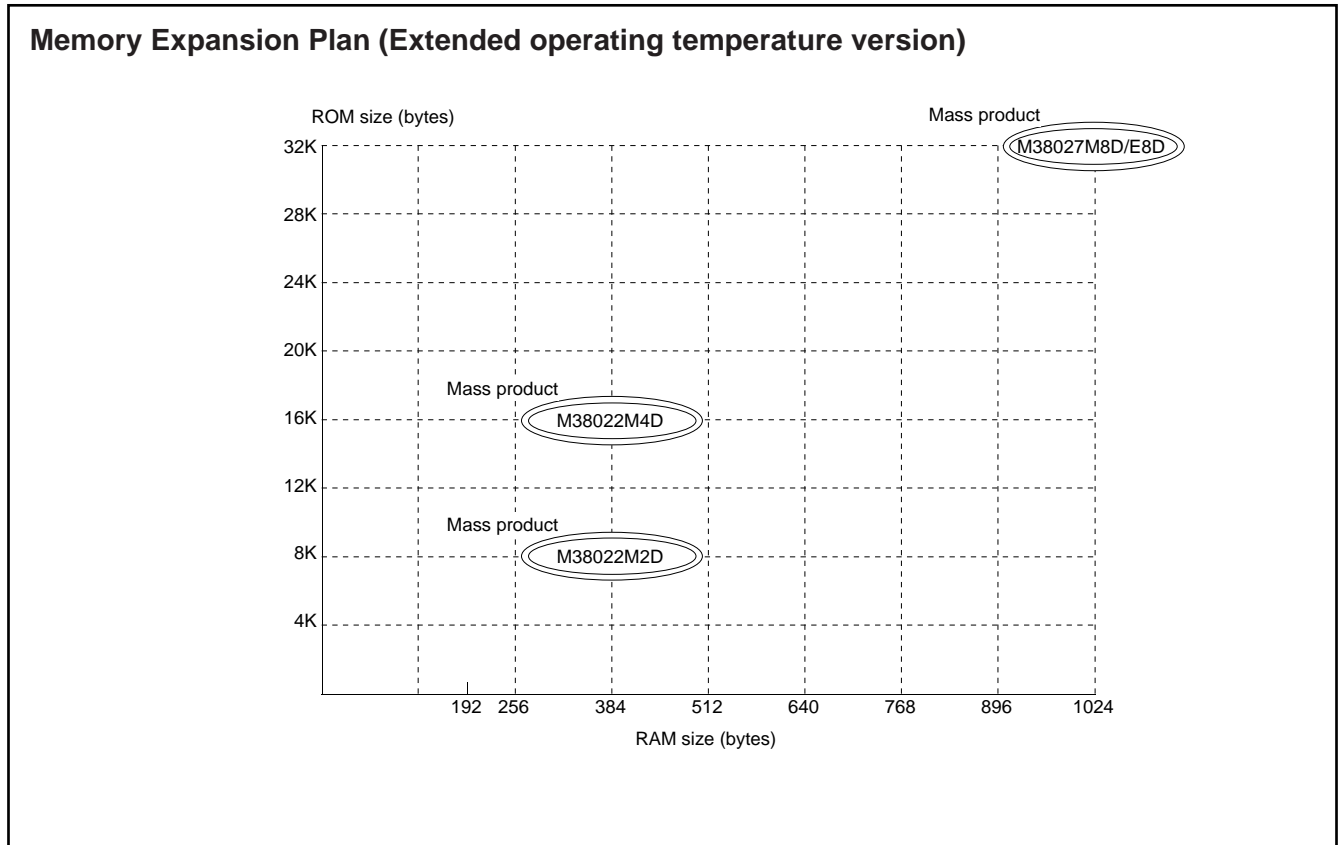
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## GROUP EXPANSION (Extended operating temperature version)

Mitsubishi plans to expand the 3802 group (extended operating temperature version) as follows:

- (1) Support for mask ROM One Time PROM, and EPROM versions
  - ROM/PROM capacity ..... 8 K to 32 K bytes
  - RAM capacity ..... 384 to 1024 bytes

- (2) Packages
  - 64P4B ..... Shrink plastic molded DIP
  - 64P6N-A ..... Plastic molded QFP

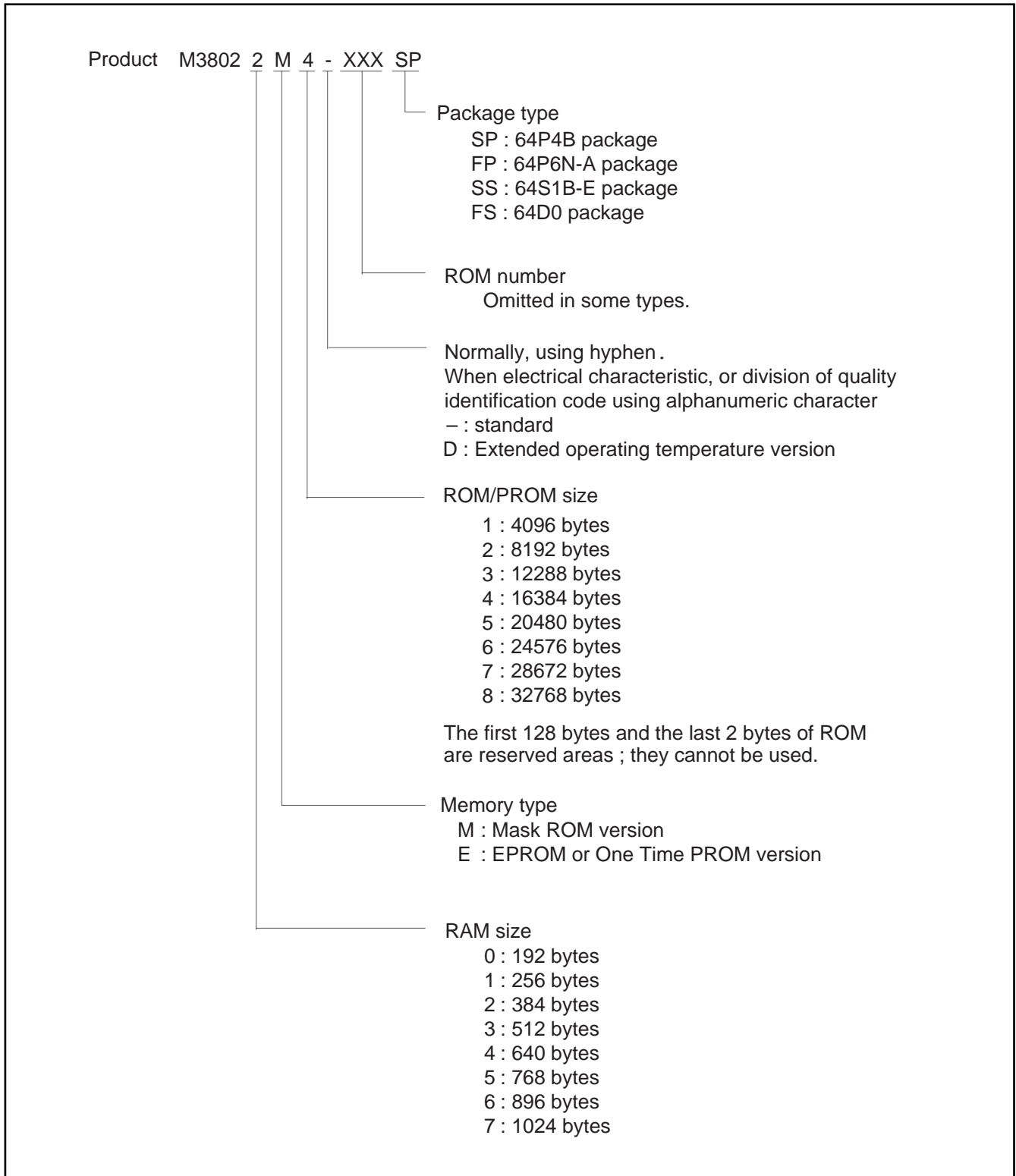


Currently supported products are listed below.

As of May 1996

| Product        | (P) ROM size (bytes) | RAM size (bytes) | Package | Remarks                       |
|----------------|----------------------|------------------|---------|-------------------------------|
| M38022M2DXXXSP | 8192                 | 384              | 64P4B   | Mask ROM version              |
| M38022M2DXXXFP | (8062)               |                  | 64P6N-A | Mask ROM version              |
| M38022M4DXXXSP | 16384                | 384              | 64P4B   | Mask ROM version              |
| M38022M4DXXXFP | (16254)              |                  | 64P6N-A | Mask ROM version              |
| M38027M8DXXXSP | 32768<br>(32638)     | 1024             | 64P4B   | Mask ROM version              |
| M38027E8DXXXSP |                      |                  |         | One Time PROM version         |
| M38027E8DSP    |                      |                  |         | One Time PROM version (blank) |
| M38027M8DXXXFP |                      |                  | 64P6N-A | Mask ROM version              |
| M38027E8DXXXFP |                      |                  |         | One Time PROM version         |
| M38027E8DFP    |                      |                  |         | One Time PROM version (blank) |

**PART NUMBERING**



## FUNCTIONAL DESCRIPTION

### Central Processing Unit (CPU)

The 3802 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

### CPU mode register

The CPU mode register is allocated at address 003B<sub>16</sub>.

The CPU mode register contains the stack page selection bit.

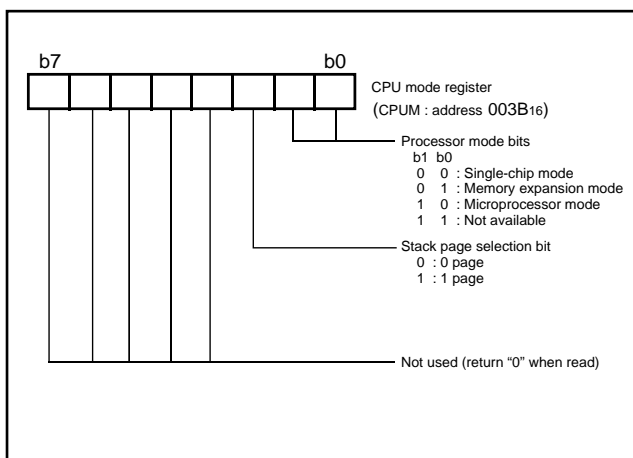


Fig. 1 Structure of CPU mode register



**Memory**

**Special function register (SFR) area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

**RAM**

RAM is used for data storage and for stack area of subroutine calls and interrupts.

**ROM**

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

**Interrupt vector area**

The interrupt vector area contains reset and interrupt vectors.

**Zero page**

The 256 bytes from addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

**Special page**

The 256 bytes from addresses FF00<sub>16</sub> to FFFF<sub>16</sub> are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

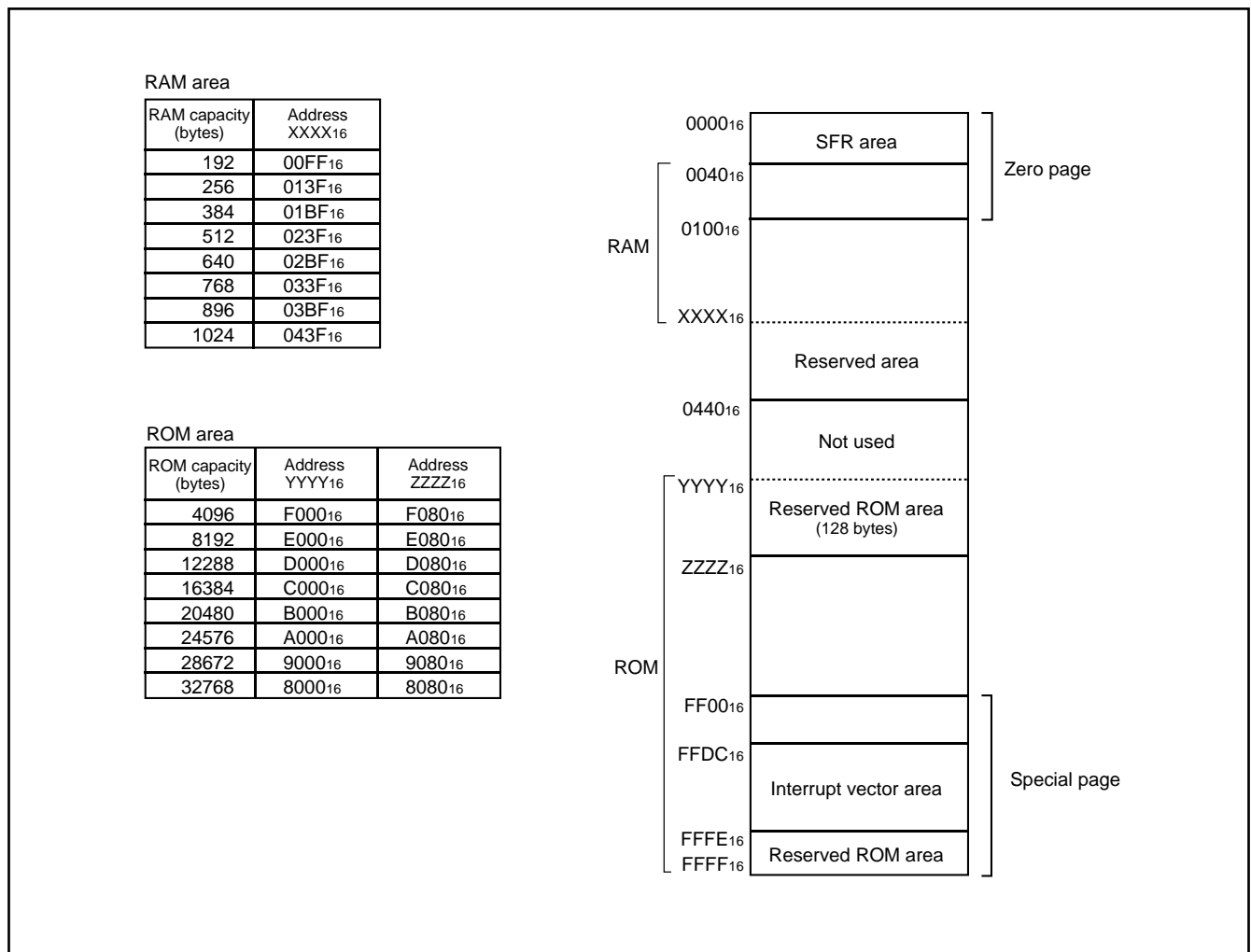


Fig. 2 Memory map diagram

|                    |  |                    |   |
|--------------------|--|--------------------|---|
| 0000 <sub>16</sub> | Port P0 (P0)                             | 0020 <sub>16</sub> | Prescaler 12 (PRE12)                        |
| 0001 <sub>16</sub> | Port P0 direction register (P0D)         | 0021 <sub>16</sub> | Timer 1 (T1)                                |
| 0002 <sub>16</sub> | Port P1 (P1)                             | 0022 <sub>16</sub> | Timer 2 (T2)                                |
| 0003 <sub>16</sub> | Port P1 direction register (P1D)         | 0023 <sub>16</sub> | Timer XY mode register (TM)                 |
| 0004 <sub>16</sub> | Port P2 (P2)                             | 0024 <sub>16</sub> | Prescaler X (PREX)                          |
| 0005 <sub>16</sub> | Port P2 direction register (P2D)         | 0025 <sub>16</sub> | Timer X (TX)                                |
| 0006 <sub>16</sub> | Port P3 (P3)                             | 0026 <sub>16</sub> | Prescaler Y (PREY)                          |
| 0007 <sub>16</sub> | Port P3 direction register (P3D)         | 0027 <sub>16</sub> | Timer Y (TY)                                |
| 0008 <sub>16</sub> | Port P4 (P4)                             | 0028 <sub>16</sub> |   |
| 0009 <sub>16</sub> | Port P4 direction register (P4D)         | 0029 <sub>16</sub> |   |
| 000A <sub>16</sub> | Port P5 (P5)                             | 002A <sub>16</sub> |   |
| 000B <sub>16</sub> | Port P5 direction register (P5D)         | 002B <sub>16</sub> | PWM control register (PWMCON)               |
| 000C <sub>16</sub> | Port P6 (P6)                             | 002C <sub>16</sub> | PMW prescaler (PREPWM)                      |
| 000D <sub>16</sub> | Port P6 direction register (P6D)         | 002D <sub>16</sub> | PWM register (PWM)                          |
| 000E <sub>16</sub> |  | 002E <sub>16</sub> |   |
| 000F <sub>16</sub> |  | 002F <sub>16</sub> |   |
| 0010 <sub>16</sub> |  | 0030 <sub>16</sub> |   |
| 0011 <sub>16</sub> |  | 0031 <sub>16</sub> |   |
| 0012 <sub>16</sub> |  | 0032 <sub>16</sub> |   |
| 0013 <sub>16</sub> |  | 0033 <sub>16</sub> |   |
| 0014 <sub>16</sub> |  | 0034 <sub>16</sub> | AD/DA control register (ADCON)              |
| 0015 <sub>16</sub> |  | 0035 <sub>16</sub> | A-D conversion register (AD)                |
| 0016 <sub>16</sub> |  | 0036 <sub>16</sub> | D-A1 conversion register (DA1)              |
| 0017 <sub>16</sub> |  | 0037 <sub>16</sub> | D-A2 conversion register (DA2)              |
| 0018 <sub>16</sub> | Transmit/Receive buffer register (TB/RB) | 0038 <sub>16</sub> |   |
| 0019 <sub>16</sub> | Serial I/O1 status register (SIO1STS)    | 0039 <sub>16</sub> |   |
| 001A <sub>16</sub> | Serial I/O1 control register (SIO1CON)   | 003A <sub>16</sub> | Interrupt edge selection register (INTEDGE) |
| 001B <sub>16</sub> | UART control register (UARTCON)          | 003B <sub>16</sub> | CPU mode register (CPUM)                    |
| 001C <sub>16</sub> | Baud rate generator (BRG)                | 003C <sub>16</sub> | Interrupt request register 1(IREQ1)         |
| 001D <sub>16</sub> | Serial I/O2 control register (SIO2CON)   | 003D <sub>16</sub> | Interrupt request register 2(IREQ2)         |
| 001E <sub>16</sub> |  | 003E <sub>16</sub> | Interrupt control register 1(ICON1)         |
| 001F <sub>16</sub> | Serial I/O2 register (SIO2)              | 003F <sub>16</sub> | Interrupt control register 2(ICON2)         |

Fig. 3 Memory map of special function register (SFR)

**I/O Ports**  
**Direction registers**

The 3802 group has 56 programmable I/O pins arranged in seven I/O ports (ports P0 to P6). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

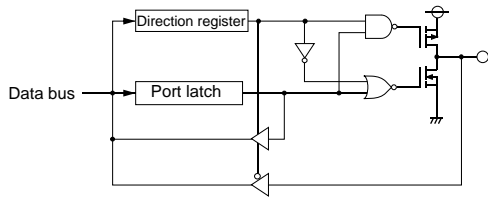
| Pin  | Name    | Input/Output                  | I/O Format   | Non-Port Function                | Related SFRs  | Ref.No.                    |
|--|---------|-------------------------------|--|----------------------------------|---|----------------------------|
| P00–P07  | Port P0 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | Address low-order byte output    | CPU mode register                                     | (1)                        |
| P10–P17  | Port P1 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | Address high-order byte output   | CPU mode register                                     |                            |
| P20–P27  | Port P2 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | Data bus I/O                     | CPU mode register                                     |                            |
| P30/DA1<br>P31/DA2<br>P32–P37  | Port P3 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | D-A conversion output            | AD/DA control register<br>CPU mode register           | (2)                        |
|  |         |                               |  | Control signal I/O               | CPU mode register                                     | (1)                        |
| P40/INT4,<br>P41/INT0,<br>P43/INT2<br>P44/RxD,<br>P45/TxD,<br>P46/SCLK1,<br>P47/SRDY1                | Port P4 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | External interrupt input         | Interrupt edge selection register                     | (3)                        |
|  |         |                               |  | Serial I/O1 function I/O         | Serial I/O1 control register<br>UART control register | (4)<br>(5)<br>(6)<br>(7)   |
| P50/SIN2,<br>P51/SOUT2,<br>P52/SCLK2,<br>P53/SRDY2<br>P54/CNTR0,<br>P55/CNTR1<br>P56/PWM<br>P57/INT3 | Port P5 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | Serial I/O2 function I/O         | Serial I/O2 control register                          | (8)<br>(9)<br>(10)<br>(11) |
|  |         |                               |  | Timer X and Timer Y function I/O | Timer XY mode register                                | (12)                       |
|  |         |                               |  | PWM output                       | PWM control register                                  | (13)                       |
|  |         |                               |  | External interrupt input         | Interrupt edge selection register                     | (3)                        |
| P60/AN0–<br>P67/AN7  | Port P6 | Input/output, individual bits | CMOS 3-state output<br>CMOS compatible input level | A-D conversion input             |   | (14)                       |

**Note 1:** For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, refer to the applicable sections.

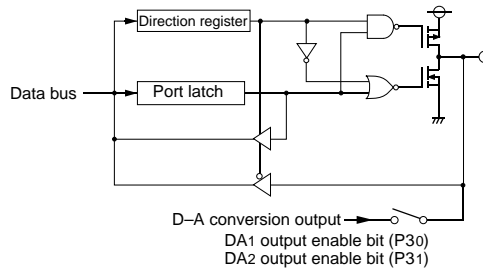
**2:** Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

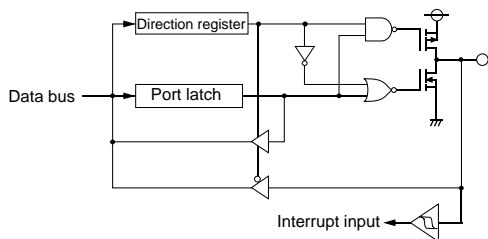
(1) Ports P0, P1, P2, P32-P37



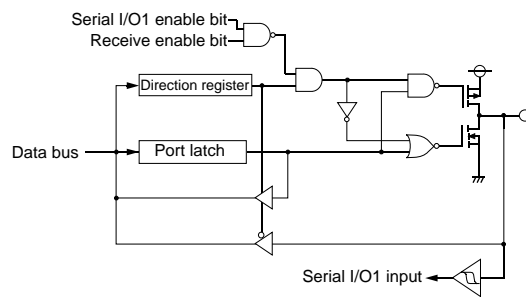
(2) Ports P30, P31



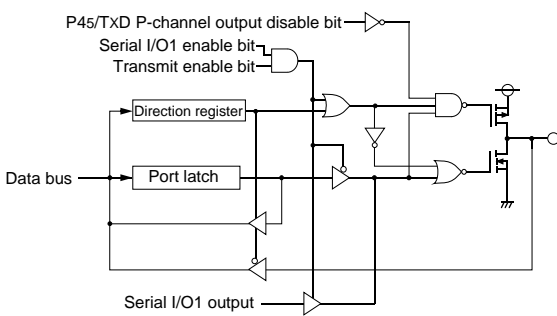
(3) Ports P40-P43, P57



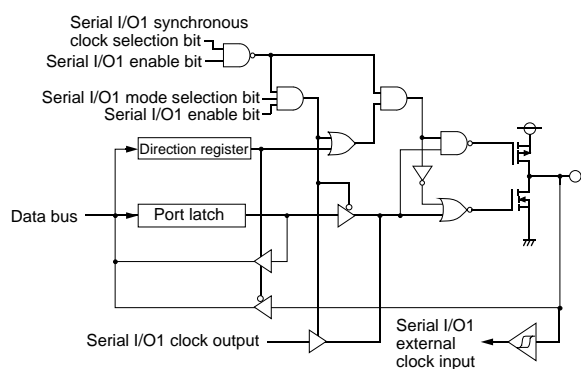
(4) Port P44



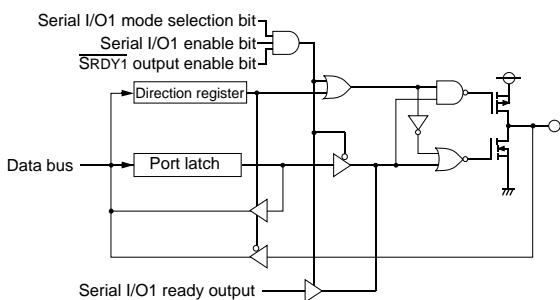
(5) Port P45



(6) Port P46



(7) Port P47



(8) Port P50

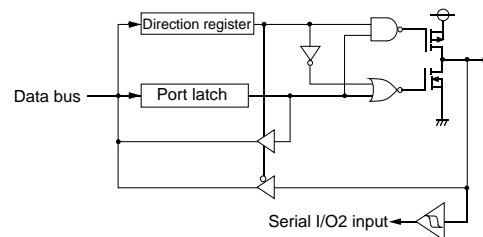


Fig. 4 Port block diagram (single-chip mode) (1)

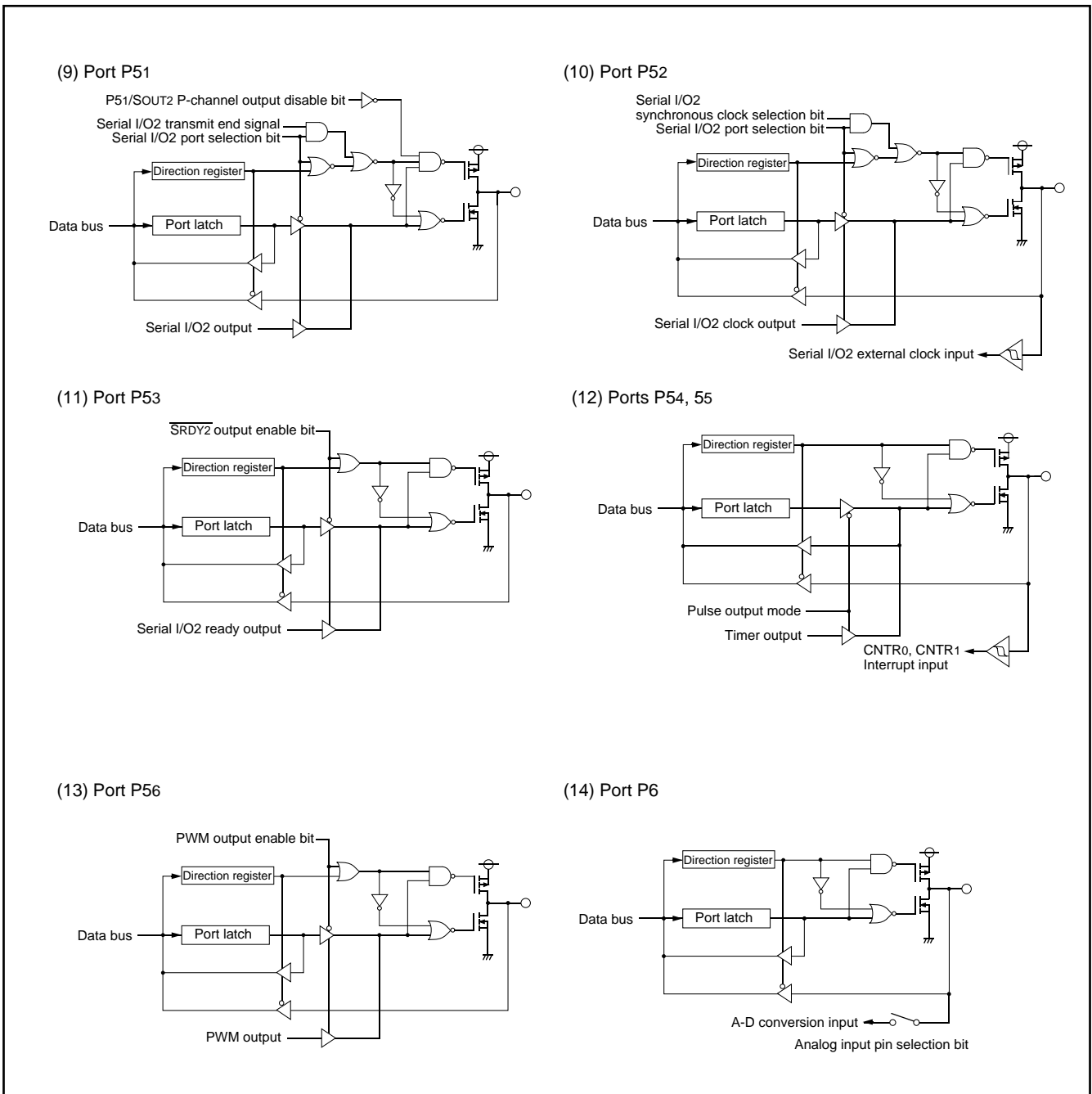


Fig. 5 Port block diagram (single-chip mode) (2)

## INTERRUPTS

Interrupts occur by sixteen sources: seven external, eight internal, and one software.

### Interrupt control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

### Interrupt operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

### Notes on use

When the active edge of an external interrupt (INT<sub>0</sub> to INT<sub>4</sub>, CNTR<sub>0</sub>, or CNTR<sub>1</sub>) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge selection.
- (3) Clear the interrupt request bit which is selected to "0".
- (4) Enable the external interrupt which is selected.

**Table 1. Interrupt vector addresses and priority**

| Interrupt Source         | Priority | Vector Addresses (Note 1) |                    | Interrupt Request Generating Conditions  | Remarks                                     |
|--------------------------|----------|---------------------------|--------------------|--|---|
|                          |          | High                      | Low                |  |   |
| Reset (Note 2)           | 1        | FFFD <sub>16</sub>        | FFFC <sub>16</sub> | At reset   | Non-maskable                                |
| INT <sub>0</sub>         | 2        | FFFB <sub>16</sub>        | FFFA <sub>16</sub> | At detection of either rising or falling edge of INT <sub>0</sub> input          | External interrupt (active edge selectable) |
| INT <sub>1</sub>         | 3        | FFF9 <sub>16</sub>        | FFF8 <sub>16</sub> | At detection of either rising or falling edge of INT <sub>1</sub> input          | External interrupt (active edge selectable) |
| Serial I/O1 reception    | 4        | FFF7 <sub>16</sub>        | FFF6 <sub>16</sub> | At completion of serial I/O1 data reception                                      | Valid when serial I/O1 is selected          |
| Serial I/O1 transmission | 5        | FFF5 <sub>16</sub>        | FFF4 <sub>16</sub> | At completion of serial I/O1 transfer shift or when transmission buffer is empty | Valid when serial I/O1 is selected          |
| Timer X                  | 6        | FFF3 <sub>16</sub>        | FFF2 <sub>16</sub> | At timer X underflow   |   |
| Timer Y                  | 7        | FFF1 <sub>16</sub>        | FFF0 <sub>16</sub> | At timer Y underflow   |   |
| Timer 1                  | 8        | FFEF <sub>16</sub>        | FFEE <sub>16</sub> | At timer 1 underflow   | STP release timer underflow                 |
| Timer 2                  | 9        | FFED <sub>16</sub>        | FFEC <sub>16</sub> | At timer 2 underflow   |   |
| CNTR <sub>0</sub>        | 10       | FFEB <sub>16</sub>        | FFEA <sub>16</sub> | At detection of either rising or falling edge of CNTR <sub>0</sub> input         | External interrupt (active edge selectable) |
| CNTR <sub>1</sub>        | 11       | FFE9 <sub>16</sub>        | FFE8 <sub>16</sub> | At detection of either rising or falling edge of CNTR <sub>1</sub> input         | External interrupt (active edge selectable) |
| Serial I/O2              | 12       | FFE7 <sub>16</sub>        | FFE6 <sub>16</sub> | At completion of serial I/O2 data transfer                                       | Valid when serial I/O2 is selected          |
| INT <sub>2</sub>         | 13       | FFE5 <sub>16</sub>        | FFE4 <sub>16</sub> | At detection of either rising or falling edge of INT <sub>2</sub> input          | External interrupt (active edge selectable) |
| INT <sub>3</sub>         | 14       | FFE3 <sub>16</sub>        | FFE2 <sub>16</sub> | At detection of either rising or falling edge of INT <sub>3</sub> input          | External interrupt (active edge selectable) |
| INT <sub>4</sub>         | 15       | FFE1 <sub>16</sub>        | FFE0 <sub>16</sub> | At detection of either rising or falling edge of INT <sub>4</sub> input          | External interrupt (active edge selectable) |
| A-D converter            | 16       | FFDF <sub>16</sub>        | FFDE <sub>16</sub> | At completion of A-D conversion  |   |
| BRK instruction          | 17       | FFDD <sub>16</sub>        | FFDC <sub>16</sub> | At BRK instruction execution   | Non-maskable software interrupt             |

**Note 1:** Vector addresses contain interrupt jump destination addresses.

**Note 2:** Reset function in the same way as an interrupt with the highest priority.

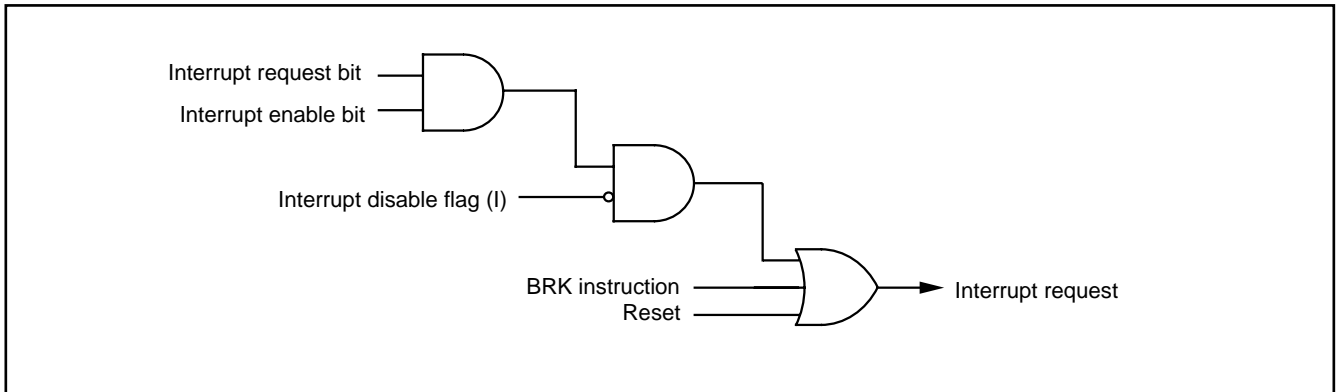


Fig. 6 Interrupt control

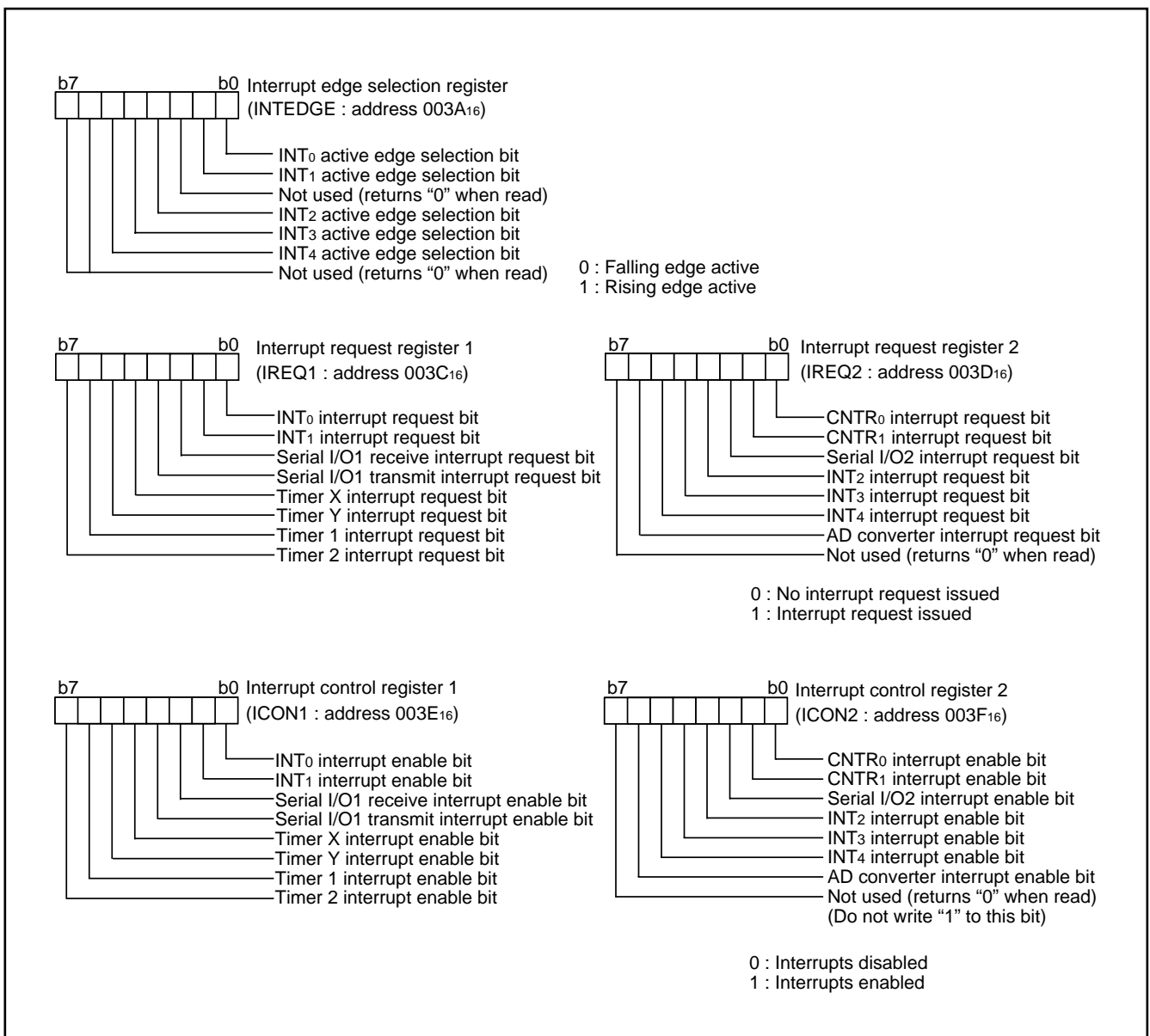


Fig. 7 Structure of interrupt-related registers

**Timers**

The 3802 group has four timers: timer X, timer Y, timer 1, and timer 2.

All timers are count down. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

The division ratio of each timer or prescaler is given by  $1/(n + 1)$ , where n is the value in the corresponding timer or prescaler latch.

**Timer 1 and Timer 2**

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

**Timer X and Timer Y**

Timer X and Timer Y can each be selected in one of four operating modes by setting the timer XY mode register.

**Timer Mode**

The timer counts  $f(XIN)/16$  in timer mode.

**Pulse Output Mode**

Timer X (or timer Y) counts  $f(XIN)/16$ . Whenever the contents of the timer reach "0016", the signal output from the CNTR0 (or CNTR1) pin is inverted. If the CNTR0 (or CNTR1) active edge switch bit is "0", output begins at "H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P54 ( or port P55) direction register to output mode.

**Event Counter Mode**

Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the CNTR0 or CNTR1 pin.

**Pulse Width Measurement Mode**

If the CNTR0 (or CNTR1) active edge selection bit is "0", the timer counts at the oscillation frequency divided by 16 while the CNTR0 (or CNTR1) pin is at "H". If the CNTR0 (or CNTR1) active edge switch bit is "1", the count continues during the time that the CNTR0 (or CNTR1) pin is at "L".

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer underflows, the corresponding interrupt request bit is set.

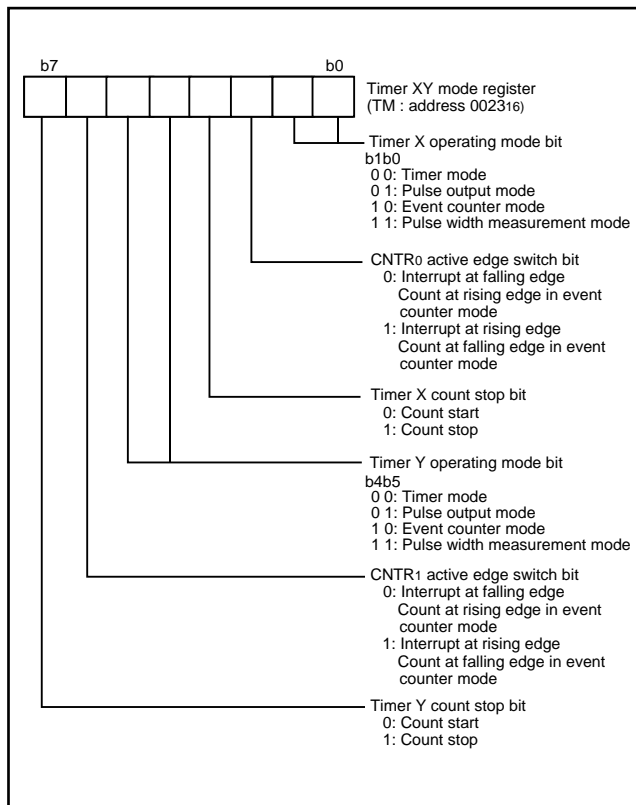


Fig. 8 Structure of timer XY register



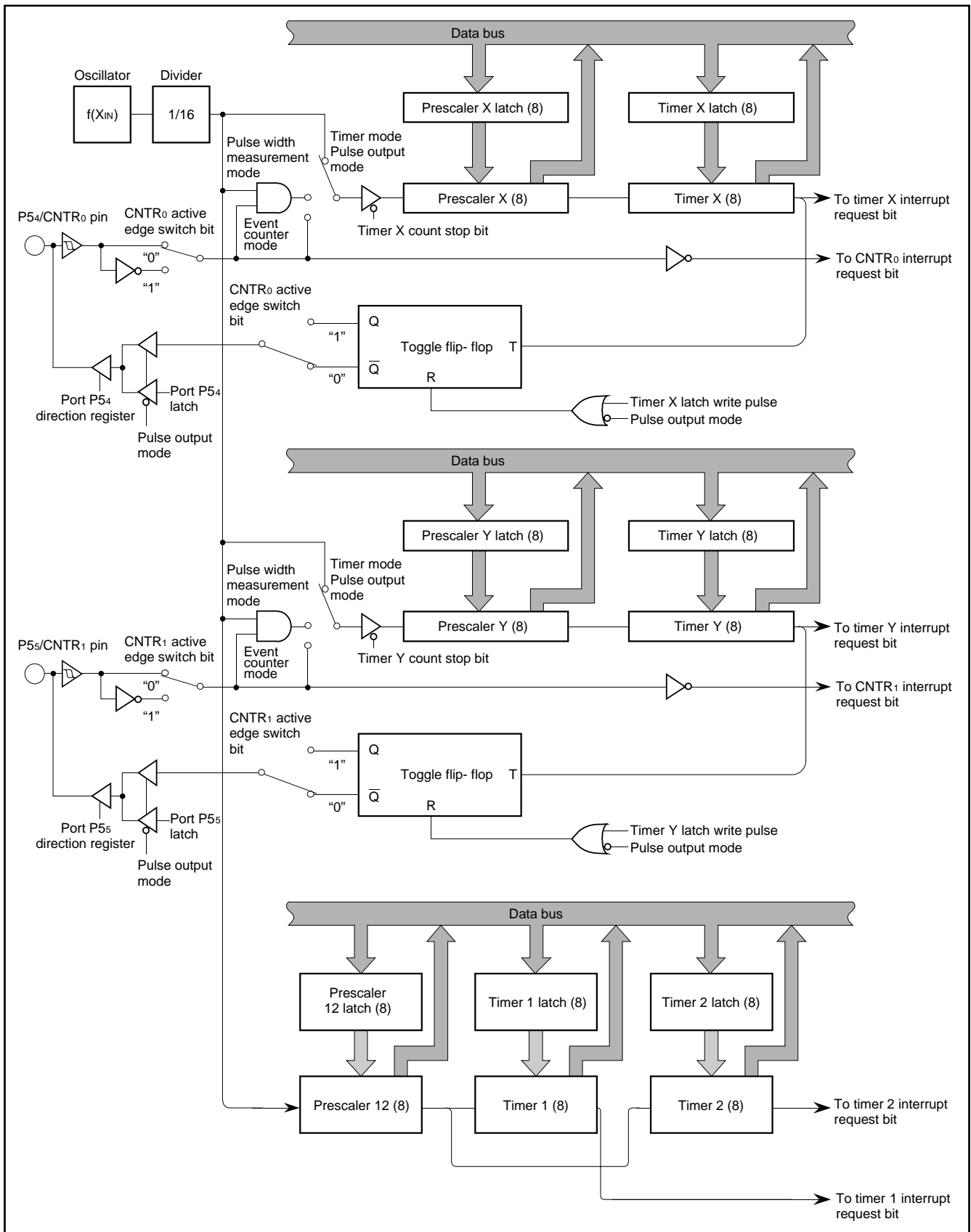


Fig. 9 Block diagram of timer X, timer Y, timer 1, and timer 2

**Serial I/O1**

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

**Clock synchronous serial I/O mode**

Clock synchronous serial I/O1 mode can be selected by setting the mode selection bit of the serial I/O1 control register to "1". For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 001816).

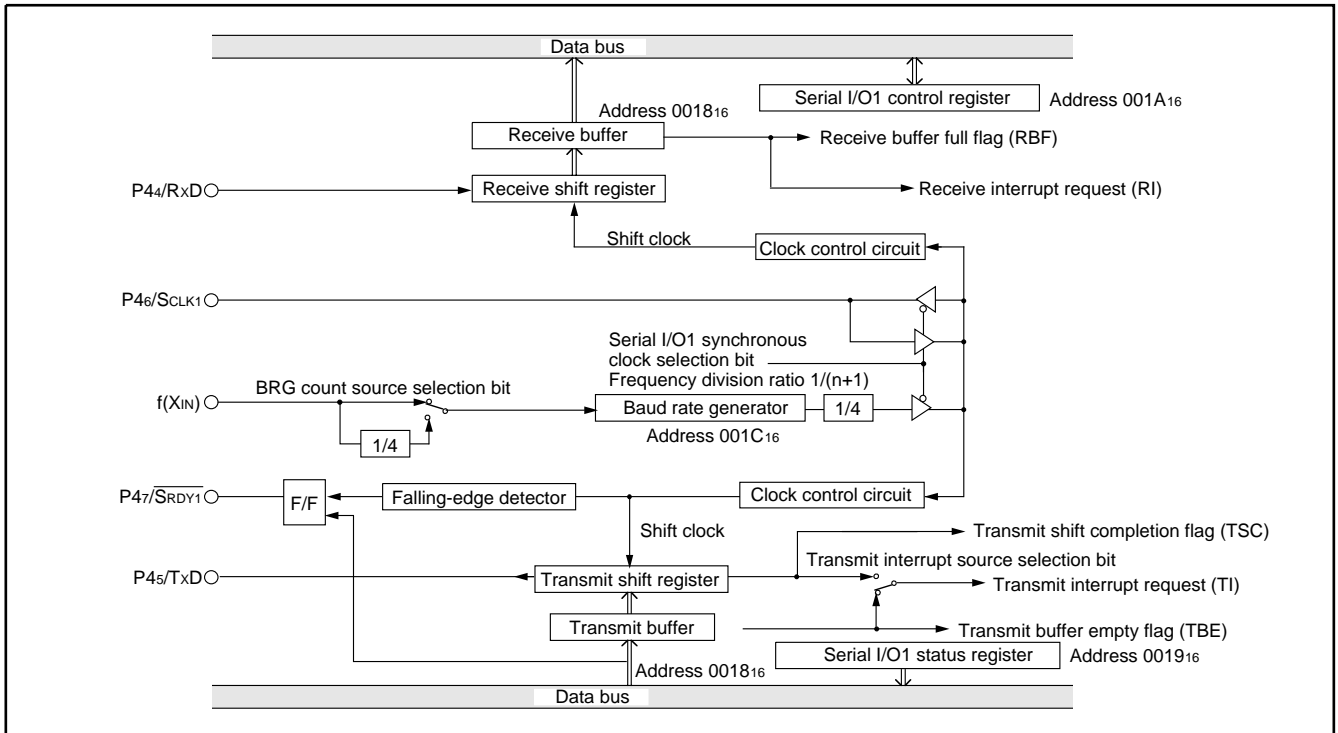


Fig. 10 Block diagram of clock synchronous serial I/O1

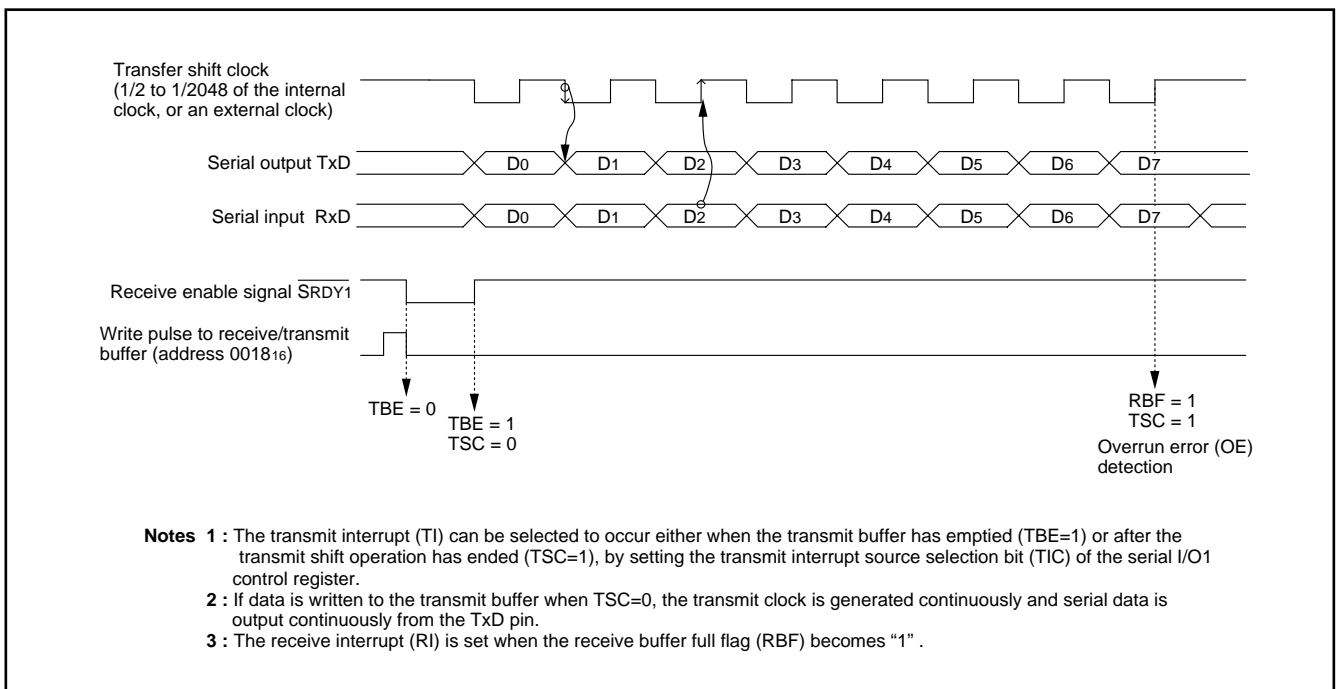


Fig. 11 Operation of clock synchronous serial I/O1 function

**Asynchronous serial I/O (UART) mode**

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

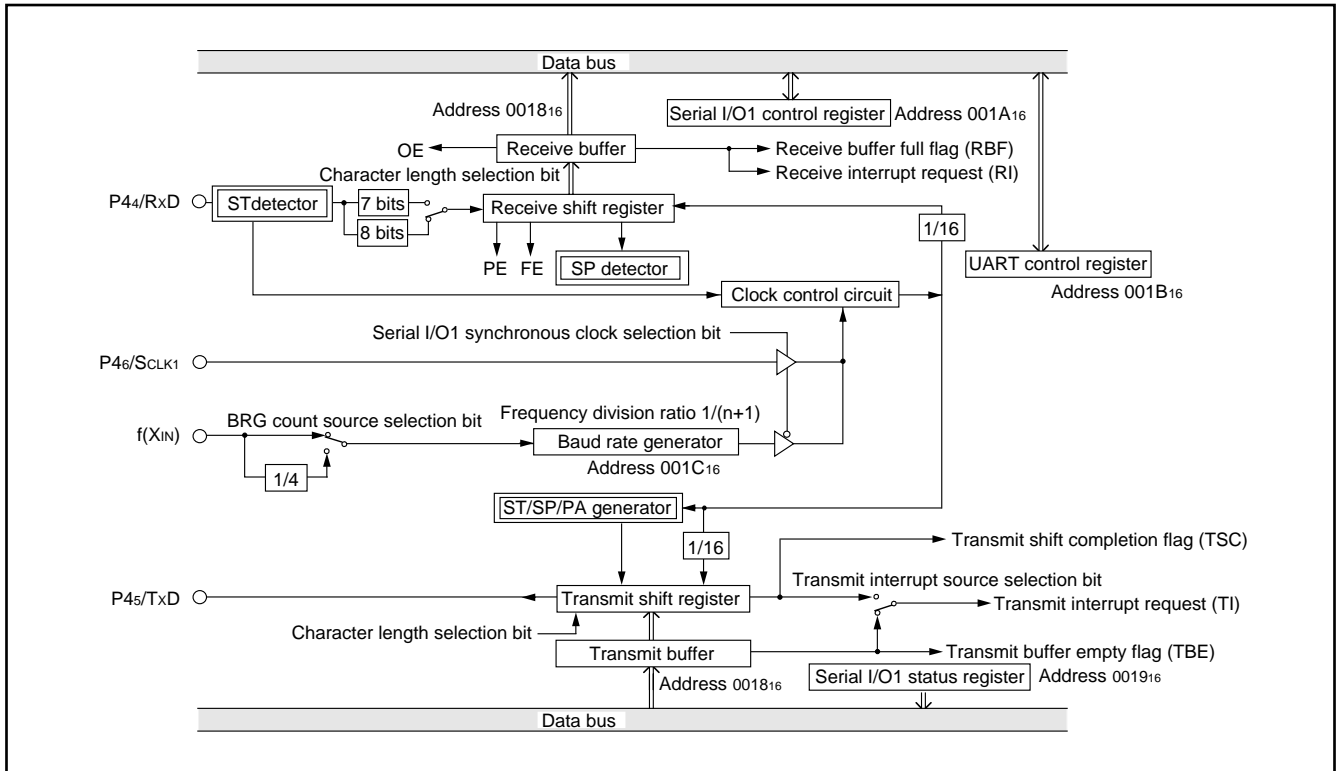


Fig. 12 Block diagram of UART serial I/O

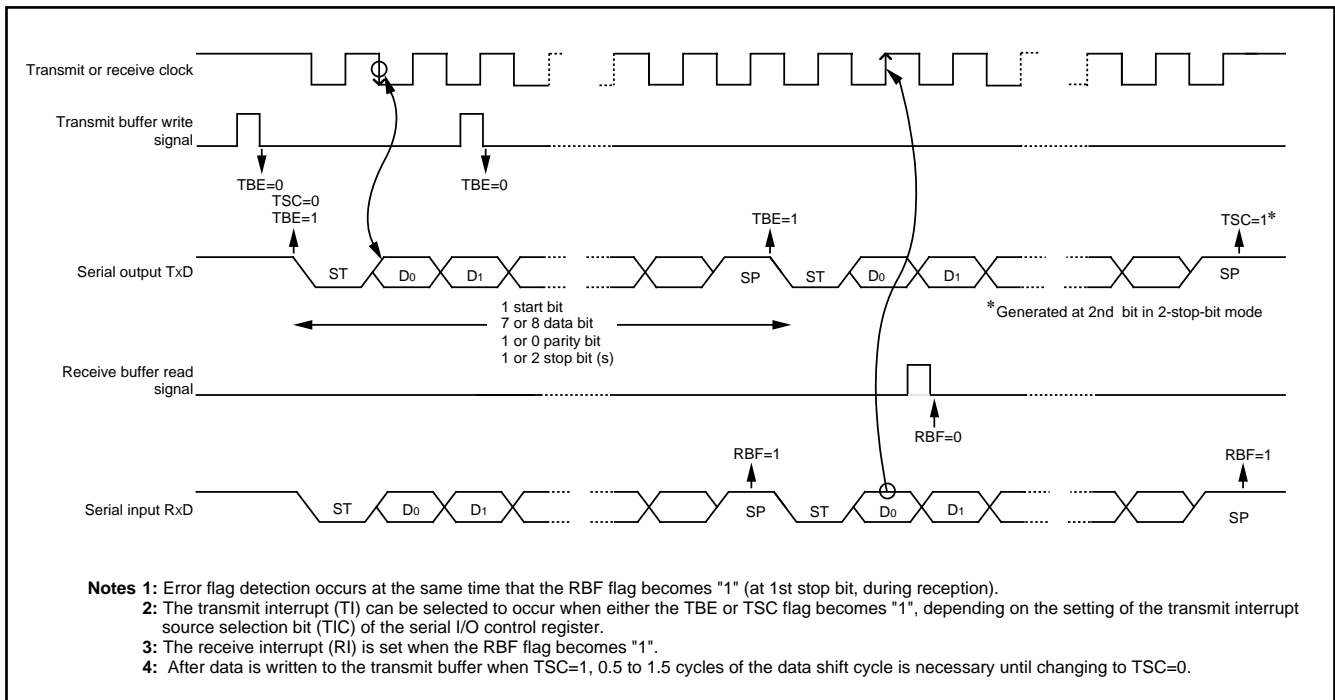


Fig. 13 Operation of UART serial I/O function

### Serial I/O1 control register (SIO1CON) 001A16

The serial I/O control register consists of eight control bits for the serial I/O function.

### UART control register (UARTCON) 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD pin.

### Serial I/O1 status register (SIO1STS) 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, re-

spectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

### Transmit buffer/Receive buffer register (TB/RB) 001816

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

### Baud rate generator (BRG) 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where  $n$  is the value written to the baud rate generator.

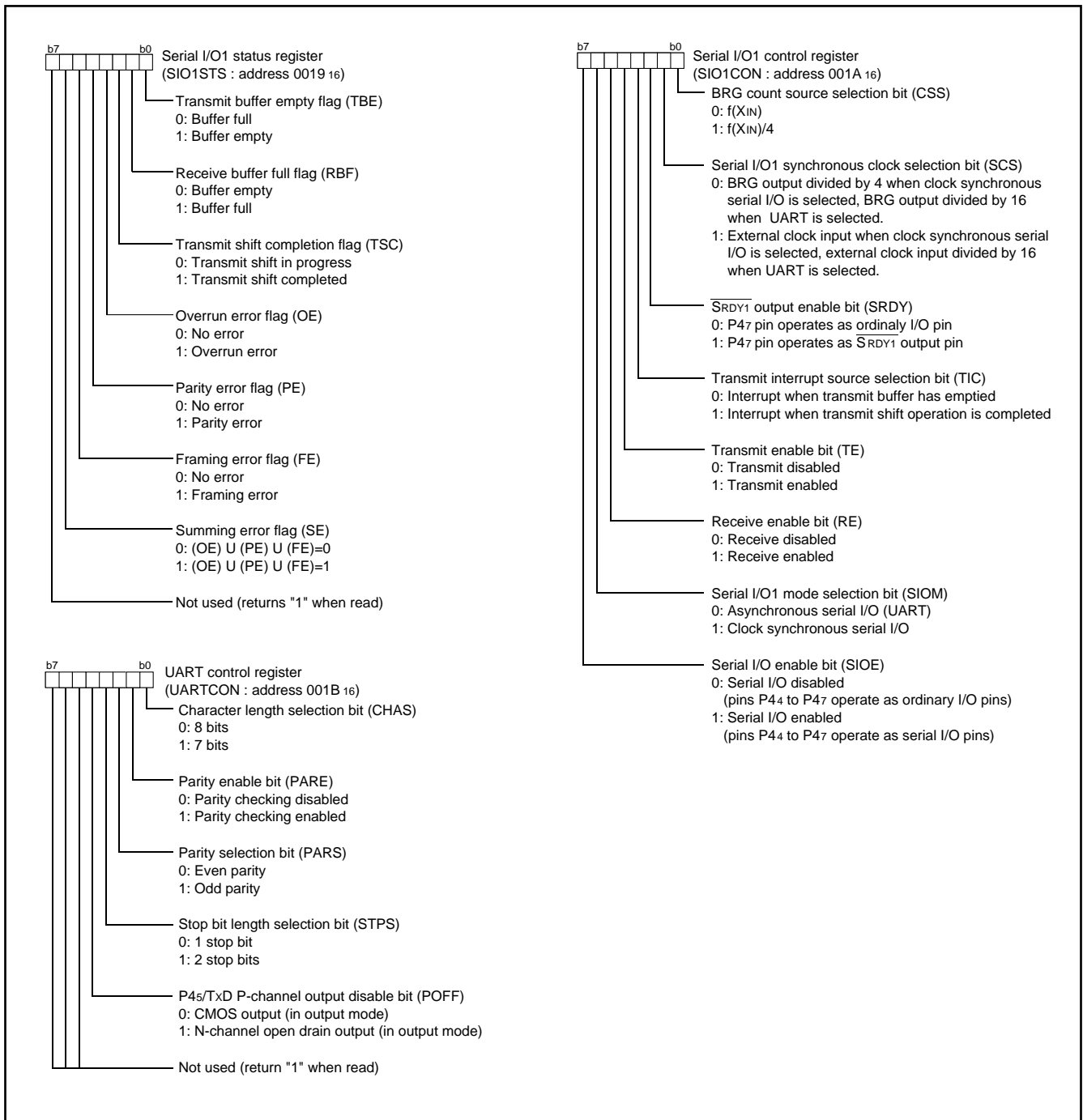


Fig. 14 Structure of serial I/O control registers

**Serial I/O2**

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

**Serial I/O2 control register (SIO2CON) 001D16**

The serial I/O2 control register contains seven bits which control various serial I/O functions.

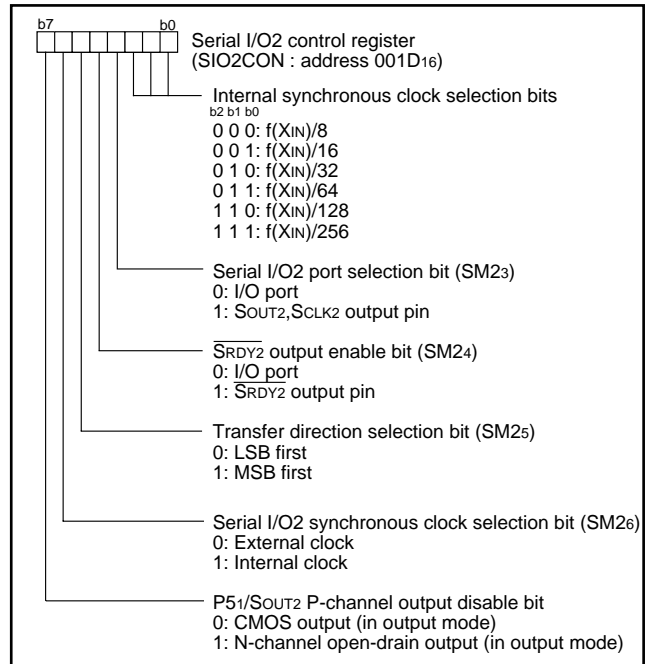


Fig. 15 Structure of serial I/O2 control register

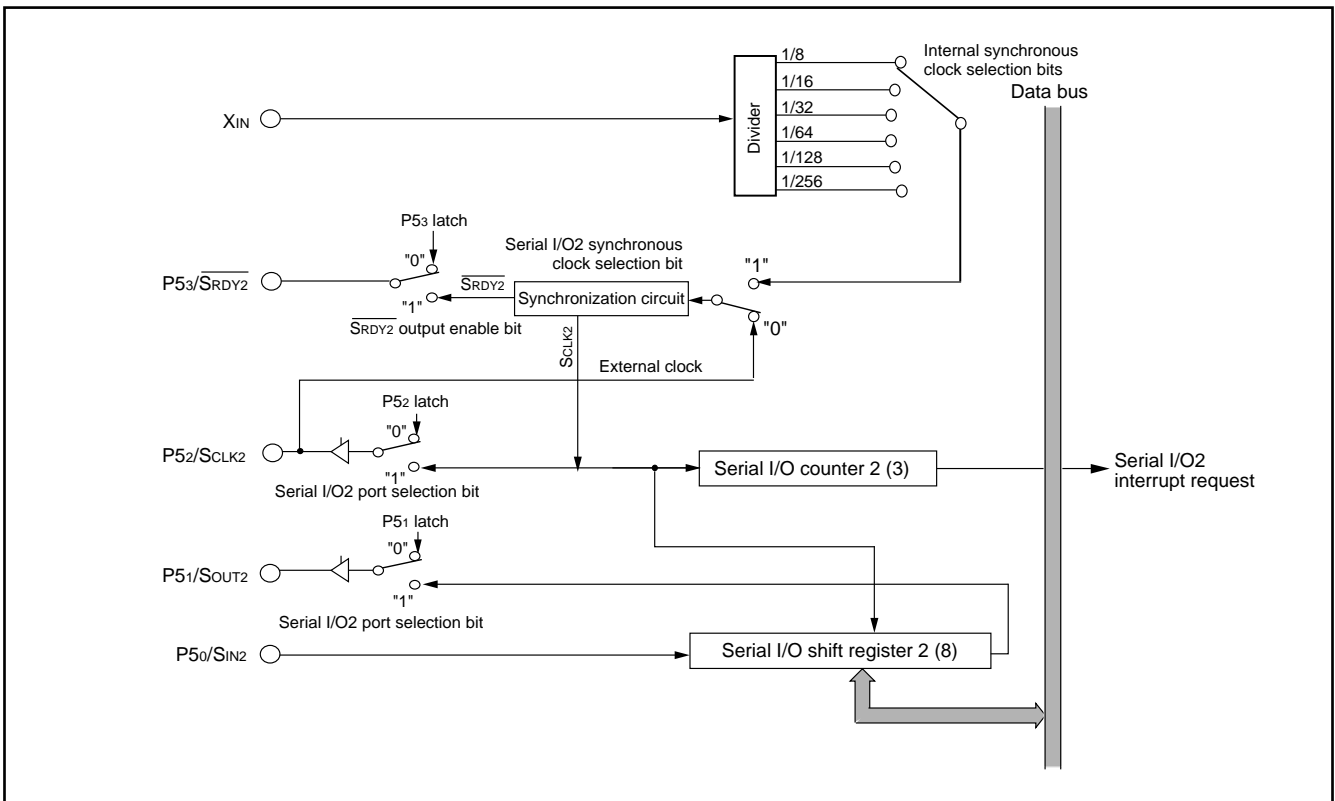


Fig. 16 Block diagram of serial I/O2 function

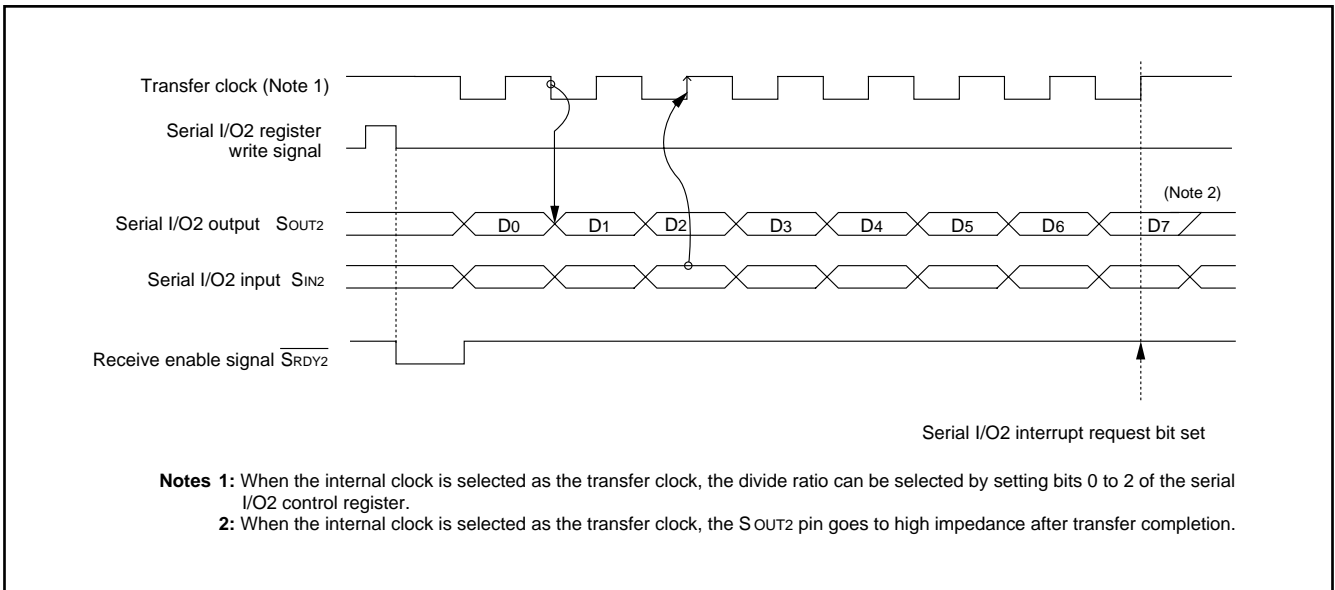


Fig. 17 Timing of serial I/O2 function

**PULSE WIDTH MODULATION (PWM)**

The 3802 group has a PWM function with an 8-bit resolution, based on a signal that is the clock input X<sub>IN</sub> or that clock input divided by 2.

**Data Setting**

The PWM output pin also functions as port P5<sub>6</sub>. Set the PWM period by the PWM prescaler, and set the period during which the output pulse is an "H" by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1) / f(X_{IN}) \\ &= 51 \times (n+1) \mu\text{s (when } X_{IN} = 5 \text{ MHz)} \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" period} &= \text{PWM period} \times m / 255 \\ &= 0.2 \times (n+1) \times m \mu\text{s} \\ &\text{(when } X_{IN} = 5 \text{ MHz)} \end{aligned}$$

**PWM Operation**

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

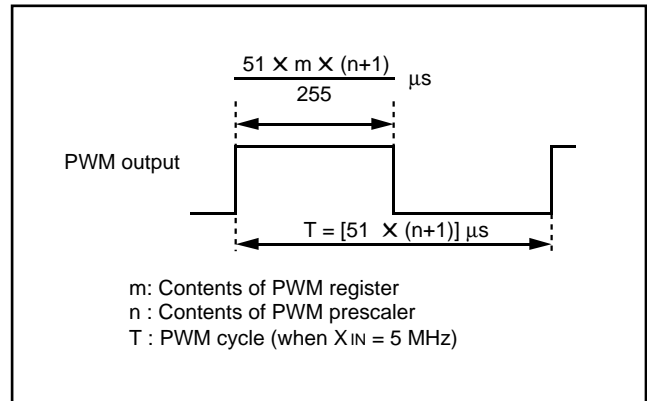


Fig. 18 Timing of PWM cycle

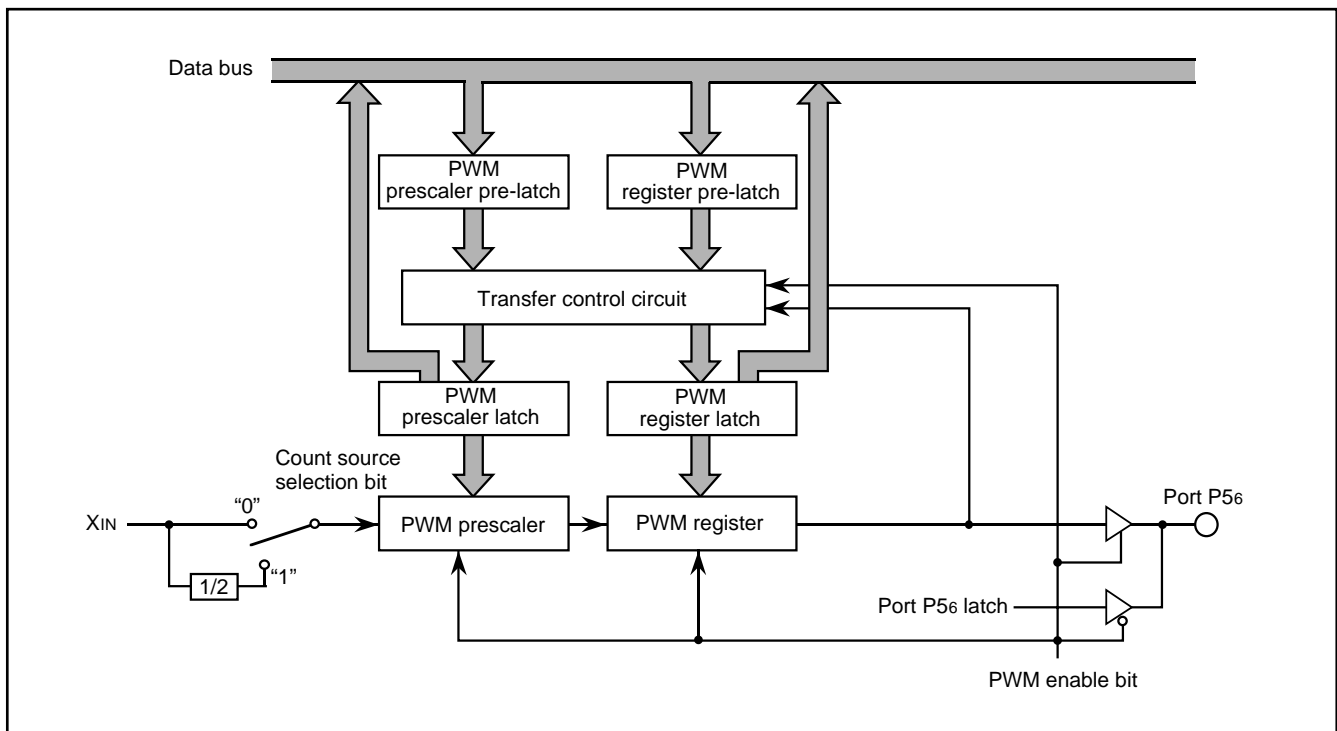


Fig. 19 Block diagram of PWM function



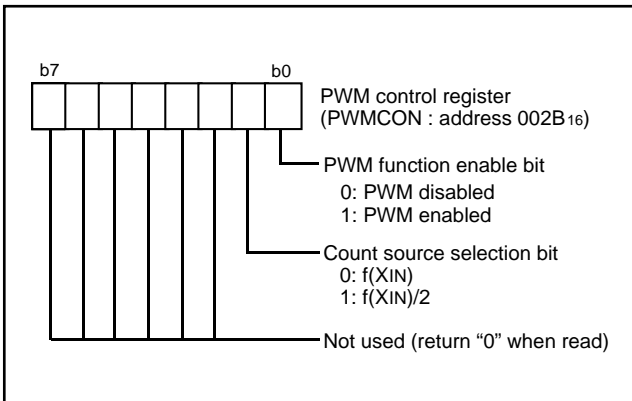


Fig. 20 Structure of PWM control register

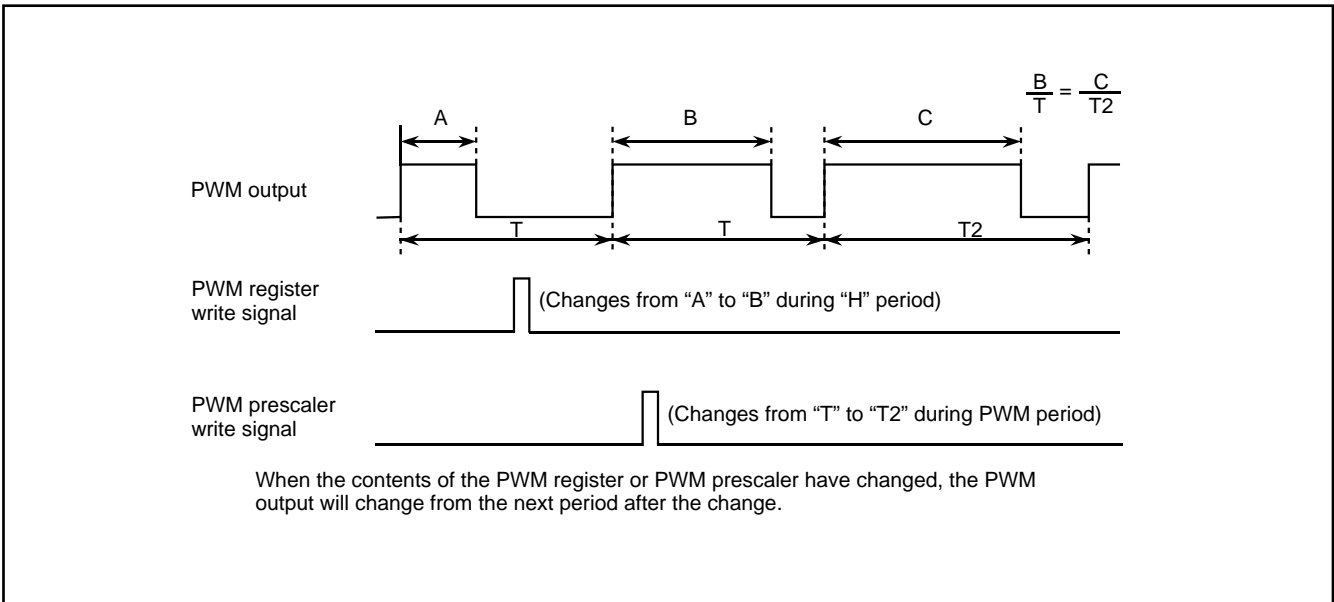


Fig. 21 PWM output timing when PWM register or PWM prescaler is changed

**A-D Converter**

The functional blocks of the A-D converter are described below.

**[A-D conversion register]**

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

**[AD/DA control register]**

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bits 6 and 7 are used to control the output of the D-A converter.

**[Comparison voltage generator]**

The comparison voltage generator divides the voltage between AVSS and VREF into 256, and outputs the divided voltages.

**[Channel selector]**

The channel selector selects one of the ports P60/AN0 to P67/AN7, and inputs the voltage to the comparator.

**[Comparator and Control circuit]**

The comparator and control circuit compares an analog input voltage with the comparison voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to 500 kHz or more during an A-D conversion.

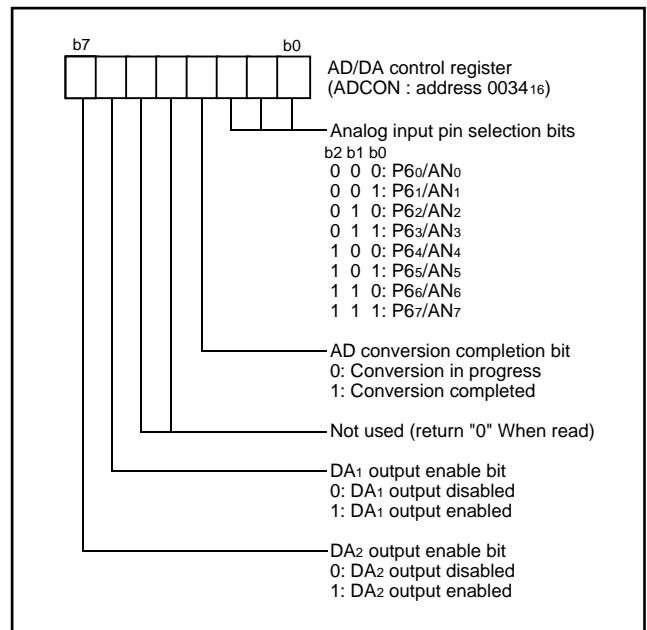


Fig.22 Structure of AD/DA control register

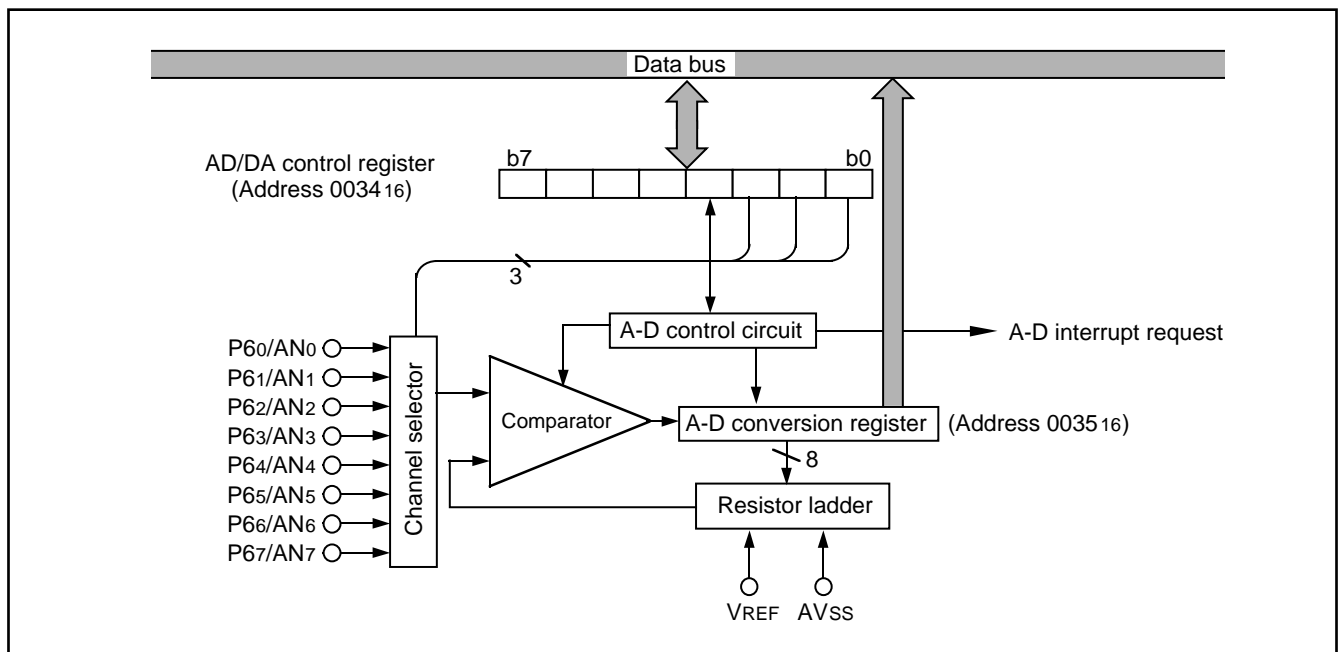


Fig. 23 Block diagram of A-D converter

**D-A Converter**

The 3802 group has two internal D-A converters (DA1 and DA2) with 8-bit resolutions.

The D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from the DA1 or DA2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit (P30/DA1 or P31/DA2) should be set to "0" (input status).

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n = 0 \text{ to } 255)$$

Where VREF is the reference voltage.

At reset, the D-A conversion registers are cleared to "0016", the DA output enable bits are cleared to "0", and the P30/DA1 and P31/DA2 pins are set to input (high impedance).

The D-A output is not buffered, so connect an external buffer when driving a low-impedance load.

Set VCC to 3.0 V or more when using the D-A converter.

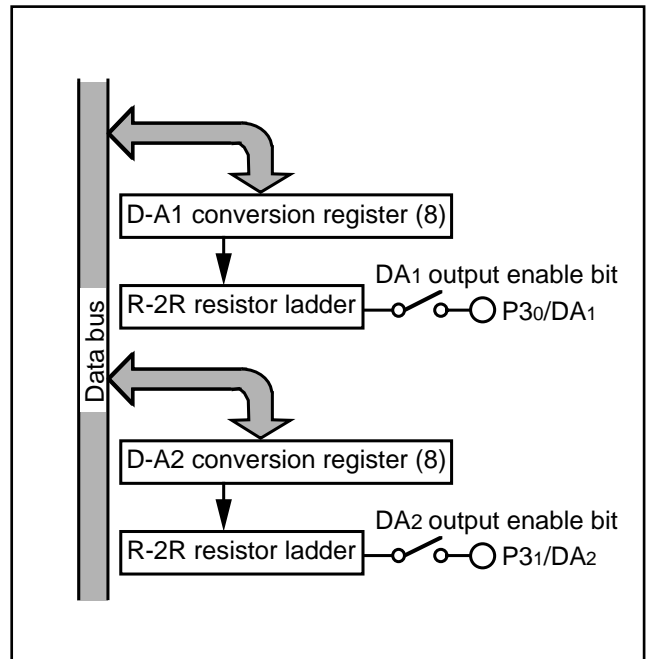


Fig. 24 Block diagram of D-A converter

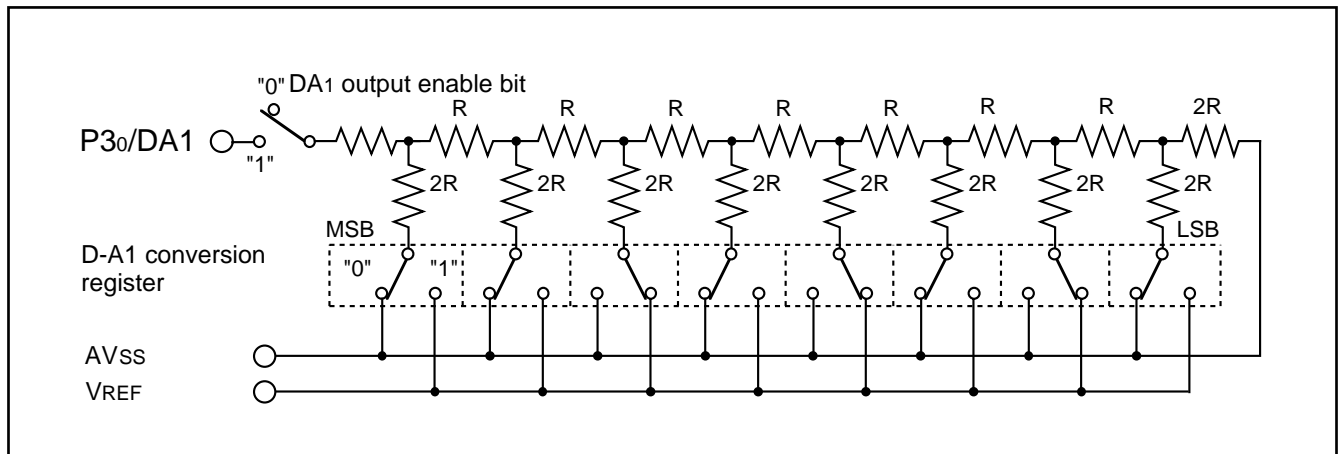


Fig. 25 Equivalent connection circuit of D-A converter

**Reset Circuit**

To reset the microcomputer, the  $\overline{\text{RESET}}$  pin should be held at an "L" level for 2  $\mu\text{s}$  or more. Then the  $\overline{\text{RESET}}$  pin is returned to an "H" level (the power source voltage should be between 4.0 V and 5.5 V), reset is released. Internal operation begin until after 8 to 13  $X_{\text{IN}}$  clock cycles are completed. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (high-order byte) and address  $\text{FFFC}_{16}$  (low-order byte).

Make sure that the reset input voltage is less than 0.6 V for  $V_{\text{CC}}$  of 3.0 V (Extended operating temperature version : the reset input voltage is less than 0.8 V for  $V_{\text{CC}}$  of 4.0 V).

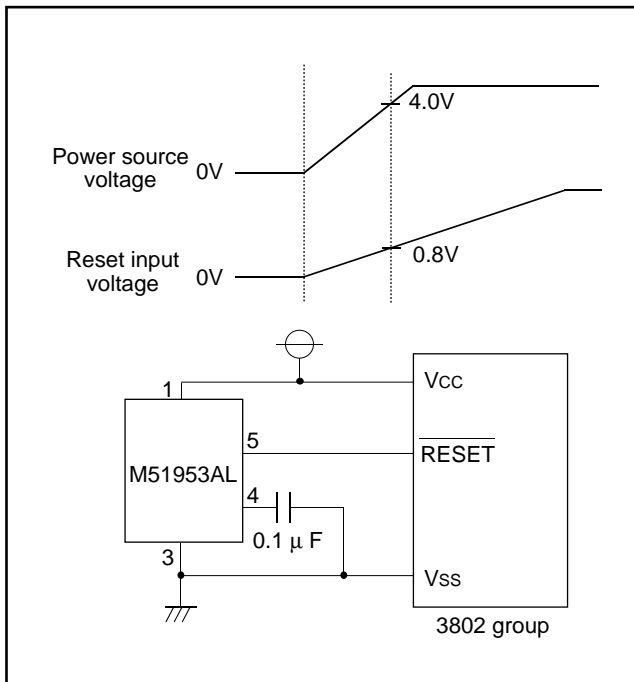


Fig. 26 Example of reset circuit

|  | Address                   | Register contents                      |
|--|---------------------------|--|
| (1) Port P0 direction register         | (0001 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (2) Port P1 direction register         | (0003 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (3) Port P2 direction register         | (0005 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (4) Port P3 direction register         | (0007 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (5) Port P4 direction register         | (0009 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (6) Port P5 direction register         | (000B <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (7) Port P6 direction register         | (000D <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (8) Serial I/O1 status register        | (0019 <sub>16</sub> ) ··· | 1 0 0 0 0 0 0 0                        |
| (9) Serial I/O1 control register       | (001A <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (10) UART control register             | (001B <sub>16</sub> ) ··· | 1 1 1 1 0 0 0 0                        |
| (11) Serial I/O2 control register      | (001D <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (12) Prescaler 12                      | (0020 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (13) Timer 1                           | (0021 <sub>16</sub> ) ··· | 01 <sub>16</sub>                       |
| (14) Timer 2                           | (0022 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (15) Timer XY mode register            | (0023 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (16) Prescaler X                       | (0024 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (17) Timer X                           | (0025 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (18) Prescaler Y                       | (0026 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (19) Timer Y                           | (0027 <sub>16</sub> ) ··· | FF <sub>16</sub>                       |
| (20) PWM control register              | (002B <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (21) AD/DA control register            | (0034 <sub>16</sub> ) ··· | 0 0 0 0 0 1 0 0                        |
| (22) D-A1 conversion register          | (0036 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (23) D-A2 conversion register          | (0037 <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (24) Interrupt edge selection register | (003A <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (25) CPU mode register                 | (003B <sub>16</sub> ) ··· | 0 0 0 0 0 0 0 *                        |
| (26) Interrupt request register 1      | (003C <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (27) Interrupt request register 2      | (003D <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (28) Interrupt control register 1      | (003E <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (29) Interrupt control register 2      | (003F <sub>16</sub> ) ··· | 00 <sub>16</sub>                       |
| (30) Processor status register         | (PS)                      | x x x x x 1 x x                        |
| (31) Program counter                   | (PC <sub>H</sub> )        | Contents of address $\text{FFFD}_{16}$ |
|  | (PC <sub>L</sub> )        | Contents of address $\text{FFFC}_{16}$ |

Note. x : Undefined  
 \* : The initial values of CM<sub>1</sub> are determined by the level at the CNV<sub>SS</sub> pin.  
 The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software.

Fig. 27 Internal status of microcomputer after reset

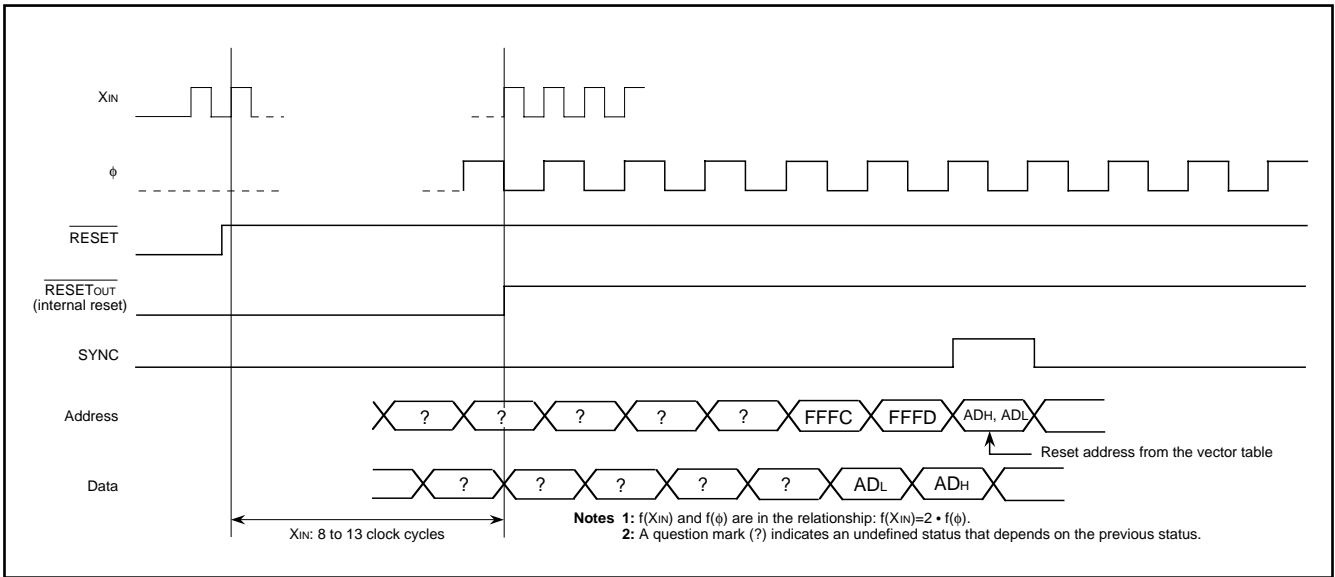


Fig. 28 Timing of reset

**Clock Generating Circuit**

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT. To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open.

**Oscillation control**

**Stop Mode**

If the STP instruction is executed, the internal clock  $\phi$  stops at an "H". Timer 1 is set to "0116" and prescaler 12 is set to "FF16". Oscillator restarts when an external interrupt is received, but the internal clock  $\phi$  remains at an "H" until timer 1 underflow. This allows time for the clock circuit oscillation to stabilize. If oscillator is restarted by a reset, no wait time is generated, so keep the RESET pin at an "L" level until oscillation has stabilized.

**Wait Mode**

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 underflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

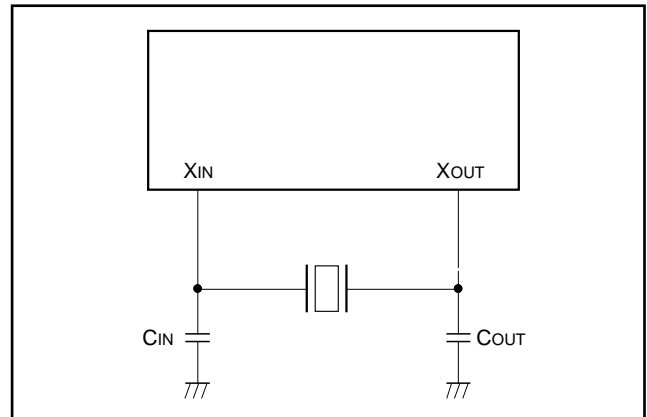


Fig. 29 Ceramic resonator circuit

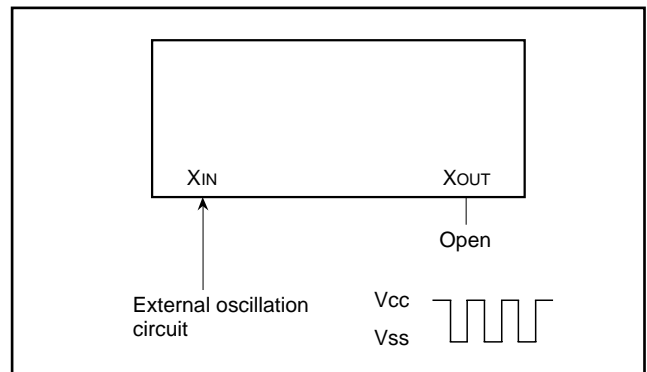


Fig. 30 External clock input circuit

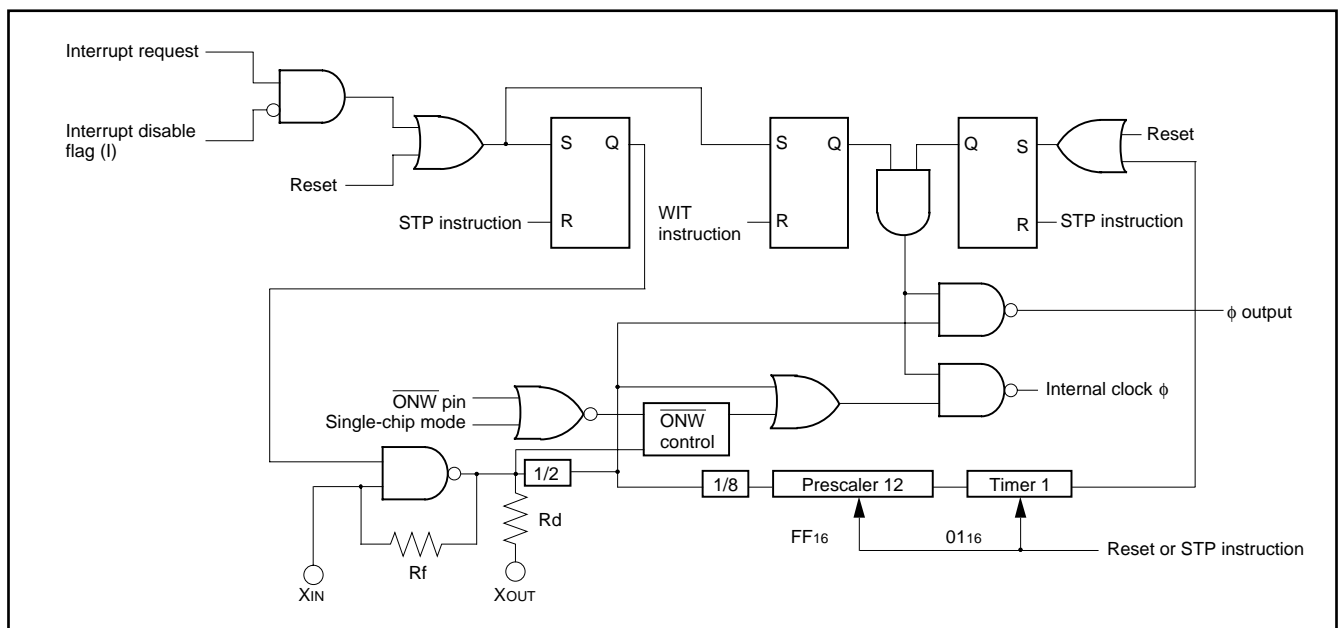


Fig. 31 Block diagram of clock generating circuit

**Processor Modes**

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM0 and CM1 (bits 0 and 1 of address 003B16). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

**Table 2. Functions of ports in memory expansion mode and microprocessor mode**

| Port Name | Function  |
|-----------|---|
| Port P0   | Outputs low-order byte of address.  |
| Port P1   | Outputs high-order byte of address.   |
| Port P2   | Operates as I/O pins for data D7 to D0 (including instruction codes).   |
| Port P3   | P30 and P31 function only as output pins (except that the port latch cannot be read).<br>P32 is the $\overline{ONW}$ input pin.<br>P33 is the $\overline{RESETOUT}$ output pin. (Note)<br>P34 is the $\phi$ output pin.<br>P35 is the SYNC output pin.<br>P36 is the $\overline{WR}$ output pin, and P37 is the $\overline{RD}$ output pin. |

**Note:** If CNVss is connected to Vss, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the  $\overline{RESETOUT}$  output pin.

**Single-Chip Mode**

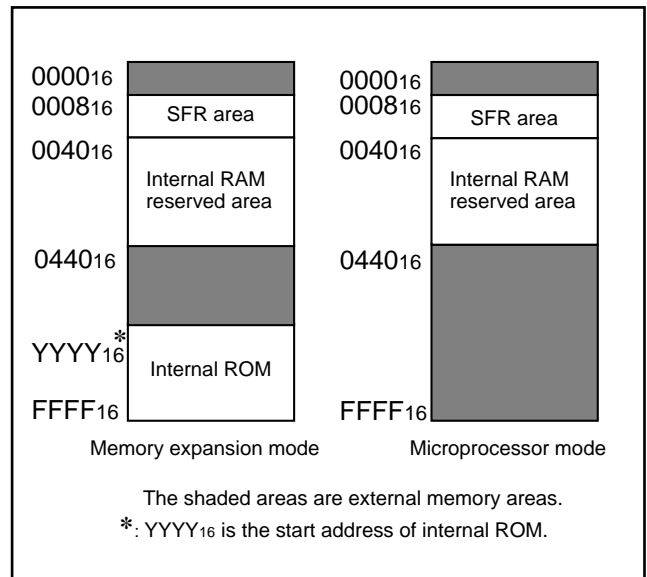
Select this mode by resetting the microcomputer with CNVss connected to Vss.

**Memory Expansion Mode**

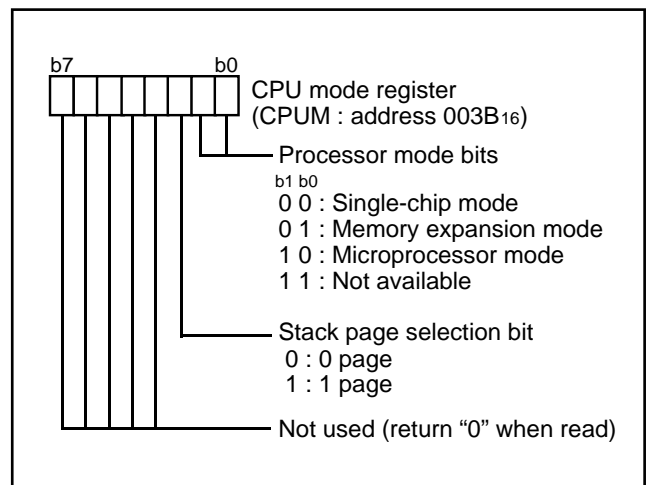
Select this mode by setting the processor mode bits to "01" in software with CNVss connected to Vss. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.

**Microprocessor Mode**

Select this mode by resetting the microcomputer with CNVss connected to Vcc, or by setting the processor mode bits to "10" in software with CNVss connected to Vss. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.



**Fig. 32 Memory maps in various processor modes**



**Fig. 33 Structure of CPU mode register**

**Bus control with memory expansion**

The 3802 group has a built-in  $\overline{\text{ONW}}$  function to facilitate access to external memory and I/O devices in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the  $\overline{\text{ONW}}$  pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of  $\phi$ . During this extended period, the  $\overline{\text{RD}}$  or  $\overline{\text{WR}}$  signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000<sub>16</sub> to 0007<sub>16</sub> and 0440<sub>16</sub> to FFFF<sub>16</sub> in microprocessor mode, 0440<sub>16</sub> to YYY<sub>16</sub> in memory expansion mode, and only read and write cycles are extended.

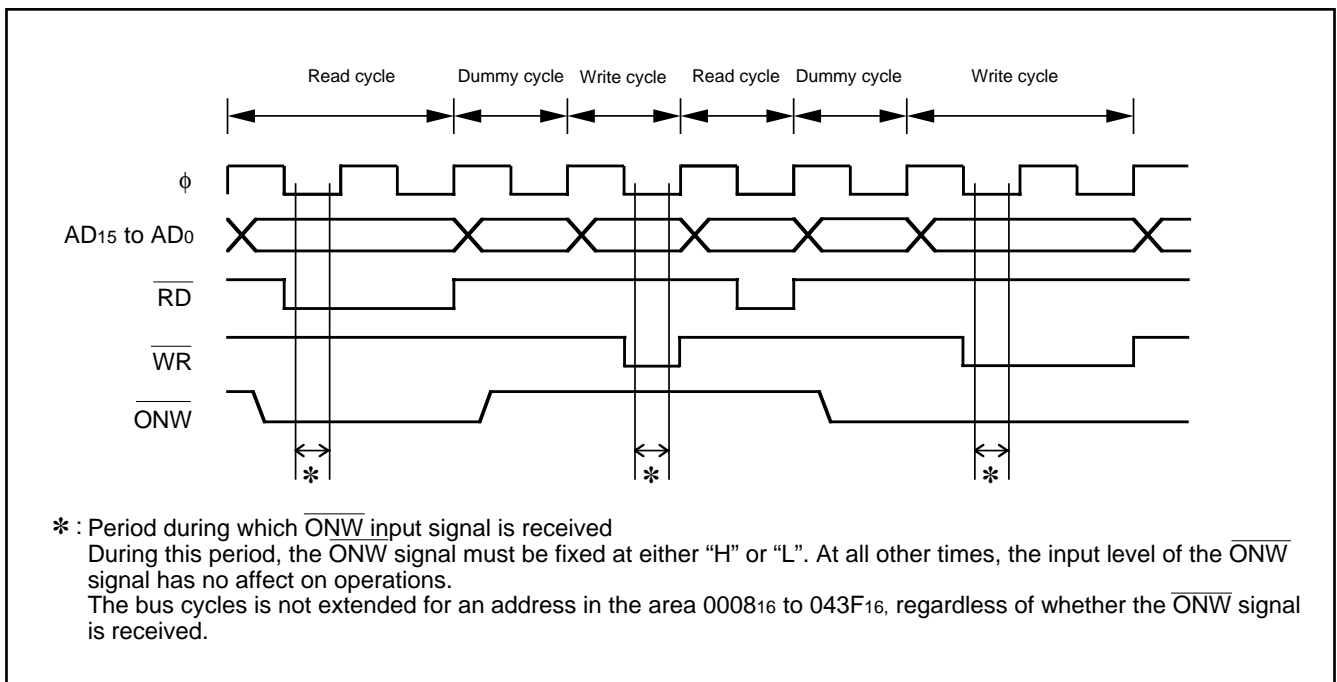


Fig. 34  $\overline{\text{ONW}}$  function timing



## NOTES ON PROGRAMMING

### Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.

In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

### Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

### Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

### Timers

If a value  $n$  (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n + 1)$ .

### Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

### Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

### Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the  $\overline{\text{SRDY}}_1$  signal, set the transmit enable bit, the receive enable bit, and the  $\overline{\text{SRDY}}_1$  output enable bit to "1".

Serial I/O1 continues to output the final bit from the TXD pin after transmission is completed. The SOUT2 pin from serial I/O2 goes to high impedance after transmission is completed.

### A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that  $f(\text{XIN})$  is at least 500 kHz during an A-D conversion. (If the  $\overline{\text{ONW}}$  pin has been set to "L", the A-D conversion will take twice as long to match the longer bus cycle, and so  $f(\text{XIN})$  must be at least 1 MHz.)

Do not execute the STP or WIT instruction during an A-D conversion.

### D-A Converter

The accuracy of the D-A converter becomes poor rapidly under the  $V_{CC} = 3.0 \text{ V}$  or less condition.

### Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock  $\phi$  is half of the XIN frequency. When the  $\overline{\text{ONW}}$  function is used in modes other than single-chip mode, the frequency of the internal clock  $\phi$  may be one fourth the XIN frequency.

### Memory Expansion Mode

The memory expansion mode is not available in the following microcomputers.

- M38024M6-XXXSP
- M38024M6-XXXFP

### Memory Expansion Mode and Microprocessor Mode

Execute the LDM or STA instruction for writing to port P3 (address 000616) in memory expansion mode and microprocessor mode.

Set areas which can be read out and write to port P3 (address 000616) in a memory, using the read-modify-write instruction (SEB, CLB).

**DATA REQUIRED FOR MASK ORDERS**

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

**ROM PROGRAMMING METHOD**

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

| Package      | Name of Programming Adapter |
|--------------|-----------------------------|
| 64P4B, 64S1B | PCA4738S-64A                |
| 64P6N        | PCA4738F-64A                |
| 64D0         | PCA4738L-64A                |

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 35 is recommended to verify programming.

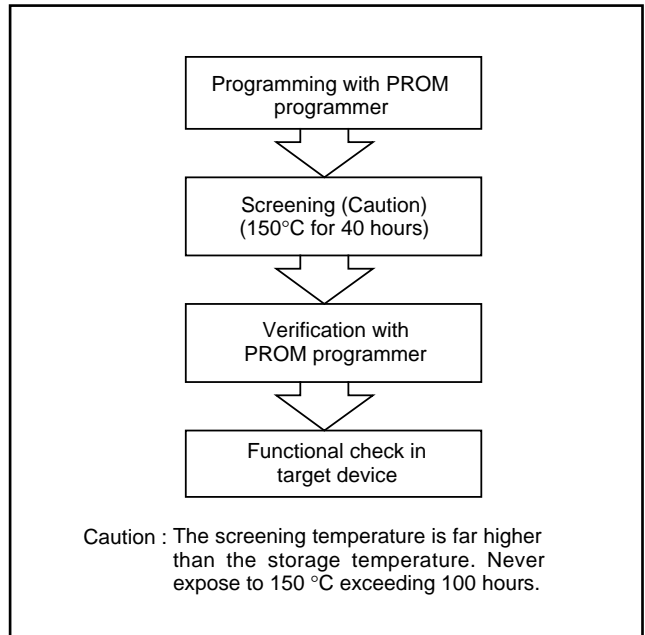


Fig. 35 Programming and testing of One Time PROM version

**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter  | Conditions   | Ratings          | Unit |
|--------|--|--|------------------|------|
| VCC    | Power source voltage   |  | -0.3 to 7.0      | V    |
| Vi     | Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, VREF  | All voltages are based on Vss. Output transistors are cut off. | -0.3 to Vcc +0.3 | V    |
| Vi     | Input voltage $\overline{\text{RESET}}$ , XIN                                      |  | -0.3 to Vcc +0.3 | V    |
| Vi     | Input voltage CNVss  |  | -0.3 to 13       | V    |
| Vo     | Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, XOUT |  | -0.3 to Vcc +0.3 | V    |
| Pd     | Power dissipation  | Ta = 25 °C   | 1000 (Note)      | mW   |
| Topr   | Operating temperature  |  | -20 to 85        | °C   |
| Tstg   | Storage temperature  |  | -40 to 125       | °C   |

**Note:** 300 mW in case of the flat package.

**RECOMMENDED OPERATING CONDITIONS** (Vcc = 3.0 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol             | Parameter   | Limits  |      |          | Unit |
|--------------------|---|---------|------|----------|------|
|                    |   | Min.    | Typ. | Max.     |      |
| VCC                | Power source voltage (f(XIN) < 2 MHz) (Note 1)  | 3.0     | 5.0  | 5.5      | V    |
|                    | Power source voltage (f(XIN) = 8 MHz) (Note 1)  | 4.0     | 5.0  | 5.5      |      |
| VSS                | Power source voltage  |         | 0    |          | V    |
| VREF               | Analog reference voltage (when A-D converter is used)   | 2.0     |      | Vcc      | V    |
|                    | Analog reference voltage (when D-A converter is used)   | 3.0     |      | Vcc      |      |
| AVSS               | Analog power source voltage   |         | 0    |          | V    |
| VIA                | Analog input voltage AN0-AN7  | AVSS    |      | Vcc      | V    |
| VIH                | "H" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67                   | 0.8 Vcc |      | Vcc      | V    |
| VIH                | "H" input voltage $\overline{\text{RESET}}$ , XIN, CNVss  | 0.8 Vcc |      | Vcc      | V    |
| VIL                | "L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67                   | 0       |      | 0.2 Vcc  | V    |
| VIL                | "L" input voltage $\overline{\text{RESET}}$ , CNVss   | 0       |      | 0.2 Vcc  | V    |
| VIL                | "L" input voltage XIN   | 0       |      | 0.16 Vcc | V    |
| $\Sigma$ IOH(peak) | "H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 2)                         |         |      | -80      | mA   |
| $\Sigma$ IOH(peak) | "H" total peak output current P40-P47, P50-P57, P60-P67 (Note 2)                                  |         |      | -80      |      |
| $\Sigma$ IOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 2)                         |         |      | 80       | mA   |
| $\Sigma$ IOL(peak) | "L" total peak output current P40-P47, P50-P57, P60-P67 (Note 2)                                  |         |      | 80       |      |
| $\Sigma$ IOH(avg)  | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 2)                      |         |      | -40      | mA   |
| $\Sigma$ IOH(avg)  | "H" total average output current P40-P47, P50-P57, P60-P67 (Note 2)                               |         |      | -40      |      |
| $\Sigma$ IOL(avg)  | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 2)                      |         |      | 40       | mA   |
| $\Sigma$ IOL(avg)  | "L" total average output current P40-P47, P50-P57, P60-P67 (Note 2)                               |         |      | 40       |      |
| IOH(peak)          | "H" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 3)    |         |      | -10      | mA   |
| IOL(peak)          | "L" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 3)    |         |      | 10       |      |
| IOH(avg)           | "H" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 4) |         |      | -5       | mA   |
| IOL(avg)           | "L" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 4) |         |      | 5        |      |
| f(XIN)             | Internal clock oscillation frequency (Vcc = 4.0 to 5.5 V)   |         |      | 8        | MHz  |
|                    | Internal clock oscillation frequency (Vcc = 3.0 to 4.0 V)   |         |      | 6 Vcc-16 |      |

**Note 1:** The minimum power source voltage is  $\frac{X+16}{6}$  [V] (f(XIN) = XMHz) on the condition of 2 MHz < f(XIN) < 8 MHz.

**2:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**3:** The peak output current is the peak current flowing in each port.

**4:** The average output current IOL(avg), IOH(avg) in an average value measured over 100 ms.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol    | Parameter  | Test conditions   | Limits                 |      |      | Unit |
|-----------|--|---|------------------------|------|------|------|
|           |  |   | Min.                   | Typ. | Max. |      |
| VOH       | “H” output voltage<br>P00–P07, P10–P17, P20–P27,<br>P30–P37, P40–P47, P50–P57,<br>P60–P67 (Note 1)     | IOH = –10 mA<br>VCC = 4.0 to 5.5 V  | VCC–2.0                |      |      | V    |
|           |  | IOH = –1.0 mA<br>VCC = 3.0 to 5.5 V   | VCC–1.0                |      |      |      |
| VOL       | “L” output voltage<br>P00–P07, P10–P17, P20–P27,<br>P30–P37, P40–P47, P50–P57,<br>P60–P67              | IOH = 10 mA<br>VCC = 4.0 to 5.5 V   |                        |      | 2.0  | V    |
|           |  | IOH = 1.0 mA<br>VCC = 3.0 to 5.5 V  |                        |      | 1.0  |      |
| VT+ – VT– | Hysteresis   | CNTR0, CNTR1, INT0–INT4   |                        | 0.4  |      | V    |
| VT+ – VT– | Hysteresis   | RxD, SCLK1, SIN2, SCLK2   |                        | 0.5  |      | V    |
| VT+ – VT– | Hysteresis   | RESET   |                        | 0.5  |      | V    |
| IiH       | “H” input current<br>P00–P07, P10–P17, P20–P27,<br>P30–P37, P40–P47, P50–P57,<br>P60–P67               | Vi = VCC  |                        |      | 5.0  | μA   |
| IiH       | “H” input current  | RESET, CNVss  | Vi = VCC               |      | 5.0  | μA   |
| IiH       | “H” input current  | XIN   | Vi = VCC               | 4    |      | μA   |
| IiL       | “L” input current<br>P00–P07, P10–P17, P20–P27,<br>P30–P37, P40–P47, P50–P57,<br>P60–P67, RESET, CNVss | Vi = VSS  |                        |      | –5.0 | μA   |
| IiL       | “L” input current  | RESET, CNVss  | Vi = VSS               |      | –5.0 | μA   |
| IiL       | “L” input current  | XIN   | Vi = VSS               | –4   |      | μA   |
| VRAM      | RAM hold voltage   | When clock stopped  | 2.0                    |      | 5.5  | V    |
| ICC       | Power source current   | f(XIN) = 8 MHz, VCC = 5 V   |                        | 6.4  | 13   | mA   |
|           |  | f(XIN) = 5 MHz, VCC = 5 V   |                        | 4    | 8    |      |
|           |  | f(XIN) = 2 MHz, VCC = 3 V   |                        | 0.8  | 2.0  |      |
|           |  | When WIT instruction is executed with<br>f(Xin) = 8MHz, VCC=5V                          |                        | 1.5  |      |      |
|           |  | When WIT instruction is executed with<br>f(Xin) = 5MHz, VCC=5V                          |                        | 1    |      |      |
|           |  | When WIT instruction is executed with<br>f(Xin) = 2MHz, VCC=3V                          |                        | 0.2  |      |      |
|           |  | When STP instruction is executed with clock<br>stopped, output<br>transistors isolated. | Ta = 25 °C<br>(Note 2) |      | 0.1  | 1    |
|           | Ta = 85 °C<br>(Note 2)   |   |                        | 10   |      |      |

**Note 1:** P45 is measured when the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.

P51 is measured when the P51/SOUT2 P-channel output disable bit of the serial I/O2 control register (bit 7 of address 001D16) is “0”.

**2:** With output transistors isolated and A-D converter having completed conversion, and not including current flowing through VREF pin.

**A–D CONVERTER CHARACTERISTICS**

( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = AV_{SS} = 0$  V,  $V_{REF} = 2.0$  V to  $V_{CC}$ ,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol  | Parameter  | Test conditions | Limits |      |      | Unit  |
|---------|--|-----------------|--------|------|------|-------|
|         |  |                 | Min.   | Typ. | Max. |       |
| —       | Resolution                                       |                 |        |      | 8    | Bits  |
| —       | Absolute accuracy (excluding quantization error) |                 |        | ±1   | ±2.5 | LSB   |
| tCONV   | Conversion time                                  |                 |        |      | 50   | tc(φ) |
| RLADDER | Ladder resistor                                  |                 |        | 35   |      | kΩ    |
| IVREF   | Reference power source input current (Note)      | VREF = 5.0 V    | 50     | 150  | 200  | μA    |
| Ii(AD)  | A-D port input current                           |                 |        | 0.5  | 5.0  | μA    |

**Note:** When D-A conversion registers (addresses 003616 and 003716) contain “0016”.

**D-A CONVERTER CHARACTERISTICS**

(VCC = 3.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 3.0 V to VCC, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter                                   | Test conditions    | Limits |      |      | Unit |
|--------|---|--------------------|--------|------|------|------|
|        |   |                    | Min.   | Typ. | Max. |      |
| —      | Resolution                                  |                    |        |      | 8    | Bits |
| —      | Absolute accuracy                           | VCC = 4.0 to 5.5 V |        |      | 1.0  | %    |
|        |   | VCC = 3.0 to 4.0 V |        |      | 2.5  |      |
| tsu    | Setting time                                |                    |        |      | 3    | μs   |
| RO     | Output resistor                             |                    | 1      | 2.5  | 4    | kΩ   |
| IVREF  | Reference power source input current (Note) |                    |        |      | 3.2  | mA   |

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

**TIMING REQUIREMENTS 1** ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol                           | Parameter   | Limits |      |      | Unit |
|----------------------------------|---|--------|------|------|------|
|                                  |   | Min.   | Typ. | Max. |      |
| $t_{w(\overline{\text{RESET}})}$ | Reset input "L" pulse width                                 | 2      |      |      | μs   |
| $t_{c(XIN)}$                     | External clock input cycle time                             | 125    |      |      | ns   |
| $t_{wH(XIN)}$                    | External clock input "H" pulse width                        | 50     |      |      | ns   |
| $t_{wL(XIN)}$                    | External clock input "L" pulse width                        | 50     |      |      | ns   |
| $t_{c(CNTR)}$                    | CNTR <sub>0</sub> , CNTR <sub>1</sub> input cycle time      | 200    |      |      | ns   |
| $t_{wH(CNTR)}$                   | CNTR <sub>0</sub> , CNTR <sub>1</sub> input "H" pulse width | 80     |      |      | ns   |
| $t_{wH(INT)}$                    | INT <sub>0</sub> to INT <sub>4</sub> input "H" pulse width  | 80     |      |      | ns   |
| $t_{wL(CNTR)}$                   | CNTR <sub>0</sub> , CNTR <sub>1</sub> input "L" pulse width | 80     |      |      | ns   |
| $t_{wL(INT)}$                    | INT <sub>0</sub> to INT <sub>4</sub> input "L" pulse width  | 80     |      |      | ns   |
| $t_{c(SCLK1)}$                   | Serial I/O1 clock input cycle time (Note)                   | 800    |      |      | ns   |
| $t_{c(SCLK2)}$                   | Serial I/O2 clock input cycle time                          | 1000   |      |      | ns   |
| $t_{wH(SCLK1)}$                  | Serial I/O1 clock input "H" pulse width (Note)              | 370    |      |      | ns   |
| $t_{wH(SCLK2)}$                  | Serial I/O2 clock input "H" pulse width                     | 400    |      |      | ns   |
| $t_{wL(SCLK1)}$                  | Serial I/O1 clock input "L" pulse width (Note)              | 370    |      |      | ns   |
| $t_{wL(SCLK2)}$                  | Serial I/O2 clock input "L" pulse width                     | 400    |      |      | ns   |
| $t_{su(RxD-SCLK1)}$              | Serial I/O1 input set up time                               | 220    |      |      | ns   |
| $t_{su(SIN2-SCLK2)}$             | Serial I/O2 input set up time                               | 200    |      |      | ns   |
| $t_{h(SCLK1-RxD)}$               | Serial I/O1 input hold time                                 | 100    |      |      | ns   |
| $t_{h(SCLK2-SIN2)}$              | Serial I/O2 input hold time                                 | 200    |      |      | ns   |

**Note:** When  $f(XIN) = 8$  MHz and bit 6 of address 001A16 is "1". Divide this value by four when  $f(XIN) = 8$  MHz and bit 6 of address 001A16 is "0".

**TIMING REQUIREMENTS 2** ( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol                           | Parameter   | Limits                  |      |      | Unit |
|----------------------------------|---|-------------------------|------|------|------|
|                                  |   | Min.                    | Typ. | Max. |      |
| $t_{w(\overline{\text{RESET}})}$ | Reset input "L" pulse width                                 | 2                       |      |      | μs   |
| $t_{c(XIN)}$                     | External clock input cycle time                             | 500/<br>(3 $V_{CC}-8$ ) |      |      | ns   |
| $t_{wH(XIN)}$                    | External clock input "H" pulse width                        | 200/<br>(3 $V_{CC}-8$ ) |      |      | ns   |
| $t_{wL(XIN)}$                    | External clock input "L" pulse width                        | 200/<br>(3 $V_{CC}-8$ ) |      |      | ns   |
| $t_{c(CNTR)}$                    | CNTR <sub>0</sub> , CNTR <sub>1</sub> input cycle time      | 500                     |      |      | ns   |
| $t_{wH(CNTR)}$                   | CNTR <sub>0</sub> , CNTR <sub>1</sub> input "H" pulse width | 230                     |      |      | ns   |
| $t_{wH(INT)}$                    | INT <sub>0</sub> to INT <sub>4</sub> input "H" pulse width  | 230                     |      |      | ns   |
| $t_{wL(CNTR)}$                   | CNTR <sub>0</sub> , CNTR <sub>1</sub> input "L" pulse width | 230                     |      |      | ns   |
| $t_{wL(INT)}$                    | INT <sub>0</sub> to INT <sub>4</sub> input "L" pulse width  | 230                     |      |      | ns   |
| $t_{c(SCLK1)}$                   | Serial I/O1 clock input cycle time (Note)                   | 2000                    |      |      | ns   |
| $t_{c(SCLK2)}$                   | Serial I/O2 clock input cycle time                          | 2000                    |      |      | ns   |
| $t_{wH(SCLK1)}$                  | Serial I/O1 clock input "H" pulse width (Note)              | 950                     |      |      | ns   |
| $t_{wH(SCLK2)}$                  | Serial I/O2 clock input "H" pulse width                     | 950                     |      |      | ns   |
| $t_{wL(SCLK1)}$                  | Serial I/O1 clock input "L" pulse width (Note)              | 950                     |      |      | ns   |
| $t_{wL(SCLK2)}$                  | Serial I/O2 clock input "L" pulse width                     | 950                     |      |      | ns   |
| $t_{su(RxD-SCLK1)}$              | Serial I/O1 input set up time                               | 400                     |      |      | ns   |
| $t_{su(SIN2-SCLK2)}$             | Serial I/O2 input set up time                               | 400                     |      |      | ns   |
| $t_{h(SCLK1-RxD)}$               | Serial I/O1 input hold time                                 | 200                     |      |      | ns   |
| $t_{h(SCLK2-SIN2)}$              | Serial I/O2 input hold time                                 | 300                     |      |      | ns   |

**Note:** When  $f(XIN) = 2$  MHz and bit 6 of address 001A16 is "1". Divide this value by four when  $f(XIN) = 2$  MHz and bit 6 of address 001A16 is "0".

**SWITCHING CHARACTERISTICS 1** ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol                | Parameter                                | Test conditions | Limits                |      |      | Unit |
|-----------------------|--|-----------------|-----------------------|------|------|------|
|                       |  |                 | Min.                  | Typ. | Max. |      |
| $t_{wH}(S_{CLK1})$    | Serial I/O1 clock output "H" pulse width | Fig. 36         | $t_c(S_{CLK1})/2-30$  |      |      | ns   |
| $t_{wH}(S_{CLK2})$    | Serial I/O2 clock output "H" pulse width |                 | $t_c(S_{CLK2})/2-160$ |      |      | ns   |
| $t_{wL}(S_{CLK1})$    | Serial I/O1 clock output "L" pulse width |                 | $t_c(S_{CLK1})/2-30$  |      |      | ns   |
| $t_{wL}(S_{CLK2})$    | Serial I/O2 clock output "L" pulse width |                 | $t_c(S_{CLK2})/2-160$ |      |      | ns   |
| $t_d(S_{CLK1}-TxD)$   | Serial I/O1 output delay time (Note 1)   |                 |                       |      | 140  | ns   |
| $t_d(S_{CLK2}-SOUT2)$ | Serial I/O2 output delay time (Note 2)   |                 |                       |      | 200  | ns   |
| $t_v(S_{CLK1}-TxD)$   | Serial I/O1 output valid time (Note 1)   |                 |                       | -30  |      | ns   |
| $t_v(S_{CLK2}-SOUT2)$ | Serial I/O2 output valid time (Note 2)   |                 |                       | 0    |      | ns   |
| $t_r(S_{CLK1})$       | Serial I/O1 clock output rising time     |                 |                       |      | 30   | ns   |
| $t_f(S_{CLK1})$       | Serial I/O1 clock output falling time    |                 |                       |      | 30   | ns   |
| $t_r(S_{CLK2})$       | Serial I/O2 clock output rising time     |                 |                       |      | 30   | ns   |
| $t_f(S_{CLK2})$       | Serial I/O2 clock output falling time    |                 |                       |      | 40   | ns   |
| $t_r(CMOS)$           | CMOS output rising time (Note 3)         |                 |                       |      | 10   | ns   |
| $t_f(CMOS)$           | CMOS output falling time (Note 3)        |                 |                       |      | 10   | ns   |

- Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
**2:** When the P51/SOUT2 P-channel output disable bit of the serial I/O2 control register (bit 7 of address 001D16) is "0".  
**3:** XOUT pin is excluded.

**SWITCHING CHARACTERISTICS 2** ( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

| Symbol                | Parameter                                | Test conditions | Limits                |      |      | Unit |
|-----------------------|--|-----------------|-----------------------|------|------|------|
|                       |  |                 | Min.                  | Typ. | Max. |      |
| $t_{wH}(S_{CLK1})$    | Serial I/O1 clock output "H" pulse width | Fig. 36         | $t_c(S_{CLK1})/2-50$  |      |      | ns   |
| $t_{wH}(S_{CLK2})$    | Serial I/O2 clock output "H" pulse width |                 | $t_c(S_{CLK2})/2-240$ |      |      | ns   |
| $t_{wL}(S_{CLK1})$    | Serial I/O1 clock output "L" pulse width |                 | $t_c(S_{CLK1})/2-50$  |      |      | ns   |
| $t_{wL}(S_{CLK2})$    | Serial I/O2 clock output "L" pulse width |                 | $t_c(S_{CLK2})/2-240$ |      |      | ns   |
| $t_d(S_{CLK1}-TxD)$   | Serial I/O1 output delay time (Note 1)   |                 |                       |      | 350  | ns   |
| $t_d(S_{CLK2}-SOUT2)$ | Serial I/O2 output delay time (Note 2)   |                 |                       |      | 400  | ns   |
| $t_v(S_{CLK1}-TxD)$   | Serial I/O1 output valid time (Note 1)   |                 |                       | -30  |      | ns   |
| $t_v(S_{CLK2}-SOUT2)$ | Serial I/O2 output valid time (Note 2)   |                 |                       | 0    |      | ns   |
| $t_r(S_{CLK1})$       | Serial I/O1 clock output rising time     |                 |                       |      | 50   | ns   |
| $t_f(S_{CLK1})$       | Serial I/O1 clock output falling time    |                 |                       |      | 50   | ns   |
| $t_r(S_{CLK2})$       | Serial I/O2 clock output rising time     |                 |                       |      | 50   | ns   |
| $t_f(S_{CLK2})$       | Serial I/O2 clock output falling time    |                 |                       |      | 50   | ns   |
| $t_r(CMOS)$           | CMOS output rising time (Note 3)         |                 |                       |      | 20   | ns   |
| $t_f(CMOS)$           | CMOS output falling time (Note 3)        |                 |                       |      | 20   | ns   |

- Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
**2:** When the P51/SOUT2 P-channel output disable bit of the serial I/O2 control register (bit 7 of address 001D16) is "0".  
**3:** XOUT pin is excluded.

**TIMING REQUIREMENTS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol                     | Parameter  | Limits |      |      | Unit |
|----------------------------|--|--------|------|------|------|
|                            |  | Min.   | Typ. | Max. |      |
| tsu(ONW-φ)                 | Before φ ONW input set up time                                     | -20    |      |      | ns   |
| th(φ-ONW)                  | After φ ONW input hold time  | -20    |      |      | ns   |
| tsu(DB-φ)                  | Before φ data bus set up time                                      | 60     |      |      | ns   |
| th(φ-DB)                   | After φ data bus hold time   | 0      |      |      | ns   |
| tsu(ONW-RD)<br>tsu(ONW-WR) | Before RD ONW input set up time<br>Before WR ONW input set up time | -20    |      |      | ns   |
| th(RD-ONW)<br>th(WR-ONW)   | After RD ONW input hold time<br>After WR ONW input hold time       | -20    |      |      | ns   |
| tsu(DB-RD)                 | Before RD data bus set up time                                     | 65     |      |      | ns   |
| th(RD-DB)                  | After RD data bus hold time  | 0      |      |      | ns   |

**SWITCHING CHARACTERISTICS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol                 | Parameter  | Test conditions | Limits                    |            |      | Unit     |
|------------------------|--|-----------------|---------------------------|------------|------|----------|
|                        |  |                 | Min.                      | Typ.       | Max. |          |
| tc(φ)                  | φ clock cycle time   | Fig. 36         |                           | 2tc(XIN)   |      | ns       |
| twH(φ)                 | φ clock "H" pulse width  |                 | tc(XIN)-10                |            |      | ns       |
| twL(φ)                 | φ clock "L" pulse width  |                 | tc(XIN)-10                |            |      | ns       |
| td(φ-AH)               | After φ AD15-AD8 delay time  |                 |                           | 20         | 40   | ns       |
| tv(φ-AH)               | After φ AD15-AD8 valid time  |                 | 6                         | 10         |      | ns       |
| td(φ-AL)               | After φ AD7-AD0 delay time   |                 |                           | 25         | 45   | ns       |
| tv(φ-AL)               | After φ AD7-AD0 valid time   |                 | 6                         | 10         |      | ns       |
| td(φ-SYNC)             | SYNC delay time  |                 |                           | 20         |      | ns       |
| tv(φ-SYNC)             | SYNC valid time  |                 |                           | 10         |      | ns       |
| td(φ-WR)               | RD and WR delay time   |                 |                           | 10         | 20   | ns       |
| tv(φ-WR)               | RD and WR valid time   |                 | 3                         | 5          | 10   | ns       |
| td(φ-DB)               | After φ data bus delay time  |                 |                           | 20         | 70   | ns       |
| tv(φ-DB)               | After φ data bus valid time  |                 | 15                        |            |      | ns       |
| twL(RD)<br>twL(WR)     | RD pulse width, WR pulse width<br>RD pulse width, WR pulse width<br>(When one-wait is valid) |                 | tc(XIN)-10<br>3tc(XIN)-10 |            |      | ns<br>ns |
| td(AH-RD)<br>td(AH-WR) | After AD15-AD8 RD delay time<br>After AD15-AD8 WR delay time                                 |                 | tc(XIN)-35                | tc(XIN)-15 |      | ns       |
| td(AL-RD)<br>td(AL-WR) | After AD7-AD0 RD delay time<br>After AD7-AD0 WR delay time                                   |                 | tc(XIN)-40                | tc(XIN)-20 |      | ns       |
| tv(RD-AH)<br>tv(WR-AH) | After RD AD15-AD8 valid time<br>After WR AD15-AD8 valid time                                 |                 | 0                         | 5          |      | ns       |
| tv(RD-AL)<br>tv(WR-AL) | After RD AD7-AD0 valid time<br>After WR AD7-AD0 valid time                                   |                 | 0                         | 5          |      | ns       |
| td(WR-DB)              | After WR data bus delay time   |                 |                           | 15         | 65   | ns       |
| tv(WR-DB)              | After WR data bus valid time   |                 | 10                        |            |      | ns       |
| td(RESET-RESETOut)     | RESETOut output delay time (Note 1)  |                 |                           |            | 200  | ns       |
| tv(φ-RESET)            | RESETOut output valid time (Note 1)  |                 | 0                         |            | 200  | ns       |

**Note 1:** The RESETOut output goes "H" in sync with the rise of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".



**TIMING REQUIREMENTS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(V<sub>CC</sub> = 3.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

| Symbol  | Parameter   | Limits |      |      | Unit |
|---|---|--------|------|------|------|
|   |   | Min.   | Typ. | Max. |      |
| tsu( $\overline{\text{ONW}}-\phi$ )                 | Before $\phi$ $\overline{\text{ONW}}$ input set up time                 | -20    |      |      | ns   |
| th( $\phi-\overline{\text{ONW}}$ )                  | After $\phi$ $\overline{\text{ONW}}$ input hold time                    | -20    |      |      | ns   |
| tsu(DB- $\phi$ )                                    | Before $\phi$ data bus set up time                                      | 180    |      |      | ns   |
| th( $\phi$ -DB)                                     | After $\phi$ data bus hold time   | 0      |      |      | ns   |
| tsu( $\overline{\text{ONW}}-\overline{\text{RD}}$ ) | Before $\overline{\text{RD}}$ $\overline{\text{ONW}}$ input set up time | -20    |      |      | ns   |
| tsu( $\overline{\text{ONW}}-\overline{\text{WR}}$ ) | Before $\overline{\text{WR}}$ $\overline{\text{ONW}}$ input set up time | -20    |      |      | ns   |
| th( $\overline{\text{RD}}-\overline{\text{ONW}}$ )  | After $\overline{\text{RD}}$ $\overline{\text{ONW}}$ input hold time    | -20    |      |      | ns   |
| th( $\overline{\text{WR}}-\overline{\text{ONW}}$ )  | After $\overline{\text{WR}}$ $\overline{\text{ONW}}$ input hold time    | -20    |      |      | ns   |
| tsu(DB- $\overline{\text{RD}}$ )                    | Before $\overline{\text{RD}}$ data bus set up time                      | 185    |      |      | ns   |
| th( $\overline{\text{RD}}$ -DB)                     | After $\overline{\text{RD}}$ data bus hold time                         | 0      |      |      | ns   |

**SWITCHING CHARACTERISTICS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(V<sub>CC</sub> = 3.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

| Symbol                                | Parameter   | Test conditions | Limits                  |                          |      | Unit |
|---------------------------------------|---|-----------------|-------------------------|--------------------------|------|------|
|                                       |   |                 | Min.                    | Typ.                     | Max. |      |
| tc( $\phi$ )                          | $\phi$ clock cycle time   | Fig. 36         |                         | 2tc(X <sub>IN</sub> )    |      | ns   |
| twH( $\phi$ )                         | $\phi$ clock "H" pulse width  |                 | tc(X <sub>IN</sub> )-20 |                          |      | ns   |
| twL( $\phi$ )                         | $\phi$ clock "L" pulse width  |                 | tc(X <sub>IN</sub> )-20 |                          |      | ns   |
| td( $\phi$ -AH)                       | After $\phi$ AD <sub>15</sub> -AD <sub>8</sub> delay time                                       |                 |                         |                          | 150  | ns   |
| tv( $\phi$ -AH)                       | After $\phi$ AD <sub>15</sub> -AD <sub>8</sub> valid time                                       |                 |                         | 10                       | 15   | ns   |
| td( $\phi$ -AL)                       | After $\phi$ AD <sub>7</sub> -AD <sub>0</sub> delay time  |                 |                         |                          | 150  | ns   |
| tv( $\phi$ -AL)                       | After $\phi$ AD <sub>7</sub> -AD <sub>0</sub> valid time  |                 |                         | 10                       | 15   | ns   |
| td( $\phi$ -SYNC)                     | SYNC delay time   |                 |                         |                          | 40   | ns   |
| tv( $\phi$ -SYNC)                     | SYNC valid time   |                 |                         |                          | 20   | ns   |
| td( $\phi$ - $\overline{\text{WR}}$ ) | $\overline{\text{RD}}$ and $\overline{\text{WR}}$ delay time                                    |                 |                         |                          | 15   | ns   |
| tv( $\phi$ - $\overline{\text{WR}}$ ) | $\overline{\text{RD}}$ and $\overline{\text{WR}}$ valid time                                    |                 |                         | 3                        | 7    | ns   |
| td( $\phi$ -DB)                       | After $\phi$ data bus delay time  |                 |                         |                          | 200  | ns   |
| tv( $\phi$ -DB)                       | After $\phi$ data bus valid time  |                 |                         | 15                       |      | ns   |
| twL( $\overline{\text{RD}}$ )         | $\overline{\text{RD}}$ pulse width, $\overline{\text{WR}}$ pulse width                          |                 |                         | tc(X <sub>IN</sub> )-20  |      | ns   |
| twL( $\overline{\text{WR}}$ )         | $\overline{\text{RD}}$ pulse width, $\overline{\text{WR}}$ pulse width (when one-wait is valid) |                 |                         | 3tc(X <sub>IN</sub> )-20 |      | ns   |
| td(AH- $\overline{\text{RD}}$ )       | After AD <sub>15</sub> -AD <sub>8</sub> $\overline{\text{RD}}$ delay time                       |                 |                         | tc(X <sub>IN</sub> )-145 |      | ns   |
| td(AH- $\overline{\text{WR}}$ )       | After AD <sub>15</sub> -AD <sub>8</sub> $\overline{\text{WR}}$ delay time                       |                 |                         | tc(X <sub>IN</sub> )-145 |      | ns   |
| td(AL- $\overline{\text{RD}}$ )       | After AD <sub>7</sub> -AD <sub>0</sub> $\overline{\text{RD}}$ delay time                        |                 |                         | tc(X <sub>IN</sub> )-145 |      | ns   |
| td(AL- $\overline{\text{WR}}$ )       | After AD <sub>7</sub> -AD <sub>0</sub> $\overline{\text{WR}}$ delay time                        |                 |                         | tc(X <sub>IN</sub> )-145 |      | ns   |
| tv( $\overline{\text{RD}}$ -AH)       | After $\overline{\text{RD}}$ AD <sub>15</sub> -AD <sub>8</sub> valid time                       |                 |                         | 5                        | 10   | ns   |
| tv( $\overline{\text{WR}}$ -AH)       | After $\overline{\text{WR}}$ AD <sub>15</sub> -AD <sub>8</sub> valid time                       |                 |                         | 5                        | 10   | ns   |
| tv( $\overline{\text{RD}}$ -AL)       | After $\overline{\text{RD}}$ AD <sub>7</sub> -AD <sub>0</sub> valid time                        |                 |                         | 5                        | 10   | ns   |
| tv( $\overline{\text{WR}}$ -AL)       | After $\overline{\text{WR}}$ AD <sub>7</sub> -AD <sub>0</sub> valid time                        |                 |                         | 5                        | 10   | ns   |
| td( $\overline{\text{WR}}$ -DB)       | After $\overline{\text{WR}}$ data bus delay time  |                 |                         |                          | 195  | ns   |
| tv( $\overline{\text{WR}}$ -DB)       | After $\overline{\text{WR}}$ data bus valid time  |                 |                         | 10                       |      | ns   |
| td(RESET-RESETO <sub>UT</sub> )       | RESETO <sub>UT</sub> output delay time (Note 1)   |                 |                         |                          | 300  | ns   |
| tv( $\phi$ -RESET)                    | RESETO <sub>UT</sub> output valid time (Note 1)   |                 |                         | 0                        | 300  | ns   |

**Note1:** The RESETO<sub>UT</sub> output goes "H" in sync with the fall of the  $\phi$  clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".

**ABSOLUTE MAXIMUM RATINGS (Extended operating temperature version)**

| Symbol | Parameter  | Conditions  | Ratings          | Unit |
|--------|--|---|------------------|------|
| VCC    | Power source voltage   |   | -0.3 to 7.0      | V    |
| VI     | Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, VREF  | All voltage are based on Vss. Output transistors are cut off. | -0.3 to Vcc +0.3 | V    |
| VI     | Input voltage RESET, XIN   |   | -0.3 to Vcc +0.3 | V    |
| VI     | Input voltage CNVss  |   | -0.3 to 13       | V    |
| VO     | Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, XOUT |   | -0.3 to Vcc +0.3 | V    |
| Pd     | Power dissipation  | Ta = 25 °C  | 1000 (Note)      | mW   |
| Topr   | Operating temperature  |   | -40 to 85        | °C   |
| Tstg   | Storage temperature  |   | -65 to 150       | °C   |

**RECOMMENDED OPERATING CONDITIONS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, Ta = -40 to 85 °C, unless otherwise noted)

| Symbol     | Parameter   | Limits  |      |          | Unit |
|------------|---|---------|------|----------|------|
|            |   | Min.    | Typ. | Max.     |      |
| VCC        | Power source voltage (f(XIN) ≤ 2 MHz)   | 4.0     | 5.0  | 5.5      | V    |
| VSS        | Power source voltage  |         | 0    |          | V    |
| VREF       | Analog reference voltage (when A-D converter is used)   | 2.0     |      | VCC      | V    |
|            | Analog reference voltage (when D-A converter is used)   | 4.0     |      | VCC      | V    |
| AVSS       | Analog power source voltage   |         | 0    |          | V    |
| VIA        | Analog input voltage AN0-AN7  | AVSS    |      | VCC      | V    |
| VIH        | "H" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67                   | 0.8 VCC |      | VCC      | V    |
| VIH        | "H" input voltage RESET, XIN, CNVss   | 0.8 VCC |      | VCC      | V    |
| VIL        | "L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67                   | 0       |      | 0.2 VCC  | V    |
| VIL        | "L" input voltage RESET, CNVss  | 0       |      | 0.2 VCC  | V    |
| VIL        | "L" input voltage XIN   | 0       |      | 0.16 VCC | V    |
| ΣIOH(peak) | "H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)                         |         |      | -80      | mA   |
| ΣIOH(peak) | "H" total peak output current P40-P47, P50-P57, P60-P67 (Note 1)                                  |         |      | -80      | mA   |
| ΣIOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)                         |         |      | 80       | mA   |
| ΣIOL(peak) | "L" total peak output current P40-P47, P50-P57, P60-P67 (Note 1)                                  |         |      | 80       | mA   |
| ΣIOH(avg)  | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)                      |         |      | -40      | mA   |
| ΣIOH(avg)  | "H" total average output current P40-P47, P50-P57, P60-P67 (Note 1)                               |         |      | -40      | mA   |
| ΣIOL(avg)  | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)                      |         |      | 40       | mA   |
| ΣIOL(avg)  | "L" total average output current P40-P47, P50-P57, P60-P67 (Note 1)                               |         |      | 40       | mA   |
| IOH(peak)  | "H" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 2)    |         |      | -10      | mA   |
| IOL(peak)  | "L" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 2)    |         |      | 10       | mA   |
| IOH(avg)   | "H" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 3) |         |      | -5       | mA   |
| IOL(avg)   | "L" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67 (Note 3) |         |      | 5        | mA   |
| f(XIN)     | Internal clock oscillation frequency (VCC = 4.0 to 5.5 V)   |         |      | 8        | MHz  |

**Note 1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**2:** The peak output current is the peak current flowing in each port.

**3:** The average output current IOL(avg), IOH(avg) in an average value measured over 100 ms.

**ELECTRICAL CHARACTERISTICS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

| Symbol    | Parameter  | Test conditions  | Limits   |      |      | Unit |
|-----------|--|--|--|------|------|------|
|           |  |  | Min.   | Typ. | Max. |      |
| VOH       | "H" output voltage<br>P00-P07, P10-P17, P20-P27,<br>P30-P37, P40-P47, P50-P57,<br>P60-P67 (Note 1)     | IOH = -10 mA   | VCC-2.0  |      |      | V    |
| VOL       | "L" output voltage<br>P00-P07, P10-P17, P20-P27,<br>P30-P37, P40-P47, P50-P57,<br>P60-P67              | IOL = 10 mA  |  |      | 2.0  | V    |
| VT+ - VT- | Hysteresis<br>CNTR0, CNTR1, INT0-INT4  |  |  | 0.4  |      | V    |
| VT+ - VT- | Hysteresis<br>RXD, SCLK1, SIN2, SCLK2  |  |  | 0.5  |      | V    |
| VT+ - VT- | Hysteresis<br>RESET  |  |  | 0.5  |      | V    |
| IiH       | "H" input current<br>P00-P07, P10-P17, P20-P27,<br>P30-P37, P40-P47, P50-P57,<br>P60-P67               | Vi = VCC   |  |      | 5.0  | μA   |
| IiH       | "H" input current<br>RESET, CNVss  | Vi = VCC   |  |      | 5.0  | μA   |
| IiH       | "H" input current<br>XIN   | Vi = VCC   |  | 4    |      | μA   |
| IiL       | "L" input current<br>P00-P07, P10-P17, P20-P27,<br>P30-P37, P40-P47, P50-P57,<br>P60-P67, RESET, CNVss | Vi = VSS   |  |      | -5.0 | μA   |
| IiL       | "L" input current<br>XIN   | Vi = VSS   |  | -4   |      | μA   |
| VRAM      | RAM hold voltage   | When clock stopped   | 2.0  |      | 5.5  | V    |
| ICC       | Power source current   | f(XIN) = 8 MHz   |  | 6.4  | 13   | mA   |
|           |  | f(XIN) = 5 MHz   |  | 4    | 8    |      |
|           |  | When WIT instruction is executed<br>with f(XIN) = 8 MHz                                    |  | 1.5  |      |      |
|           |  | When WIT instruction is executed<br>with f(XIN) = 5 MHz                                    |  | 1    |      |      |
|           |  | When STP instruction<br>is executed with clock<br>stopped, output<br>transistors isolated. | Ta = 25 °C<br>(Note 2)<br>Ta = 85 °C<br>(Note 2) |      | 0.1  | 1    |

**Note 1:** P45 is measured when the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

P51 is measured when the P51/SOUT2 P-channel output disable bit of the serial I/O2 control register (bit 7 of address 001D16) is "0".

**2:** With output transistors isolated and A-D converter having completed conversion, and not including current flowing through VREF pin.

**A-D CONVERTER CHARACTERISTICS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 2.0 V to VCC, Ta = -40 to 85 °C, unless otherwise noted)

| Symbol  | Parameter  | Test conditions | Limits |      |      | Unit  |
|---------|--|-----------------|--------|------|------|-------|
|         |  |                 | Min.   | Typ. | Max. |       |
| —       | Resolution                                       |                 |        |      | 8    | Bits  |
| —       | Absolute accuracy (excluding quantization error) |                 |        | ±1   | ±2.5 | LSB   |
| tCONV   | Conversion time                                  |                 |        |      | 50   | tC(φ) |
| RLADDER | Ladder resistor                                  |                 |        | 35   |      | kΩ    |
| IvREF   | Reference power source input current (Note)      | VREF = 5.0 V    | 50     | 150  | 200  | μA    |
| Ii(AD)  | A-D port input current                           |                 |        | 0.5  | 5.0  | μA    |

**Note:** When D-A conversion registers (addresses 003616 and 003716) contain "0016".

**D-A CONVERTER CHARACTERISTICS (Extended operating temperature version)**(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, V<sub>REF</sub> = 4.0 V to V<sub>CC</sub>, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

| Symbol            | Parameter                                   | Test conditions | Limits |      |      | Unit |
|-------------------|---|-----------------|--------|------|------|------|
|                   |   |                 | Min.   | Typ. | Max. |      |
| —                 | Resolution                                  |                 |        |      | 8    | Bits |
| —                 | Absolute accuracy                           |                 |        |      | 1.0  | %    |
| t <sub>su</sub>   | Setting time                                |                 |        |      | 3    | μs   |
| R <sub>O</sub>    | Output resistor                             |                 | 1      | 2.5  | 4    | kΩ   |
| I <sub>VREF</sub> | Reference power source input current (Note) |                 |        |      | 3.2  | mA   |

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

**TIMING REQUIREMENTS 1 (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

| Symbol                                       | Parameter                                      | Limits |      |      | Unit |
|--|--|--------|------|------|------|
|  |  | Min.   | Typ. | Max. |      |
| t <sub>w</sub> ( $\overline{\text{RESET}}$ ) | Reset input "L" pulse width                    | 2      |      |      | μs   |
| t <sub>c</sub> (X <sub>IN</sub> )            | External clock input cycle time                | 125    |      |      | ns   |
| t <sub>wH</sub> (X <sub>IN</sub> )           | External clock input "H" pulse width           | 50     |      |      | ns   |
| t <sub>wL</sub> (X <sub>IN</sub> )           | External clock input "L" pulse width           | 50     |      |      | ns   |
| t <sub>c</sub> (CNTR)                        | CNTR0, CNTR1 input cycle time                  | 200    |      |      | ns   |
| t <sub>wH</sub> (CNTR)                       | CNTR0, CNTR1 input "H" pulse width             | 80     |      |      | ns   |
| t <sub>wH</sub> (INT)                        | INT0 to INT4 input "H" pulse width             | 80     |      |      | ns   |
| t <sub>wL</sub> (CNTR)                       | CNTR0, CNTR1 input "L" pulse width             | 80     |      |      | ns   |
| t <sub>wL</sub> (INT)                        | INT0 to INT4 input "L" pulse width             | 80     |      |      | ns   |
| t <sub>c</sub> (SCLK1)                       | Serial I/O1 clock input cycle time (Note)      | 800    |      |      | ns   |
| t <sub>c</sub> (SCLK2)                       | Serial I/O2 clock input cycle time             | 1000   |      |      | ns   |
| t <sub>wH</sub> (SCLK1)                      | Serial I/O1 clock input "H" pulse width (Note) | 370    |      |      | ns   |
| t <sub>wH</sub> (SCLK2)                      | Serial I/O2 clock input "H" pulse width        | 400    |      |      | ns   |
| t <sub>wL</sub> (SCLK1)                      | Serial I/O1 clock input "L" pulse width (Note) | 370    |      |      | ns   |
| t <sub>wL</sub> (SCLK2)                      | Serial I/O2 clock input "L" pulse width        | 400    |      |      | ns   |
| t <sub>su</sub> (RxD-SCLK1)                  | Serial I/O1 input set up time                  | 220    |      |      | ns   |
| t <sub>su</sub> (SIN2-SCLK2)                 | Serial I/O2 input set up time                  | 200    |      |      | ns   |
| t <sub>h</sub> (SCLK1-RxD)                   | Serial I/O1 input hold time                    | 100    |      |      | ns   |
| t <sub>h</sub> (SCLK2-SIN2)                  | Serial I/O2 input hold time                    | 200    |      |      | ns   |

**Note:** When f(X<sub>IN</sub>) = 8 MHz and bit 6 of address 001A16 is "1". Divide this value by four when f(X<sub>IN</sub>) = 8 MHz and bit 6 of address 001A16 is "0".

**SWITCHING CHARACTERISTICS 1 (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

| Symbol                       | Parameter                                | Test conditions | Limits                       |      |      | Unit |    |
|------------------------------|--|-----------------|------------------------------|------|------|------|----|
|                              |  |                 | Min.                         | Typ. | Max. |      |    |
| t <sub>wH</sub> (SCLK1)      | Serial I/O1 clock output "H" pulse width | Fig. 36         | t <sub>c</sub> (SCLK1)/2-30  |      |      | ns   |    |
| t <sub>wH</sub> (SCLK2)      | Serial I/O2 clock output "H" pulse width |                 | t <sub>c</sub> (SCLK2)/2-160 |      |      | ns   |    |
| t <sub>wL</sub> (SCLK1)      | Serial I/O1 clock output "L" pulse width |                 | t <sub>c</sub> (SCLK1)/2-30  |      |      | ns   |    |
| t <sub>wL</sub> (SCLK2)      | Serial I/O2 clock output "L" pulse width |                 | t <sub>c</sub> (SCLK2)/2-160 |      |      | ns   |    |
| t <sub>d</sub> (SCLK1-TxD)   | Serial I/O1 output delay time (Note 1)   |                 |                              |      | 140  | ns   |    |
| t <sub>d</sub> (SCLK2-SOUT2) | Serial I/O2 output delay time (Note 2)   |                 |                              |      | 200  | ns   |    |
| t <sub>v</sub> (SCLK1-TxD)   | Serial I/O1 output valid time (Note 1)   |                 |                              | -30  |      | ns   |    |
| t <sub>v</sub> (SCLK2-SOUT2) | Serial I/O2 output valid time (Note 2)   |                 |                              | 0    |      | ns   |    |
| t <sub>r</sub> (SCLK1)       | Serial I/O1 clock output rising time     |                 |                              |      | 30   | ns   |    |
| t <sub>f</sub> (SCLK1)       | Serial I/O1 clock output falling time    |                 |                              |      | 30   | ns   |    |
| t <sub>r</sub> (SCLK2)       | Serial I/O2 clock output rising time     |                 |                              |      | 30   | ns   |    |
| t <sub>f</sub> (SCLK2)       | Serial I/O2 clock output falling time    |                 |                              |      | 40   | ns   |    |
| t <sub>r</sub> (CMOS)        | CMOS output rising time (Note 3)         |                 |                              |      | 10   | 30   | ns |
| t <sub>f</sub> (CMOS)        | CMOS output falling time (Note 3)        |                 |                              |      | 10   | 30   | ns |

**Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** When the P51/SOUT2 P-channel output disable bit of the serial I/O2 control register (bit 7 of address 001D16) is "0".

**3:** XOUT pin excluded.

**TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

**(Extended operating temperature version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

| Symbol   | Parameter   | Limits |      |      | Unit |
|--|---|--------|------|------|------|
|  |   | Min.   | Typ. | Max. |      |
| t <sub>su</sub> ( $\overline{\text{ONW}}-\phi$ )                 | Before $\phi$ $\overline{\text{ONW}}$ input set up time                 | -20    |      |      | ns   |
| t <sub>h</sub> ( $\phi-\overline{\text{ONW}}$ )                  | After $\phi$ $\overline{\text{ONW}}$ input hold time                    | -20    |      |      | ns   |
| t <sub>su</sub> (DB- $\phi$ )                                    | Before $\phi$ data bus set up time                                      | 60     |      |      | ns   |
| t <sub>h</sub> ( $\phi$ -DB)                                     | After $\phi$ data bus hold time   | 0      |      |      | ns   |
| t <sub>su</sub> ( $\overline{\text{ONW}}-\overline{\text{RD}}$ ) | Before $\overline{\text{RD}}$ $\overline{\text{ONW}}$ input set up time | -20    |      |      | ns   |
| t <sub>su</sub> ( $\overline{\text{ONW}}-\overline{\text{WR}}$ ) | Before $\overline{\text{WR}}$ $\overline{\text{ONW}}$ input set up time | -20    |      |      | ns   |
| t <sub>h</sub> ( $\overline{\text{RD}}-\overline{\text{ONW}}$ )  | After $\overline{\text{RD}}$ $\overline{\text{ONW}}$ input hold time    | -20    |      |      | ns   |
| t <sub>h</sub> ( $\overline{\text{WR}}-\overline{\text{ONW}}$ )  | After $\overline{\text{WR}}$ $\overline{\text{ONW}}$ input hold time    | -20    |      |      | ns   |
| t <sub>su</sub> (DB- $\overline{\text{RD}}$ )                    | Before $\overline{\text{RD}}$ data bus set up time                      | 65     |      |      | ns   |
| t <sub>h</sub> ( $\overline{\text{RD}}$ -DB)                     | After $\overline{\text{RD}}$ data bus hold time                         | 0      |      |      | ns   |

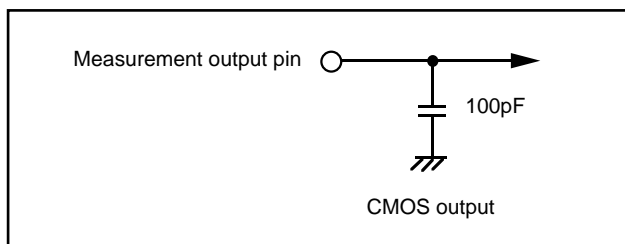
**SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

**(Extended operating temperature version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

| Symbol  | Parameter   | Test conditions | Limits                                |                                      |      | Unit |
|---|---|-----------------|---------------------------------------|--------------------------------------|------|------|
|   |   |                 | Min.                                  | Typ.                                 | Max. |      |
| t <sub>c</sub> ( $\phi$ )   | $\phi$ clock cycle time   | Fig. 36         |                                       | 2Xt <sub>c</sub> (X <sub>IN</sub> )  |      | ns   |
| t <sub>wH</sub> ( $\phi$ )  | $\phi$ clock "H" pulse width  |                 | t <sub>c</sub> (X <sub>IN</sub> )-10  |                                      |      | ns   |
| t <sub>wL</sub> ( $\phi$ )  | $\phi$ clock "L" pulse width  |                 | t <sub>c</sub> (X <sub>IN</sub> )-10  |                                      |      | ns   |
| t <sub>d</sub> ( $\phi$ -AH)  | After $\phi$ AD15-AD8 delay time  |                 |                                       | 20                                   | 40   | ns   |
| t <sub>v</sub> ( $\phi$ -AH)  | After $\phi$ AD15-AD8 valid time  |                 |                                       | 6                                    | 10   | ns   |
| t <sub>d</sub> ( $\phi$ -AL)  | After $\phi$ AD7-AD0 delay time   |                 |                                       | 25                                   | 45   | ns   |
| t <sub>v</sub> ( $\phi$ -AL)  | After $\phi$ AD7-AD0 valid time   |                 |                                       | 6                                    | 10   | ns   |
| t <sub>d</sub> ( $\phi$ -SYNC)  | SYNC delay time   |                 |                                       | 20                                   |      | ns   |
| t <sub>v</sub> ( $\phi$ -SYNC)  | SYNC valid time   |                 |                                       | 10                                   |      | ns   |
| t <sub>d</sub> ( $\phi$ - $\overline{\text{WR}}$ )                          | $\overline{\text{RD}}$ and $\overline{\text{WR}}$ delay time                                    |                 |                                       | 10                                   | 20   | ns   |
| t <sub>v</sub> ( $\phi$ - $\overline{\text{WR}}$ )                          | $\overline{\text{RD}}$ and $\overline{\text{WR}}$ valid time                                    |                 |                                       | 3                                    | 5    | ns   |
| t <sub>d</sub> ( $\phi$ -DB)  | After $\phi$ data bus delay time  |                 |                                       | 20                                   | 70   | ns   |
| t <sub>v</sub> ( $\phi$ -DB)  | After $\phi$ data bus valid time  |                 |                                       | 15                                   |      | ns   |
| t <sub>wL</sub> ( $\overline{\text{RD}}$ )                                  | $\overline{\text{RD}}$ pulse width, $\overline{\text{WR}}$ pulse width                          |                 | t <sub>c</sub> (X <sub>IN</sub> )-10  |                                      |      | ns   |
| t <sub>wL</sub> ( $\overline{\text{WR}}$ )                                  | $\overline{\text{RD}}$ pulse width, $\overline{\text{WR}}$ pulse width (when one wait is valid) |                 | 3t <sub>c</sub> (X <sub>IN</sub> )-10 |                                      |      | ns   |
| t <sub>d</sub> (AH- $\overline{\text{RD}}$ )                                | After AD15-AD8 $\overline{\text{RD}}$ delay time  |                 | t <sub>c</sub> (X <sub>IN</sub> )-35  | t <sub>c</sub> (X <sub>IN</sub> )-15 |      | ns   |
| t <sub>d</sub> (AH- $\overline{\text{WR}}$ )                                | After AD15-AD8 $\overline{\text{WR}}$ delay time  |                 |                                       |                                      |      | ns   |
| t <sub>d</sub> (AL- $\overline{\text{RD}}$ )                                | After AD7-AD0 $\overline{\text{RD}}$ delay time   |                 | t <sub>c</sub> (X <sub>IN</sub> )-40  | t <sub>c</sub> (X <sub>IN</sub> )-20 |      | ns   |
| t <sub>d</sub> (AL- $\overline{\text{WR}}$ )                                | After AD7-AD0 $\overline{\text{WR}}$ delay time   |                 |                                       |                                      |      | ns   |
| t <sub>v</sub> ( $\overline{\text{RD}}$ -AH)                                | After $\overline{\text{RD}}$ AD15-AD8 valid time  |                 |                                       | 0                                    | 5    | ns   |
| t <sub>v</sub> ( $\overline{\text{WR}}$ -AH)                                | After $\overline{\text{WR}}$ AD15-AD8 valid time  |                 |                                       |                                      |      | ns   |
| t <sub>v</sub> ( $\overline{\text{RD}}$ -AL)                                | After $\overline{\text{RD}}$ AD7-AD0 valid time   |                 |                                       | 0                                    | 5    | ns   |
| t <sub>v</sub> ( $\overline{\text{WR}}$ -AL)                                | After $\overline{\text{WR}}$ AD7-AD0 valid time   |                 |                                       |                                      |      | ns   |
| t <sub>d</sub> ( $\overline{\text{WR}}$ -DB)                                | After $\overline{\text{WR}}$ data bus delay time  |                 |                                       | 15                                   | 65   | ns   |
| t <sub>v</sub> ( $\overline{\text{WR}}$ -DB)                                | After $\overline{\text{WR}}$ data bus valid time  |                 |                                       | 10                                   |      | ns   |
| t <sub>d</sub> ( $\overline{\text{RESET}}$ - $\overline{\text{RESETOUT}}$ ) | $\overline{\text{RESETOUT}}$ output delay time  |                 |                                       |                                      | 200  | ns   |
| t <sub>v</sub> ( $\phi$ - $\overline{\text{RESET}}$ )                       | $\overline{\text{RESETOUT}}$ output valid time (Note 1)   |                 | 0                                     | 200                                  | ns   |      |

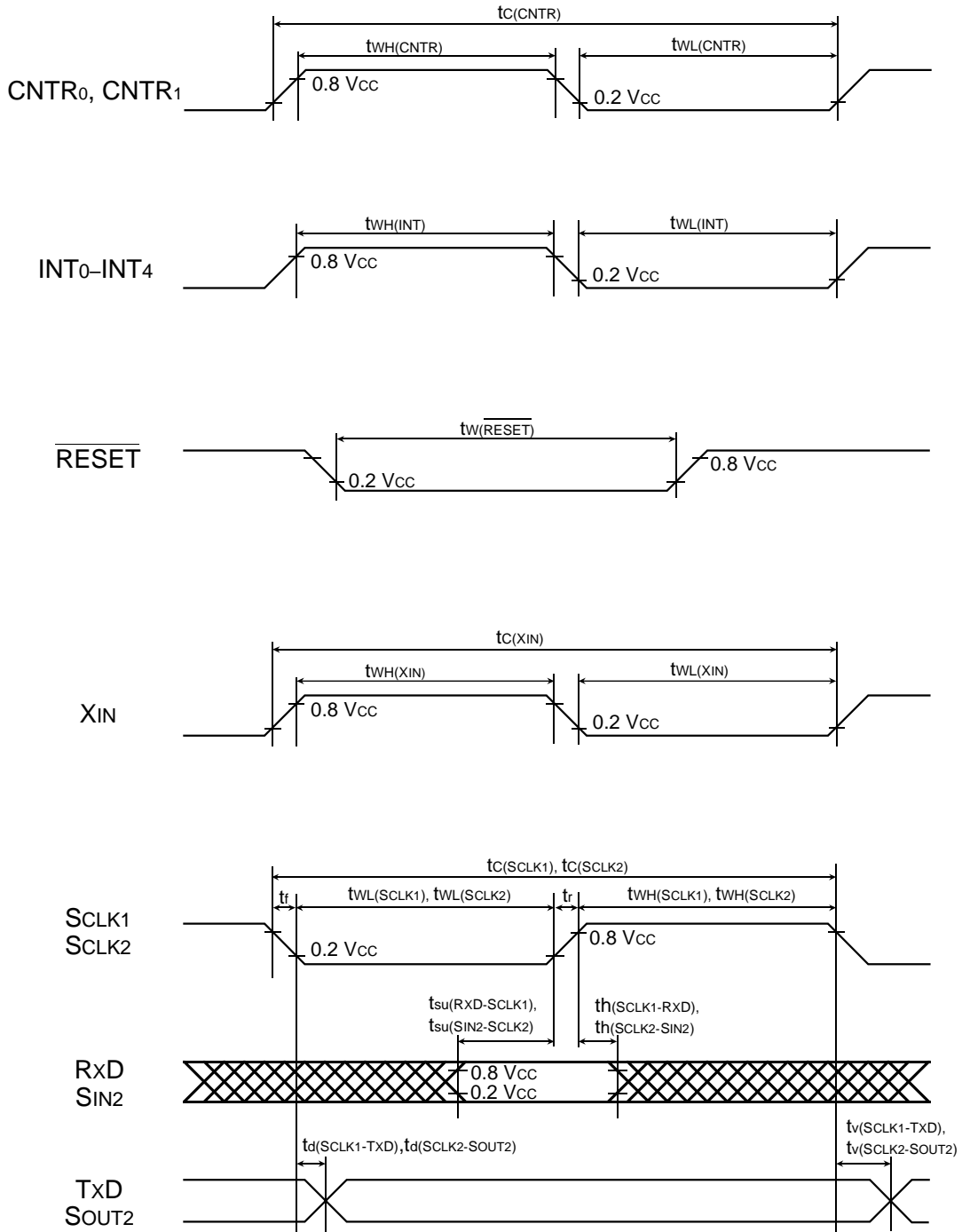
**Note 1:** The  $\overline{\text{RESETOUT}}$  output goes "H" in sync with the rise of the  $\phi$  clock that is anywhere between about 8 cycle and 13 cycles after the  $\overline{\text{RESET}}$  input goes "H".



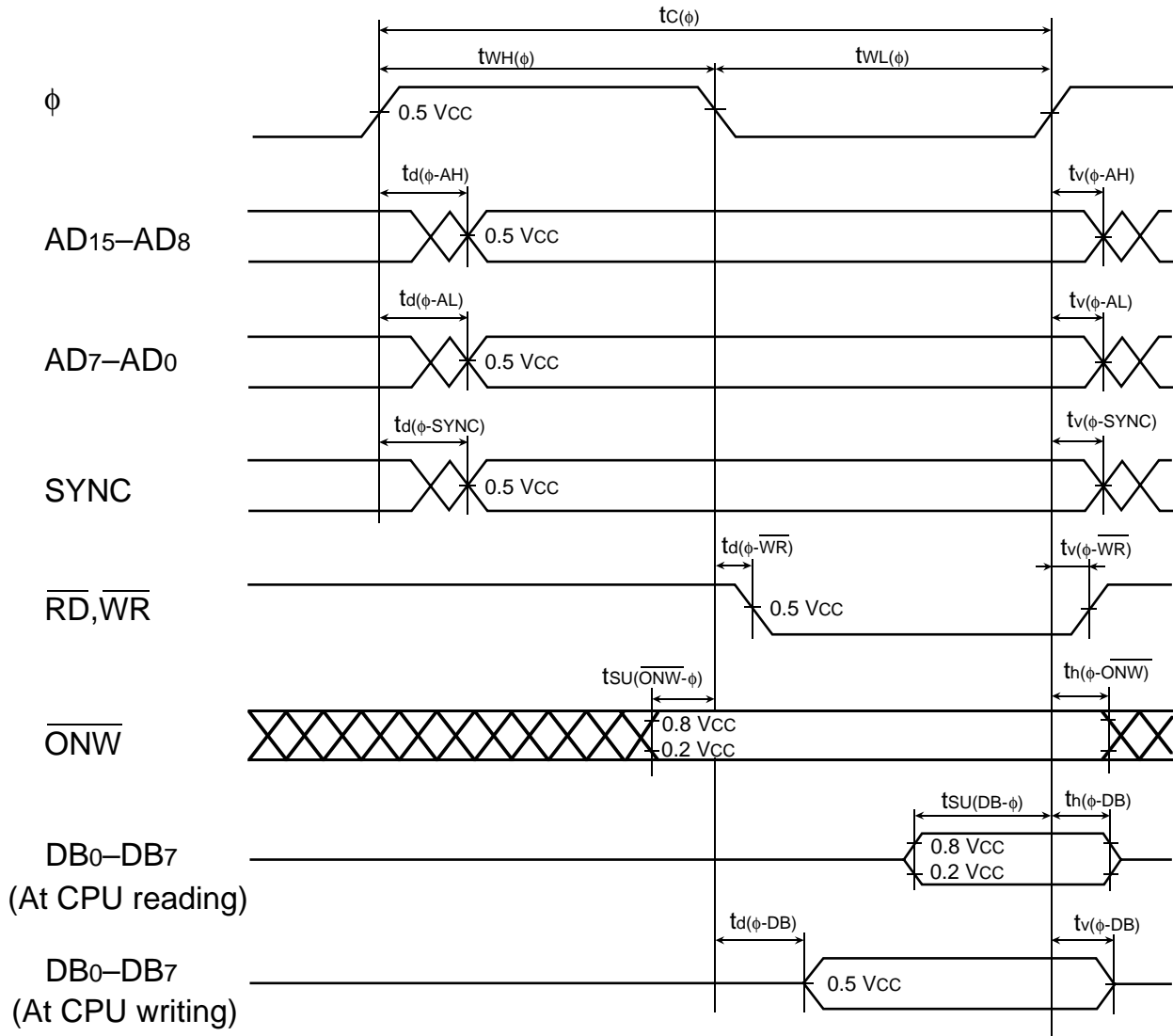
**Fig. 36** Circuit for measuring output switching characteristics

TIMING DIAGRAM

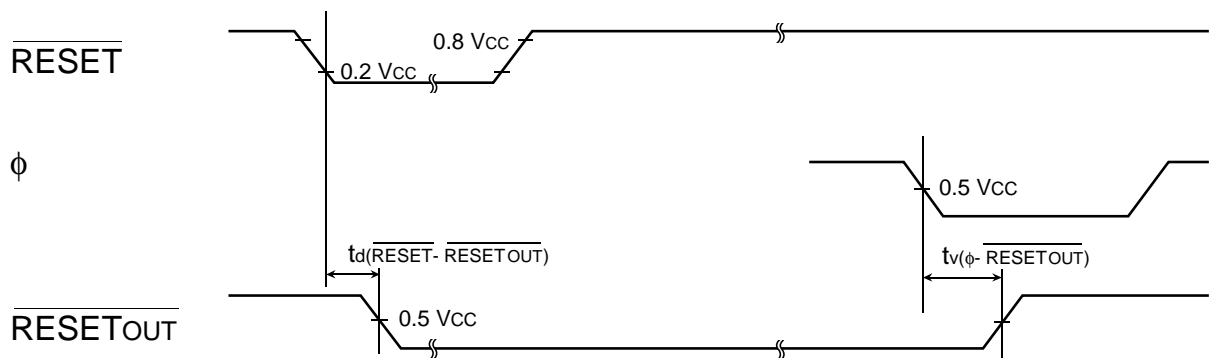
(1) Timing Diagram



(2) Timing Diagram in Memory Expansion Mode and Microprocessor Mode (a)

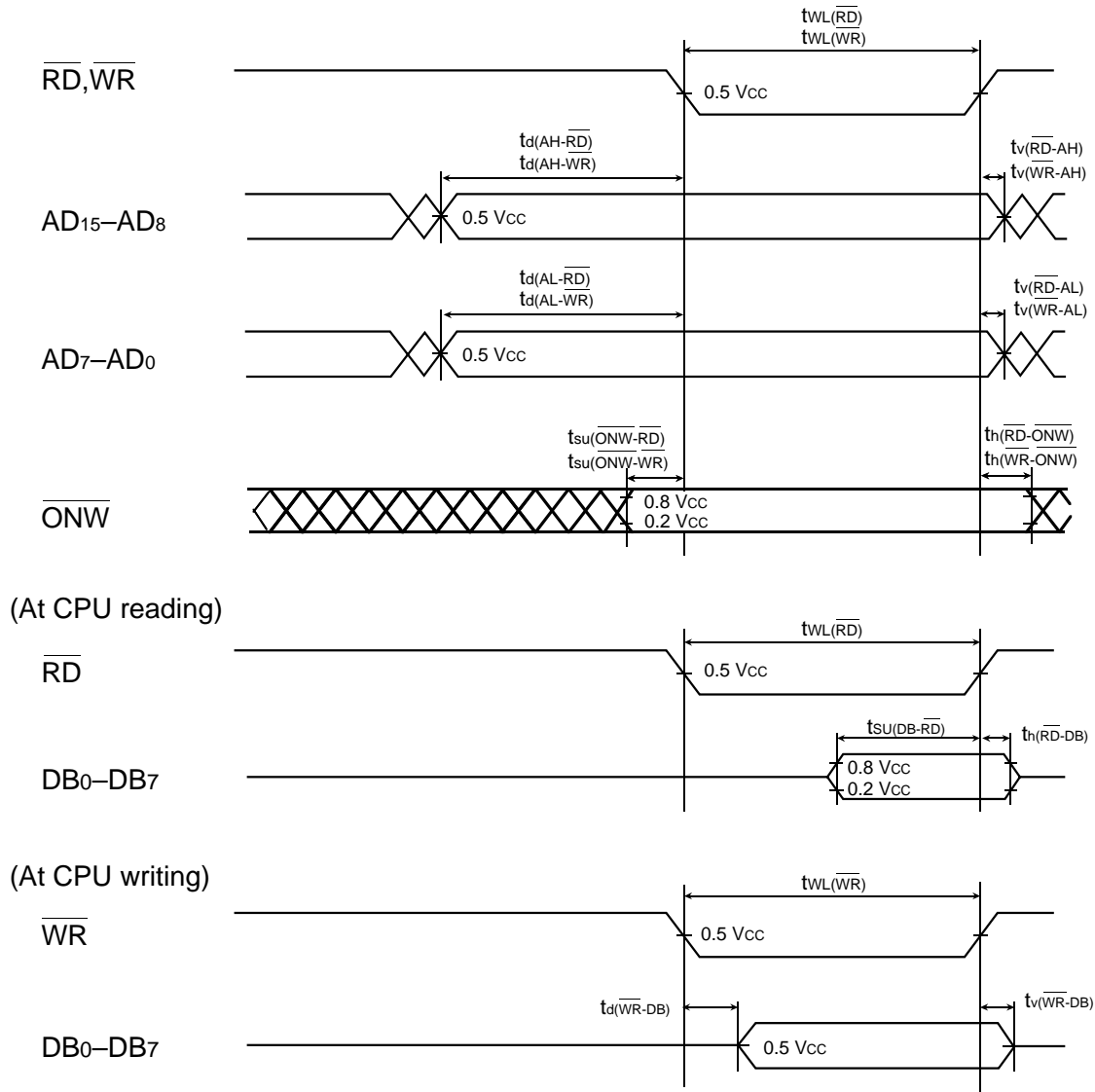


(3) Timing Diagram in Microprocessor Mode





(4) Timing Diagram in Memory Expansion Mode and Microprocessor Mode (b)



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