Version 2.0, 6 Dec 2007

F3 PWM controller

ICE3BS03LJG

Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell (Latched and frequency jitter Mode)

Power Management & Supply

Never stop thinking.

F3 PWM controller
ICE3BS03LJG
Revision History: 2007-12-6 Datasheet

Previous Version: 1.0

Page	Subjects (major changes since last revision)

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F3 PWM controller
ICE3BS03LJG

Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell (Latched and frequency jitter Mode)

PG-DSO-8

Product Highlights

- **Active Burst Mode to reach the lowest Standby Power Requirements < 100mW**
- **Built-in latched Off protection Mode and external latch enable function to increase robustness of the system**
- **Built-in and extendable blanking Window for high load jumps to increase system reliability**
- **Frequency jitter for low EMI**
- **Pb-free lead plating; RoHS compilant**

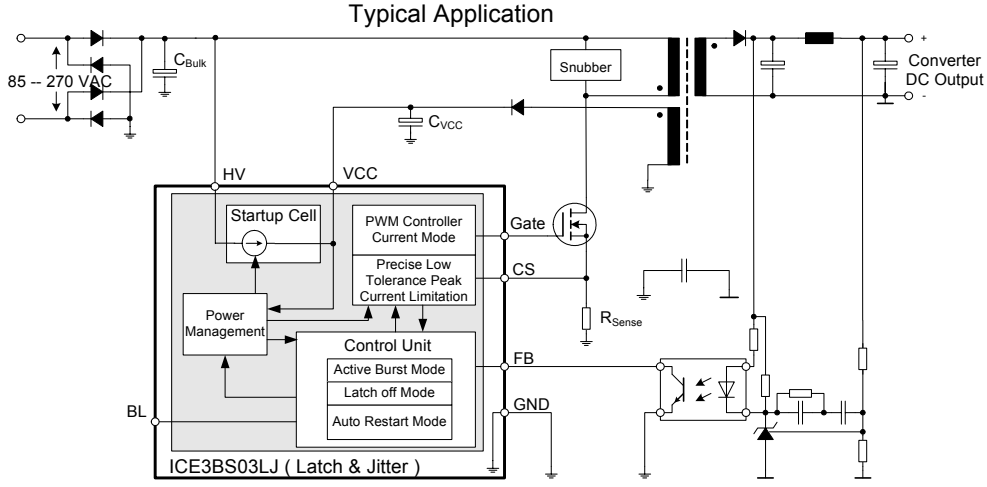
Features

- 500V Startup Cell switched off after Start Up
- Active Burst Mode for lowest Standby Power
- Fast load jump response in Active Burst Mode
- 65kHz internally fixed switching frequency
- Built-in Latched Off Protection Mode for Overtemperature, Overvoltage & Short Winding
- Auto Restart Protection Mode for Overload, Open Loop & VCC Undervoltage
- Built-in Soft Start
- Built-in blanking window with extendable blanking time for short duration high current
- External latch off enable function
- Max Duty Cycle 75%
- Overall tolerance of Current Limiting < ±5%
- Internal PWM Leading Edge Blanking
- BiCMOS technology provide wide VCC range
- Frequency jitter and soft gate driving for low EMI

Description

The ICE3BS03LJG is the latest version of the F3 controller for lowest standby power and low EMI features with both auto-restart and latch off protection features to enhance the system robustness. It targets for off-Line battery adapters, and low cost SMPS for low to medium power range such as application for the DVD R/W, DVD Combi, Blue Ray DVD player and recorder, set top box, charger, note book adapter, etc. The inherited outstanding features includes 500V startup cell, active burst mode (achieve the lowest standby power; i.e. <100 mV at no load with Vin=270Vac) and propagation delay compensation (accurate output power limit for wide range input), modulated gate drive (low EMI), etc. The newly added technology and features can further enhance the features. It includes BiCMOS technology (further lower power consumption and extend Vcc operating range to 26V), frequency jittering feature (low EMI), built-in soft start, built-in blanking window with extendable blanking time for high load jump, external latch off enable pin (feasible for extra protection), etc. Therefore, ICE3BS03LJG is a versatile PWM controller for low to medium power application.

Typical Application



Type	Marking	Package	F_{osc}
ICE3BS03LJG	3BS3LJ	PG-DSO-8	65kHz

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1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DSO-8

Pin	Symbol	Function
1	BL	extended Blanking and Latch off enable
2	FB	Feedback
3	CS	Current Sense
4	Gate	Gate driver output
5	HV	High Voltage input
6	n.c.	Not Connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

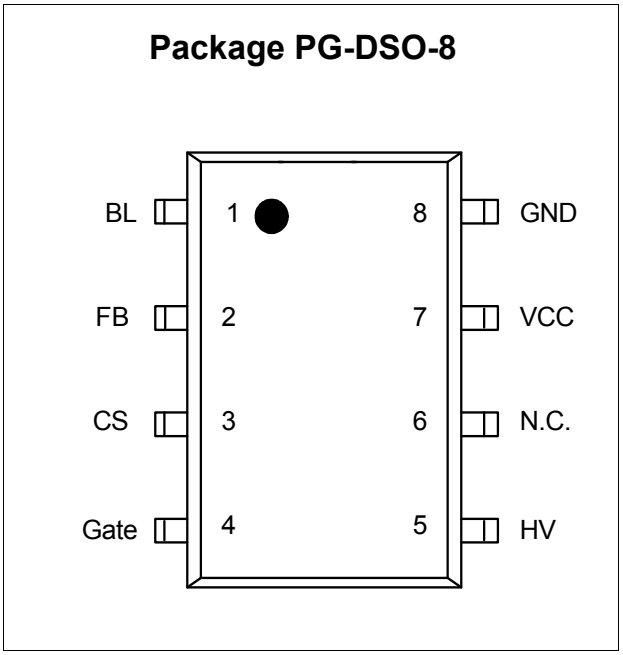


Figure 1 Pin Configuration PG-DSO-8(top view)

1.2 Pin Functionality

BL (extended Blanking and Latch off enable)

The BL pin combines the functions of extendable blanking time for entering the Auto Restart Protection Mode and the external latch off enable. The extendable blanking time function is to extend the built-in 20ms blanking time by adding an external capacitor at BL to ground. The external latch off enable function is an external access to latch off the IC. It is triggered by pulling down the BL pin to less than 0.25V.

FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal is the only control in case of light load at the Active Burst Mode.

CS (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the Power MOSFET. If CS reaches the internal threshold of the Current Limit Comparator, the Drive r output is immediately switched off. Furthermore, this current information can be used to realize the Current Mode operation through the PWM-Comparator where it compares with FB signal.

Gate

The Gate pin is the output of the internal driver stage connected to the Gate of an external power MOSFET.

HV (High Voltage)

The high voltage Pin is connected to the rectified DC input voltage. It is the input for the integrated 500V Startup cell.

VCC (Power supply)

The VCC pin is the positive supply of the IC. The operating range is between 10.5V and 26V.

GND (Ground)

The GND pin is the ground of the controller.

2 Representative Blockdiagram

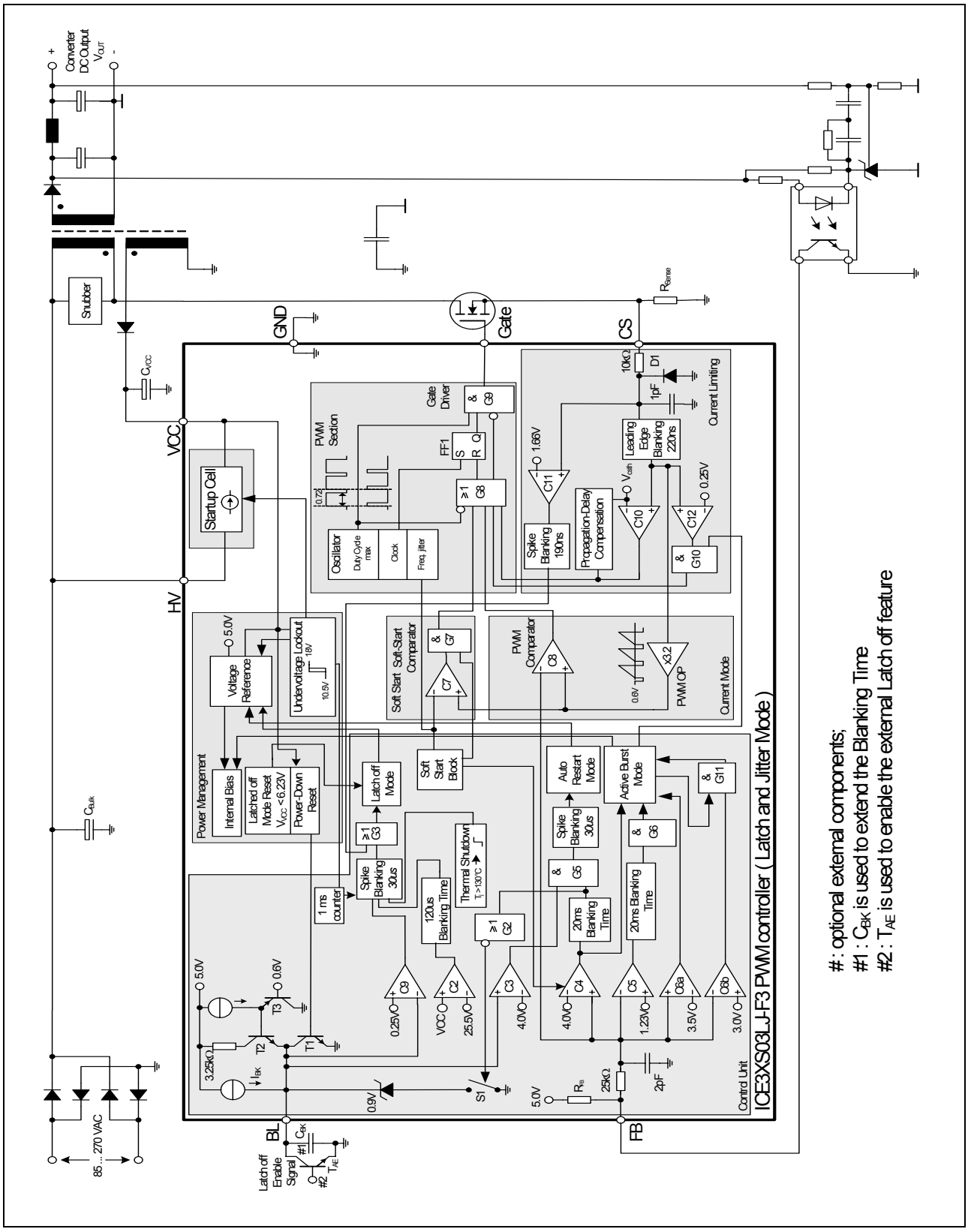


Figure 2 Representative Blockdiagram

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

ICE3BS03LJG is an enhanced version of the F3 PWM controller (ICE3xS02) for the low to medium power application. The particular enhanced features are the built-in features for soft start, blanking window and frequency jitter. It also provides the flexibility to increase the blanking window by simply adding capacitor in BL pin. To increase the robustness and flexibility of the protection feature, an external latch-off enable feature is added. Moreover, the proven outstanding features in F3 PWM controller are still remained such as the active burst mode, propagation delay compensation, modulated gate drive, protection for Vcc overvoltage, over temperature, over load, open loop, etc.

The intelligent Active Burst Mode at Standby Mode can effective obtain the lowest Standby Power at minimum load and no load conditions. After entering this burst mode, there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on V_{out} is minimized. V_{out} is on well controlled in this mode.

The usual externally connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore, a high voltage Startup Cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 18V is exceeded. The external startup resistor is no longer necessary as this Startup Cell can directly connected to the input bulk capacitor. Power losses are therefore reduced. This increases the efficiency under light load conditions drastically.

Adopting the BiCMOS technology, it can further decrease the power consumption and provide a even better standby input power. Besides, it also increases the design flexibility as the Vcc voltage range is extended to 26V.

The built-in soft start time at 20ms can provide sufficient timing to reduce the over-stress at power MOSFET and the output rectifier during startup.

There are 2 modes of blanking time for high load jumps; the basic mode and the extendable mode. The blanking time for the basic mode is set at 20ms while the extendable mode will increase the blanking time at basic mode by adding external capacitor at the BL pin. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

In order to increase the robustness and safety of the system, the IC provides 2 levels of protection modes: Latched Off Mode and Auto Restart Mode. The Latched Off Mode is only entered under dangerous conditions which can damage the SMPS if not switched off immediately. A restart of the system can only be done by recycling the AC line. In addition, for this enhanced version, there is an external Latch Enable function provided to increase the flexibility in protection. When the BL pin is pulled down to less than 0.25V, the Latch Off Mode is triggered.

The Auto Restart Mode reduces the average power conversion to a minimum under unsafe operating conditions. This is necessary for a prolonged fault condition which could otherwise lead to a destruction of the SMPS over time. Once the malfunction is removed, normal operation is automatically retained after the next Start Up Phase.

The internal precise peak current control reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the maximum power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage, which is required for wide range SMPS. Thus there is no need for the over-sizing of the SMPS, e.g. the transformer and the output diode.

Furthermore, this enhanced version implements the frequency jitter mode to the switching clock and modulated gate drive signal at the Gate pin such that the EMI noise will be effectively reduced.

3.2 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC}. When the SMPS is plugged to the main line, the internal Startup Cell is biased and starts to charge the external capacitor C_{VCC} which is connected to the VCC pin. This VCC charge current is controlled to 0.9mA by the Startup Cell. When the V_{VCC} exceeds the on-threshold V_{CCon}=18V, the bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on a hysteresis start up voltage is implemented. The switch-off of the controller can only take place after Active Mode was entered and V_{VCC} falls below 10.5V. The maximum current consumption before the controller is activated is about 250µA.

When V_{VCC} falls below the off-threshold V_{CCoff}=10.5V, the bias circuit switched off and the soft start counter is

reset. Thus it is ensured that at every startup cycle the soft start starts at zero.

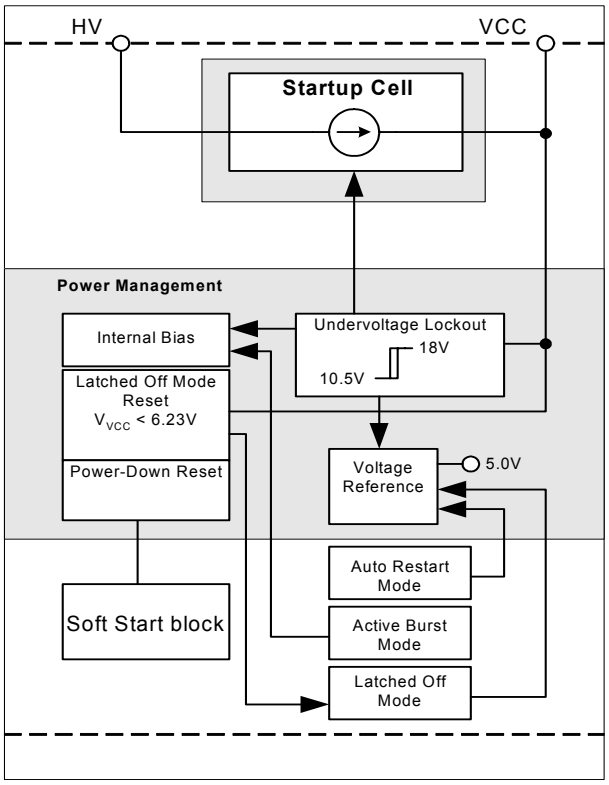


Figure 3 Power Management

The internal bias circuit is switched off if Latched Off Mode or Auto Restart Mode is entered. The current consumption is then reduced to 250µA.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require re-cycling the AC line. In case Latched Off Mode is entered, VCC needs to be dropped below 6.23V to reset the Latched Off Mode. This is done usually by re-cycling the AC line.

When Active Burst Mode is entered, the internal Bias is switched off most of the time but the Voltage Reference is kept alive in order to reduce the current consumption below 450µA.

3.3 Improved Current Mode

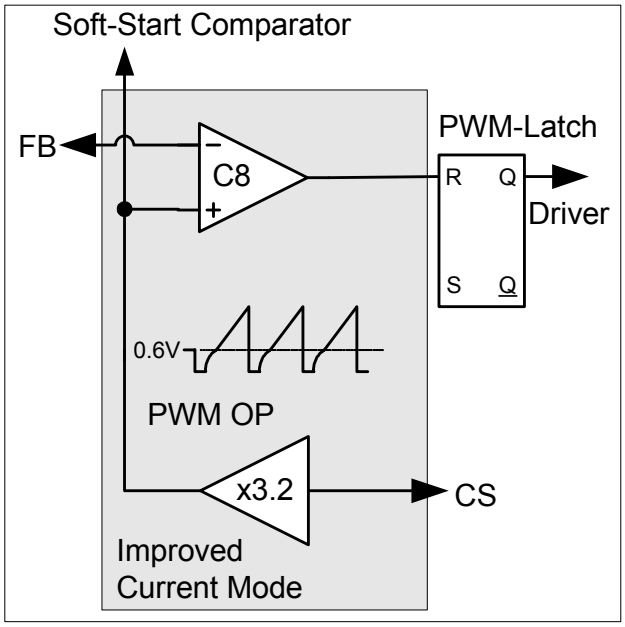


Figure 4 Current Mode

Current Mode means the duty cycle is controlled by the slope of the primary current. This is done by comparing the FB signal with the amplified current sense signal.

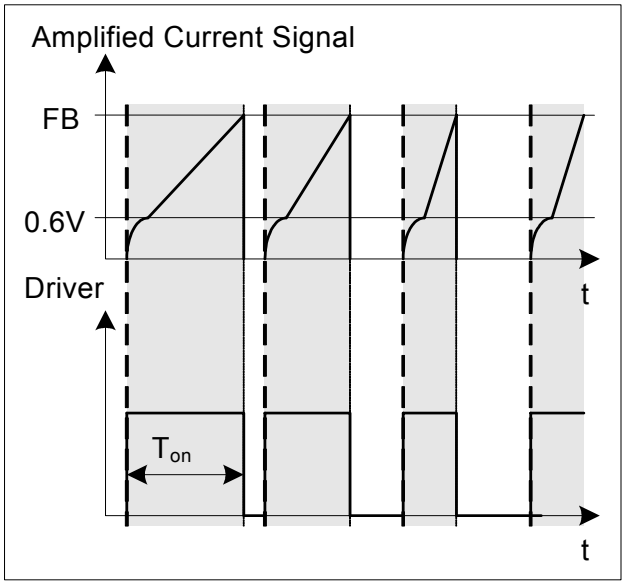


Figure 5 Pulse Width Modulation

In case the amplified current sense signal exceeds the FB signal, the on-time T_{on} of the driver is finished by resetting the PWM-Latch (see Figure 5).

The primary current is sensed by the external series resistor R_{Sense} inserted in the source of the external power MOSFET. By means of Current Mode regulation, the secondary output voltage is insensitive

to the line variations. The current waveform slope will change with the line variation, which controls the duty cycle.

The external R_{Sense} allows an individual adjustment of the maximum source current of the external power MOSFET.

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T2, the voltage source V1 and a resistor R1 (see Figure 6). Every time the oscillator shuts down for maximum duty cycle limitation the switch T2 is closed by V_{OSC}. When the oscillator triggers the Gate Driver, T2 is opened so that the voltage ramp can start.

In case of light load the amplified current ramp is too small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the time delay circuit which is triggered by the inverted V_{OSC} signal, the Gate Driver is switched-off until it reaches approximately 156ns delay time (see Figure 7). It allows the duty cycle to be reduced continuously till 0 % by decreasing V_{FB} below that threshold.

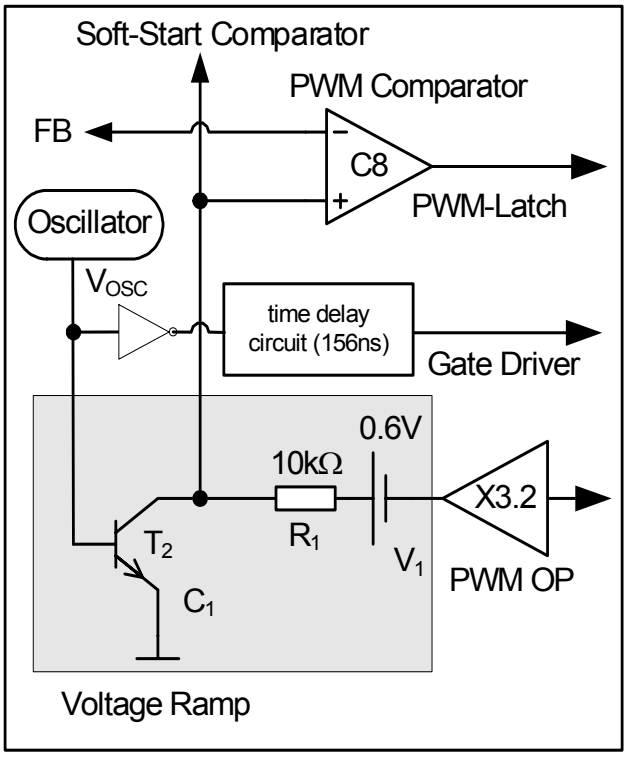


Figure 6 Improved Current Mode

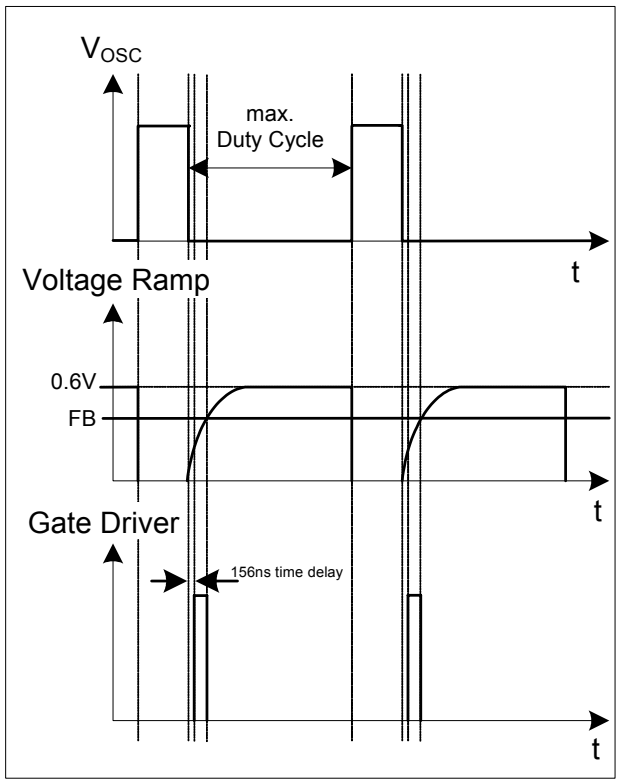


Figure 7 Light Load Conditions

3.3.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor R_{Sense} connected to pin CS. R_{Sense} converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.2 by PWM OP. The output of the PWM-OP is connected to the voltage source V_1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator C8 and the Soft-Start-Comparator (see Figure 6).

3.3.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the external power MOSFET with the feedback signal V_{FB} (see Figure 8). V_{FB} is created by an external optocoupler or external transistor in combination with the internal pull-up resistor R_{FB} and provides the load information of the feedback circuitry. When the amplified current signal of the external power MOSFET exceeds the signal V_{FB} the PWM-Comparator switches off the Gate Driver.

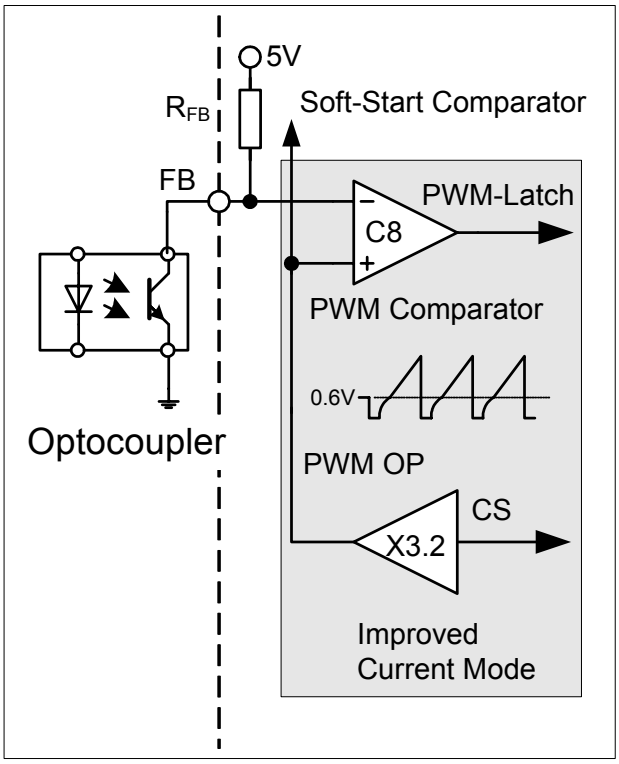


Figure 8 PWM Controlling

3.4 Startup Phase

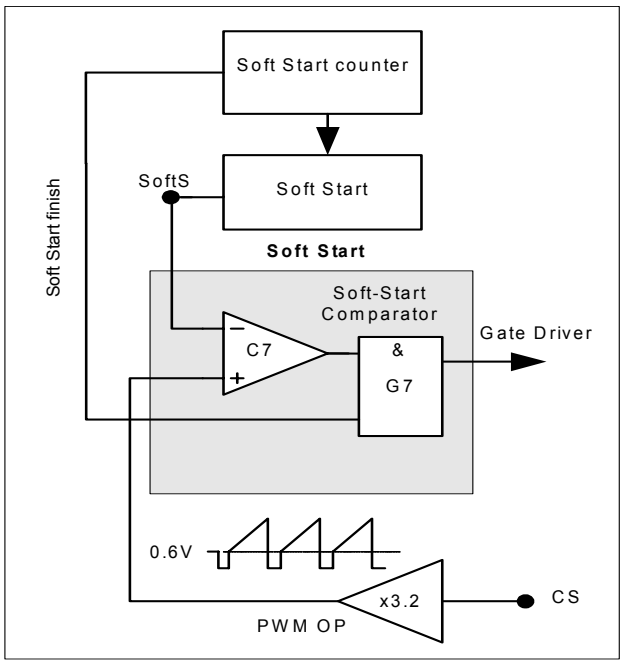


Figure 9 Soft Start

In the Startup Phase, the IC provides a Soft Start period to control the maximum primary current by means of a duty cycle limitation. The Soft Start function is a built-in function and it is controlled by an internal counter.

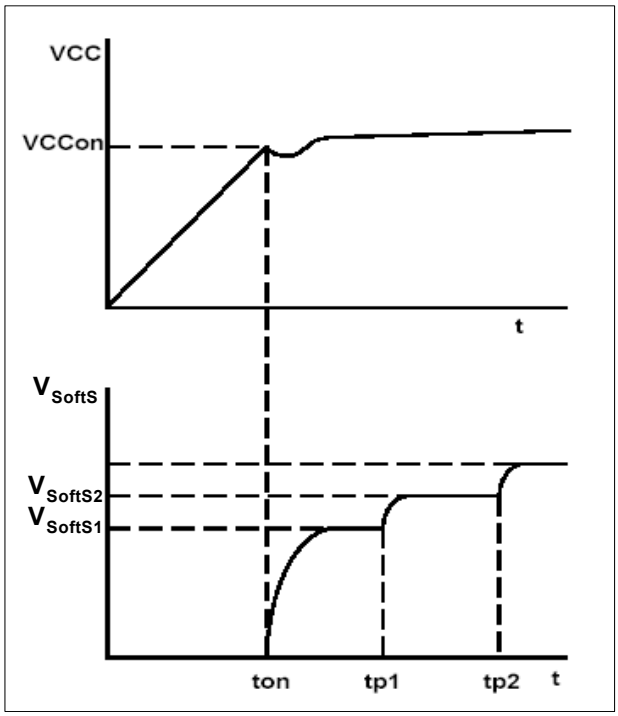


Figure 10 Soft Start Phase

When the V_{VCC} exceeds the on-threshold voltage, the IC starts the Soft Start mode (see Figure 10).

The function is realized by an internal Soft Start resistor, a n current sink and a counter. And the amplitude of the current sink is controlled by the counter (see Figure 11).

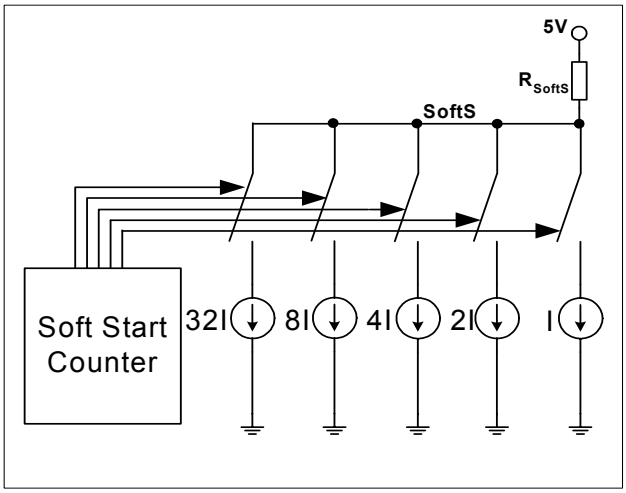


Figure 11 Soft Start Circuit

After the IC is switched on, the V_{SFOFTS} voltage is controlled such that the voltage is increased stepwisely (32 steps) with the increase of the counts. The Soft Start counter would send a signal to the current sink control in every 600us such that the current sink

decrease gradually and the duty ratio of the gate drive increases gradually. The Soft Start will be finished in 20ms ($T_{Soft-Start}$) after the IC is switched on. At the end of the Soft Start period, the current sink is switched off.

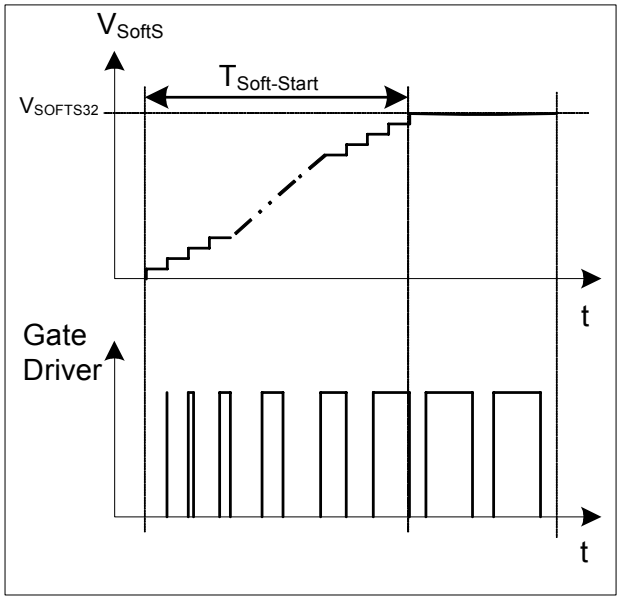


Figure 12 Gate drive signal under Soft-Start Phase

Within the soft start period, the duty cycle is increasing from zero to maximum gradually (see Figure 12).

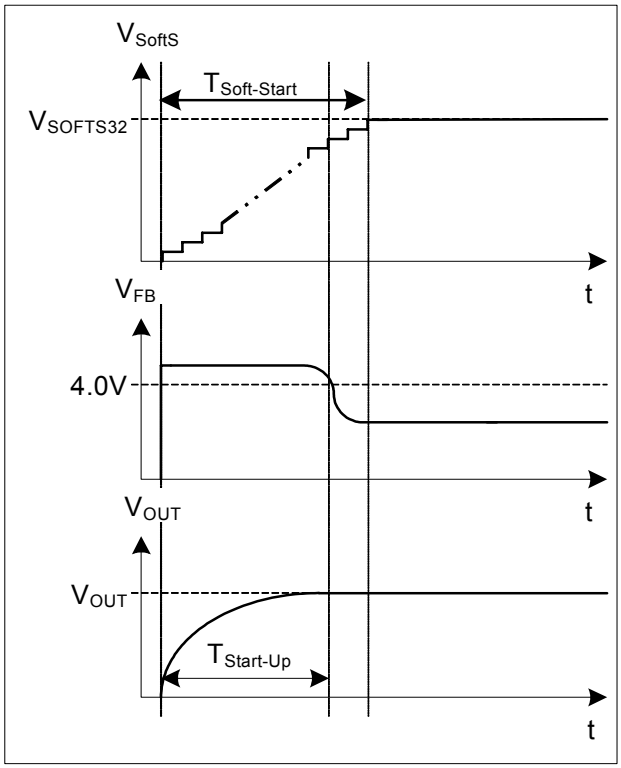


Figure 13 Start Up Phase

In addition to Start-Up , Soft-Start is also activated at each restart attempt during Auto Restart.

The Start-Up time $T_{Start-Up}$ before the converter output voltage V_{OUT} is settled, must be shorter than the Soft-Start Phase $T_{Soft-Start}$ (see Figure 13).

By means of Soft-Start there is an effective minimization of current and voltage stresses on the external power MOSFET, the clamp circuit and the output overshoot and it helps to prevent saturation of the transformer during Start-Up.

3.5 PWM Section

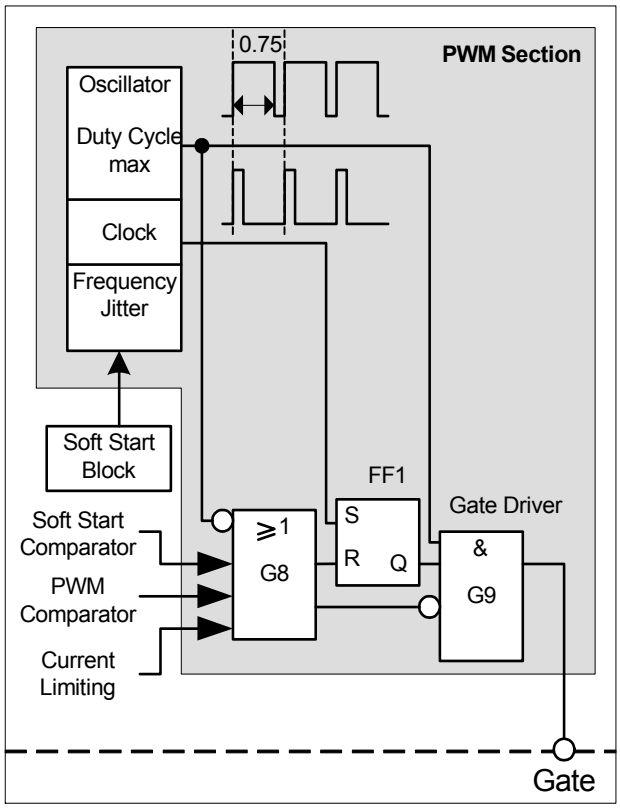


Figure 14 PWM Section Block

3.5.1 Oscillator

The oscillator generates a fixed frequency of 65KHz with frequency jittering of ±4% (which is ±2.6KHz) at a jittering period of 4ms.

A capacitor, a current source and a current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max}=0.75.

Once the Soft Start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the Soft

Start block. Then the switching frequency is varied in range of 65KHz ± 2.6KHz at period of 4ms.

3.5.2 PWM-Latch FF

The output of the oscillator block provides continuous pulse to the PWM-Latch which turns on/off the external power MOSFET. After the PWM-Latch is set, it is reset by the PWM comparator, the Soft Start comparator or the Current -Limit comparator. When it is in reset mode, the output of the gate driver is shut down immediately.

3.5.3 Gate Driver

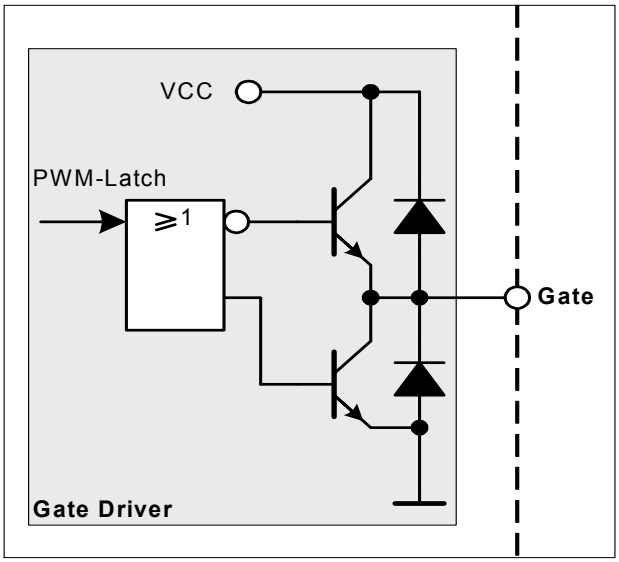


Figure 15 Gate Driver

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the external power MOSFET threshold. This is achieved by a slope control of the rising edge at the gate driver's output (see Figure 16).

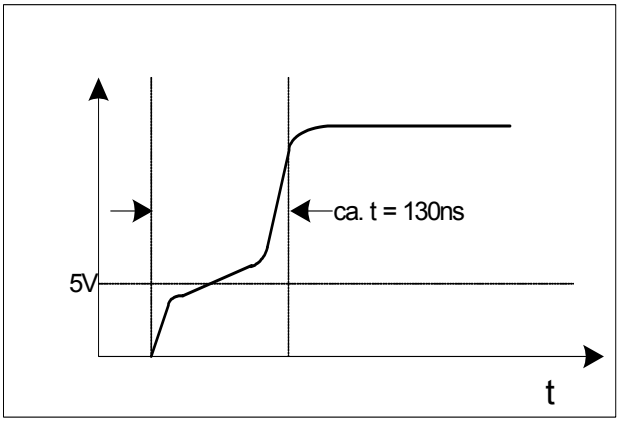


Figure 16 Gate Rising Slope

Thus the leading switch on spike is minimized. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During power up, when VCC is below the undervoltage lockout threshold V_{VCCoff}, the output of the Gate Driver is set to low in order to disable power transfer to the secondary side.

3.6 Current Limiting

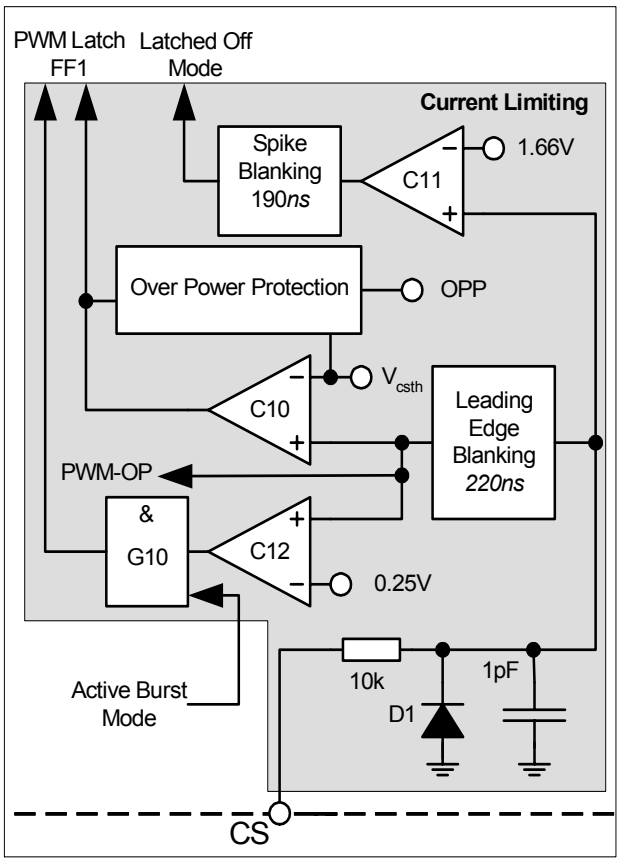


Figure 17 Current Limiting Block

There is a cycle by cycle peak current limiting operation realized by the Current-Limit comparator C10. The source current of the external power MOSFET is sensed via an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed into the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth}, the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1.

A Propagation Delay Compensation is added to support the immediate shut down of the external power MOSFET with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to minimal.

In order to prevent the current limit from distortions caused by leading edge spikes, a Leading Edge

Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the AND Gate G10 if Active Burst Mode is entered. When it is activated, the current limiting is reduced to 0.25V. This voltage level determines the maximum power level in Active Burst Mode.

Furthermore, the comparator C11 is implemented to detect dangerous current levels which could occur if there is a short winding in the transformer or the secondary diode is shorten. To ensure that there is no accidentally entering of the Latched Mode by the comparator C11, a 190 ns spike blanking time is integrated in the output path of comparator C11.

3.6.1 Leading Edge Blanking

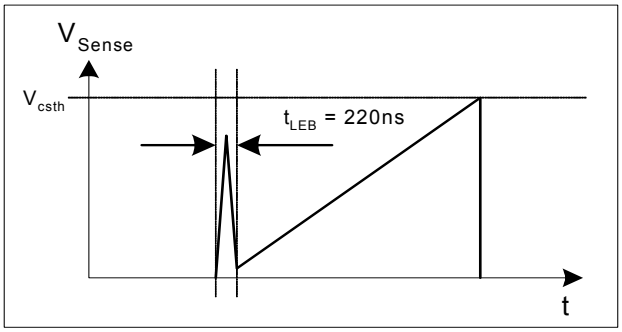


Figure 18 Leading Edge Blanking

Whenever the power MOSFET is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220ns.

3.6.2 Propagation Delay Compensation

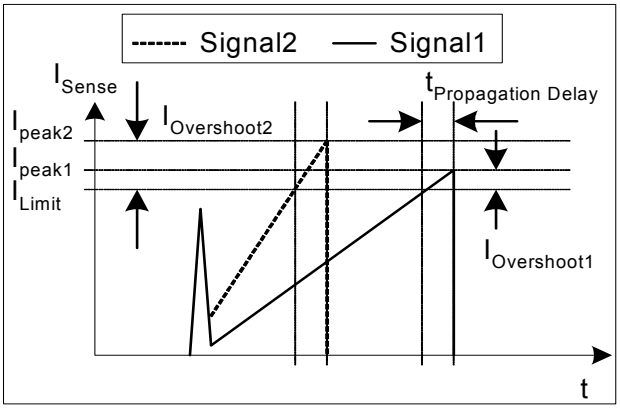


Figure 19 Current Limiting

In case of overcurrent detection, there is always propagation delay to switch off the external power MOSFET. An overshoot of the peak current I_{peak} is induced to the delay, which depends on the ratio of dI/dt of the peak current (see Figure 19).

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{csth} and the switching off of the external power MOSFET is compensated over temperature within a wide range. Current Limiting is then very accurate.

For example, I_{peak} = 0.5A with R_{Sense} = 2. The current sense threshold is set to a static voltage level V_{csth}=1V without Propagation Delay Compensation. A current ramp of dI/dt = 0.4A/µs, or dV_{Sense}/dt = 0.8V/µs, and a propagation delay time of $t_{Propagation\ Delay}$ =180ns leads to an I_{peak} overshoot of 14.4%. With the propagation delay compensation, the overshoot is only around 2% (see Figure 20).

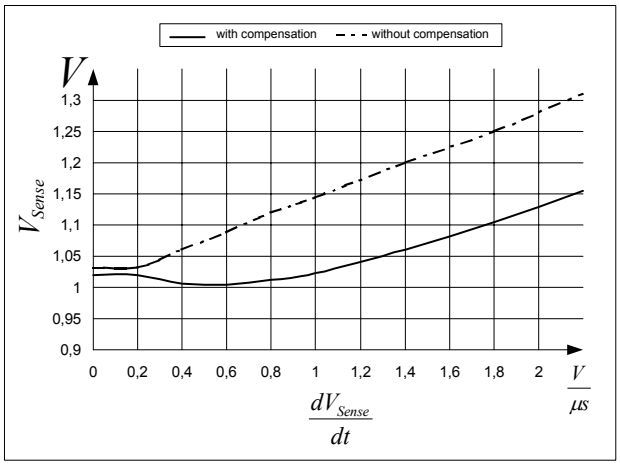


Figure 20 Overcurrent Shutdown

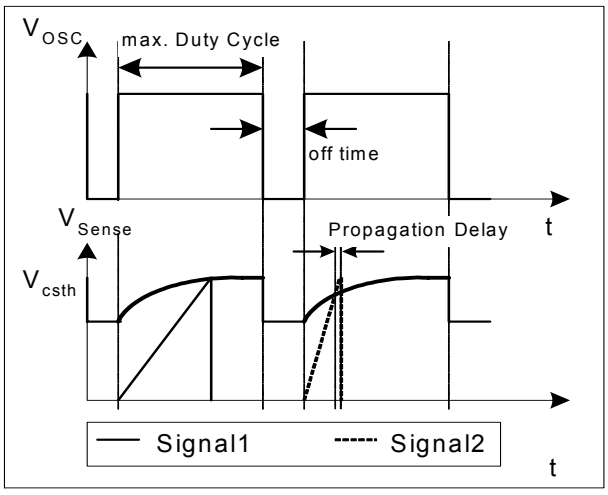


Figure 21 Dynamic Voltage Threshold V_{csth}

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (see Figure 21). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

3.7 Control Unit

The Control Unit contains the functions for Active Burst Mode, Auto Restart Mode and Latched Off Mode. The Active Burst Mode and the Auto Restart Mode both have 20ms internal Blanking Time. For the Auto Restart Mode, a further extendable Blanking Time is achieved by adding external capacitor at BL pin. By means of this Blanking Time, the IC avoids entering into these two modes accidentally. Furthermore those buffer time for the overload detection is very useful for the application that works in low current but requires a short duration of high current occasionally.

3.7.1 Basic and Extendable Blanking Mode

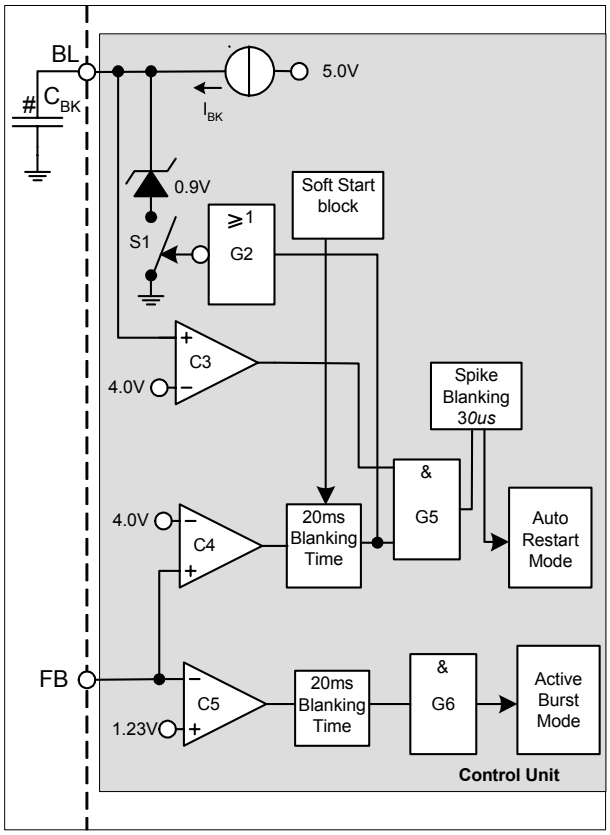


Figure 22 Basic and Extendable Blanking Mode

There are 2 kinds of Blanking mode; basic mode and the extendable mode. The basic mode has an internal pre-set 20ms blanking time while the extendable mode has extended blanking time to basic mode by connecting an external capacitor to the BL pin. For the extendable mode, the gate G5 is blocked even though the 20 ms blanking time is reached if an external capacitor C_{BK} is added to BL pin. While the 20 ms blanking time is passed, the switch S1 is opened by G2. Then the 0.9V clamped voltage at BL pin is charged to 4.0V through the internal I_{BK} constant current. Then G5 is enabled by comparator C3. After the 30us spike blanking time, the Auto Restart Mode is activated.

For example, if C_{BK} = 0.22uF, I_{BK} = 13uA

Blanking time = 20ms + C_{BK} x (4.0 - 0.9) / I_{BK} = 72ms

The 20ms blanking time circuit after C4 is disabled by the soft stat block such that the controller can start up properly.

The Active Burst Mode has basic blanking mode only while the Auto Restart Mode has both the basic and the extendable blanking mode.

3.7.2 Active Burst Mode

The IC enters Active Burst Mode under low load conditions. With the Active Burst Mode, the efficiency increases significantly at light load conditions while still maintaining a low ripple on V_{OUT} and a fast response on load jumps. During Active Burst Mode, the IC is controlled by the FB signal. Since the IC is always active, it can be a very fast response to the quick change at the FB signal. The Start up Cell is kept OFF in order to minimize the power loss.

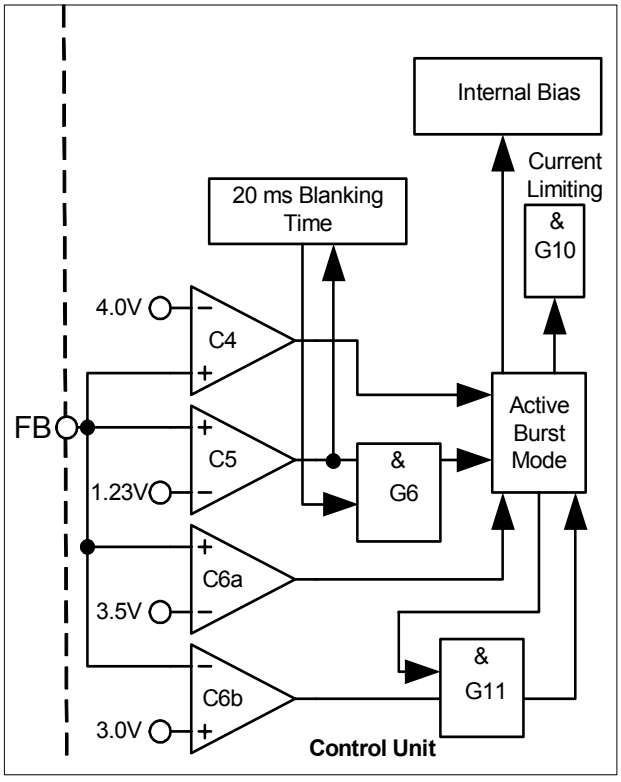


Figure 23 Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 23 shows the related components.

3.7.2.1 Entering Active Burst Mode

The FB signal is kept monitoring by the comparator C4. During normal operation, the internal blanking time counter is reset to 0. When FB signal falls below 1.23V, it starts to count. When the counter reach 20ms and FB signal is still below 1.23V, the system enters the Active Burst Mode. This time window prevents a sudden entering into the Active Burst Mode due to large load jumps.

After entering Active Burst Mode, a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC to approx. 450uA.

It needs the application to enforce the VCC voltage above the Undervoltage Lockout level of 10.5V such that the Startup Cell will not be switched on accidentally. Or otherwise the power loss will increase drastically. The minimum VCC level during Active Burst Mode depends on the load condition and the application. The lowest VCC level is reached at no load condition.

3.7.2.2 Working in Active Burst Mode

After entering the Active Burst Mode, the FB voltage rises as V_{OUT} starts to decrease, which is due to the inactive PWM section. The comparator C6a monitors the FB signal. If the voltage level is larger than 3.5V, the internal circuit will be activated; the Internal Bias circuit resumes and starts to provide switching pulse. In Active Burst Mode the gate G10 is released and the current limit is reduced to 0.25 V. In one hand, it can reduce the conduction loss and the other hand, it can reduce the audible noise. If the load at V_{OUT} is still kept unchanged, the FB signal will drop to 3.0V. At this level the C6b deactivates the internal circuit a gain by switching off the internal Bias. The gate G11 is active again as the burst flag is set after entering Active Burst Mode. In Active Burst Mode, the FB voltage is changing like a saw tooth between 3.0V and 3.5V (see Figure 24).

3.7.2.3 Leaving Active Burst Mode

The FB voltage will increase immediately if there is a high load jump. This is observed by the comparator C4. As the current limit is app. 25% during Active Burst Mode, a certain load jump is needed so that the FB signal can exceed 4.0V. At that time the comparator C4 resets the Active Burst Mode control which in turn blocks the comparator C12 by the gate G10. The maximum current can then be resumed to stabilize V_{OUT}.

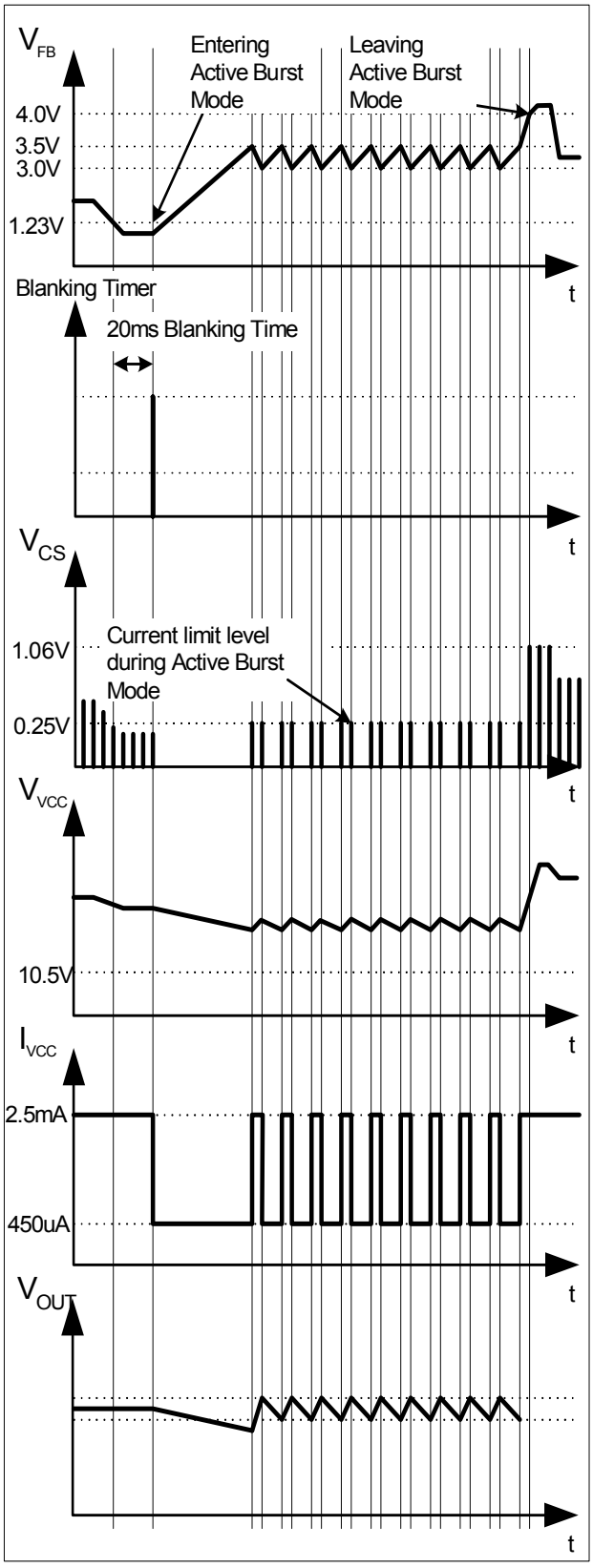


Figure 24 Signals in Active Burst Mode

3.7.3 Protection Modes

The IC provides several protection features which are separated into two categories. Some enter Latched Off Mode and the others enter Auto Restart Mode. Besides the pre-defined protection feature for the Latch off mode, there is also an external Latch off Enable pin for customer defined Latch off protection features. The Latched Off Mode can only be reset if VCC falls below 6.23V. Both modes prevent the SMPS from destructive states.The following table shows the relationship between possible system failures and the chosen protection modes.

VCC Overvoltage	Latched Off Mode
Overtemperature	Latched Off Mode
Short Winding/Short Diode	Latched Off Mode
BL pin < 0.25V	Latched Off Mode
Overload A	uto Restart Mode
Open Loop	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Short Optocoupler	Auto Restart Mode

3.7.3.1 Latched Off Mode

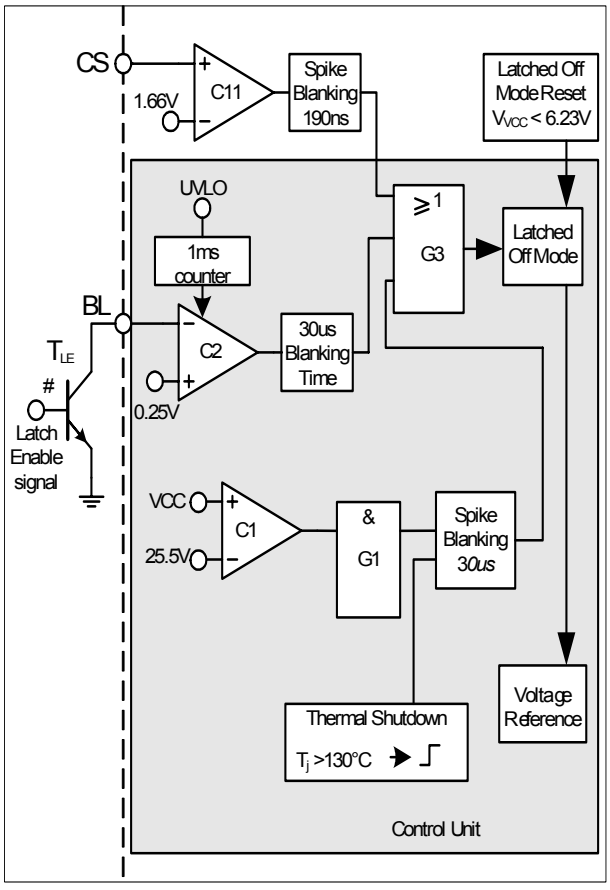


Figure 25 Latched Off Mode

The VCC voltage is observed by comparator C1. If the VCC voltage is > 25.5V, the overvoltage detection is activated. It enters the latch off mode.

The internal Voltage Reference is switched off most of the time once Latched Off Mode is entered in order to minimize the current consumption of the IC. This Latched Off Mode can only be reset if the V_{VCC} < 6.23V. In this mode, only the UVLO is working which controls the Startup Cell by switching on/off at V_{VCCon}/V_{VCCoff}. During this phase, the average current consumption is only 250µA. As there is no longer a self-supply by the auxiliary winding, the VCC drops . The Undervoltage Lockout switches on the integrated Startup Cell when VCC falls below 10.5V. The Startup Cell is switched off again when VCC has exceeded 18V. Once the Latched Off Mode was entered, there is no Start Up Phase whenever the VCC exceeds the switch-on level of the Undervoltage Lockout. Therefore the VCC voltage changes between the switch-on and switch-off levels of the Undervoltage Lockout with a saw tooth shape (see Figure 26).

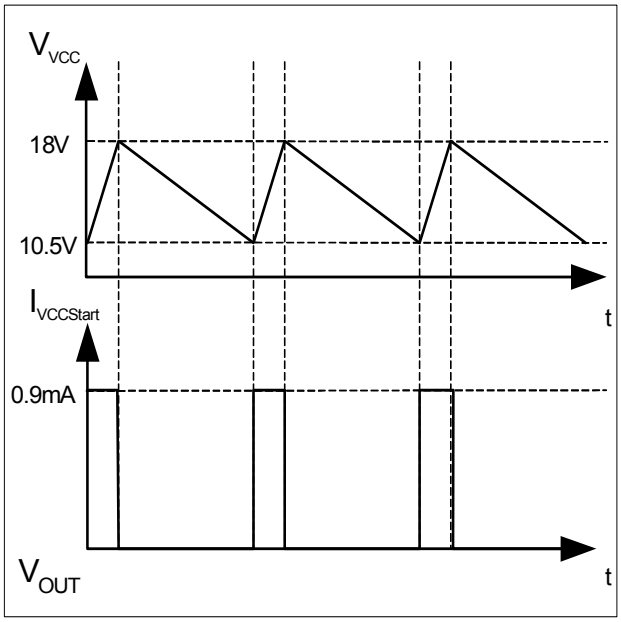


Figure 26 Signals in Latched Off Mode

The Thermal Shutdown block monitors the junction temperature of the IC. After detecting a junction temperature higher than latched thermal shutdown temperature; T_{jSD}, the Latched Off Mode is entered.

The signals coming from the temperature detection and VCC overvoltage detection are fed into a spike blanking with a time constant of 30µs in order to ensure the system reliability.

Furthermore, a short winding or short diode on the secondary side can be detected by the comparator C11 which is in parallel to the propagation delay compensated current limit comparator C10. In normal operating mode, comparator C10 controls the maximum level of the CS signal at 1.06V. If there is a

failure such as short winding or short diode, C10 is no longer able to limit the CS signal at 1.06V. Instead the comparator C11 detects the peak current voltage > 1.66V and enters the Latched Off Mode immediately in order to keep the SMPS in a safe stage.

In case the pre-defined Latch Off features are not sufficient, there is a customer defined external Latch Enable feature. The Latch Off Mode can be triggered by pulling down the BL pin to < 0.25V. It can simply add a trigger signal to the base of the externally added transistor, T_{LE} at the BL pin. To ensure this latch function will not be mis-triggered during start up, a 1ms delay time is implemented to blank the unstable signal.

3.7.3.2 Auto Restart Mode

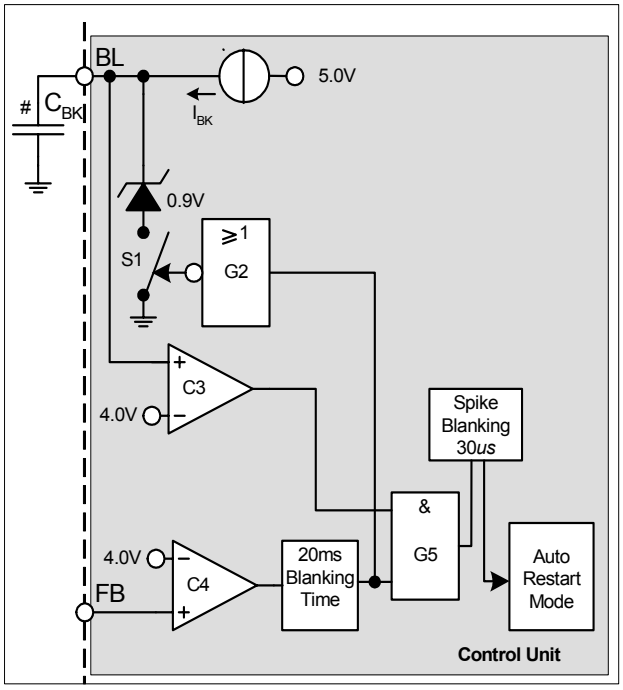


Figure 27 Auto Restart Mode

In case of Overload or Open Loop, the FB exceeds 4.0V which will be observed by comparator C4. Then the internal blanking counter starts to count. When it reaches 20ms, the switch S1 is released. Then the clamped voltage 0.9V at V_{BL} can increase. When there is no external capacitor C_{BK} connected, the V_{BL} will reach 4.0V immediately. When both the input signals at AND gate G5 is positive, the Auto-Restart Mode will be activated after the extra spike blanking time of 30us is elapsed. However, when an extra blanking time is needed, it can be achieved by adding an external capacitor, C_{BK}. A constant current source of I_{BK} will start to charge the capacitor C_{BK} from 0.9V to 4.0V after the switch S1 is released. The charging time from 0.9V to 4.0V are the extendable blanking time. If C_{BK} is 0.22uF and I_{BK} is 13uA, the extendable blanking time is around 52ms and the total blanking time is 72ms. In combining the FB and blanking time, there is a blanking window generated which prevents the system to enter Auto Restart Mode due to large load jumps.

In case of VCC undervoltage, the IC enters in to the Auto Restart Mode and starts a new startup cycle.

Short Optocoupler also leads to VCC undervoltage as there is no self supply after activating the internal reference and bias.

In contrast to the Latched Off Mode, there is always a Startup Phase with switching cycles in Auto Restart Mode. After this Start Up Phase, the conditions are again checked whether the failure mode is still present. Normal operation is resumed once the failure mode is removed that had caused the Auto Restart Mode.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HV Voltage	V_{HV}	-5	00	V	
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
FB Voltage	V_{FB}	-0.3	5.0	V	
CS Voltage	V_{CS}	-0.3	5.0	V	
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction -Ambient	R_{thJA}	-1	85	K/W	
ESD Capability (incl. Drain Pin)	V_{ESD}	-	2	kV	Human body model[1)]

[1)] According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	26	V	
Junction Temperature of Controller	T_{jCon}	-25	130	°C	Max value limited due to thermal shut down of controller

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 25 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	150	250	µA	V_{VCC} =16.5V
VCC Charge Current	$I_{VCCcharge1}$	--		5.0	mA	V_{VCC} = 0V
	$I_{VCCcharge2}$	0.55	0.90	1.60	mA	V_{VCC} = 1V
	$I_{VCCcharge3}$	-0	.7	-m	A	V_{VCC} =16.5V
Leakage Current of Start Up Cell	$I_{StartLeak}$	-0	.2	50	µA	V_{HV} = 450V, V_{VCC}=18V
Supply Current with Inactive Gate	$I_{VCCsup1}$	-1	.5	2.5	mA	
Supply Current with Active Gate	$I_{VCCsup2}$	-2	.5	4.2	mA	I_{FB} = 0A, C_{Load}=1nF
Supply Current in Latched Off Mode	$I_{VCClatch}$	-2	50	-	µA	I_{FB} = 0A
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-2	50	-	µA	I_{FB} = 0A
Supply Current in Active Burst Mode with Inactive Gate	$I_{VCCburst1}$	-	450	950	µA	V_{FB} = 2.5V
	$I_{VCCburst2}$	-	450	950	µA	V_{VCC} = 11.5V, V_{FB} = 2.5V
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis	V_{VCCon} V_{VCCoff} V_{VChys}	17.0 9.8 -	18.0 10.5 7.5	19.0 11.2 -	V V V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V_{REF}	4.90	5.00	5.10	V	measured at pin FB I_{FB} = 0

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	f_{OSC1}	56.5	65	73.7	kHz	
	f_{OSC2}	59.8	65.0	70.2	kHz	T_j = 25°C
Frequency Jittering Range	f_{jitter}	-±	2.6	-k	Hz	T_j = 25°C
Max. Duty Cycle	D_{max}	0.70	0.75	0.80		
Min. Duty Cycle	D_{min}	0-		-		V_{FB} < 0.3V
PWM-OP Gain	A_V	3.0	3.2	3.4		
Voltage Ramp Offset	$V_{Offset-Ramp}$	-0	.6	-	V	
V_{FB} Operating Range Min Level	V_{FBmin}	-0	.5	-V		
V_{FB} Operating Range Max level	V_{FBmax}	-	-	4.3	V	CS=1V, limited by Comparator C4[1)]
FB Pull-Up Resistor	R_{FB}	9	15.4	22	kΩ	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.4 Soft Start time

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft Start time	t_{SS}	-	20	-	ms	

4.3.5 Control Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Clamped V_{BL} voltage during Normal Operating Mode	V_{BLclmp}	0.85	0.90	0.95	V	V_{FB} = 4V
Blanking time voltage limit for Comparator C3	V_{BKC3}	3.85	4.00	4.15	V	
Over Load & Open Loop Detection Limit for Comparator C4	V_{FBC4}	3.85	4.00	4.15	V	
Active Burst Mode Level for Comparator C5	V_{FBC5}	1.12	1.23	1.34	V	
Active Burst Mode Level for Comparator C6a	V_{FBC6a}	3.35	3.50	3.65	V	After Active Burst Mode is entered
Active Burst Mode Level for Comparator C6b	V_{FBC6b}	2.88	3.00	3.12	V	After Active Burst Mode is entered
Overvoltage Detection Limit	V_{VCCOVP}	24.5	25.5	26.5	V	
Latch Enable level at BL pin	V_{LE}	0.17	0.25	0.33	V	> 30µs
Charging current at BL pin	I_{BK}	9.1	13.0	16.9	µA	Charge starts after the built-in 20ms blanking time elapsed
Latched Thermal Shutdown[1)]	T_{jSD}	130	140	150	°C	
Built-in Blanking Time for Overload Protection or enter Active Burst Mode	t_{BK}	-	20	-	ms	without external capacitor at BL pin
Inhibit Time for Latch Enable function during Start up	t_{IHLE}	-	1.0	-	ms	After IC turns on
Spike Blanking Time before Latch off or Auto Restart Protection	t_{Spike}	-3	0	-	µs	
Power Down Reset for Latched Mode	V_{VCCPD}	5.2	6.23	7.8	V	After Latched Off Mode is entered

1) The parameter is not subjected to production test - verified by design/characterization. The thermal shut down temperature refers to the junction temperature of the controller.

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} *and* V_{VCCPD}

4.3.6 Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay)	V_{csth}	0.99	1.06	1.13	V	dV_{sense} / dt = 0.6V/µs (see Figure 20)
Peak Current Limitation during Active Burst Mode	V_{CS2}	0.21	0.25	0.31	V	
Leading Edge Blanking	t_{LEB}	-2	20	-	ns	
CS Input Bias Current	I_{CSbias}	-1.5	-0.2	-	µA	V_{CS} =0V
Over Current Detection for Latched Off Mode	V_{CS1}	1.57	1.66	1.76	V	
CS Spike Blanking for Comparator C11	$t_{CSspike}$	-1	90	-	ns	

4.3.7 Driver Section

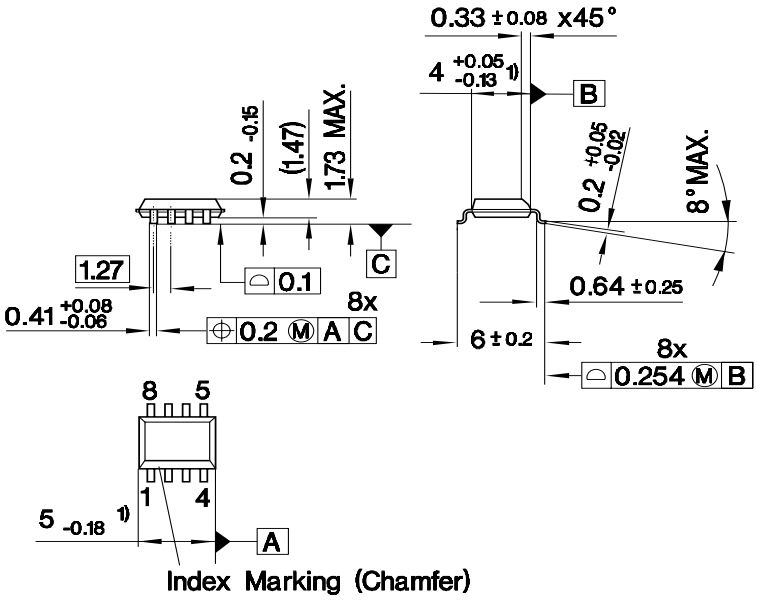
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	$V_{GATElow}$	--		1.2	V	V_{VCC} = 5 V I_{Gate} = 1 mA
		--		1.5	V	V_{VCC} = 5 V I_{Gate} = 5 mA
		-0	.8	-V		I_{Gate} = 0 A
		-1	.6	2.0	V	I_{Gate} = 20 mA
		-0.2	0.2	-	V	I_{Gate} = -20 mA
GATE High Voltage	$V_{GATEhigh}$	-1	0.0	-	V	V_{VCC} = 26V C_L = 680pF
		-9	.0	-V		V_{VCC} = 15V C_L = 680pF
		-8	.0	-V		V_{VCC} = V_{VCCoff} + 0.2V C_L = 680pF
GATE Rise Time (incl. Gate Rising Slope)	t_{rise}	-1	50	-n	s	V_{Gate} = 2V ...9V[1)] C_L = 680pF
GATE Fall Time	t_{fall}	-5	5	-	ns	V_{Gate} = 9V ...2V[1)] C_L = 680pF
GATE Current, Peak, Rising Edge	I_{GATE}	-0.17	-	-	A	C_L = 680pF[2)]
GATE Current, Peak, Falling Edge	I_{GATE}	-	-	0.39	A	C_L = 680pF[2)]

1) Transient reference value

2) The parameter is not subjected to production test - verified by design/characterization

5 Outline Dimension

PG-DSO-8
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 28 PG-DSO-8 (PB-free Plating Plastic Dual Small Outline)

Dimensions in mm

6 Marking

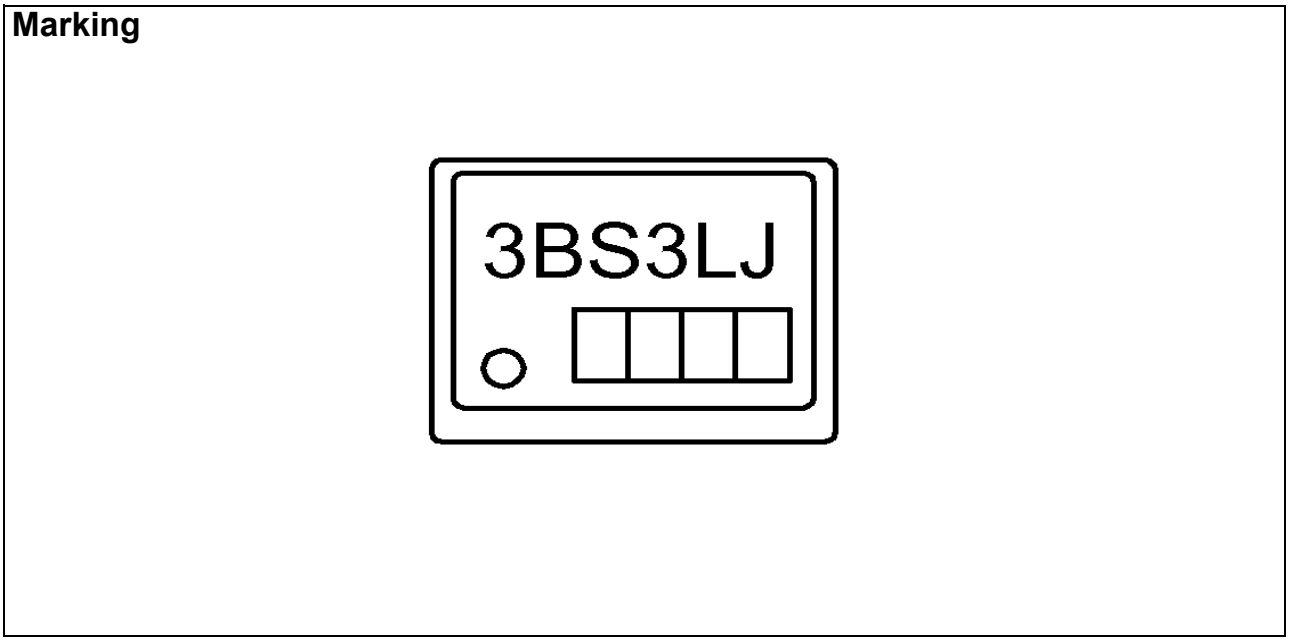


Figure 29 Marking for ICE3BS03LJG

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