All Silicon Delay Line

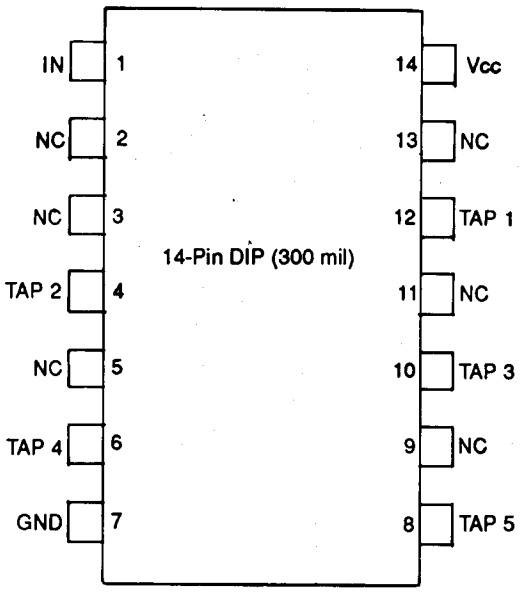
SERIES: 3D7005 — 5 Taps

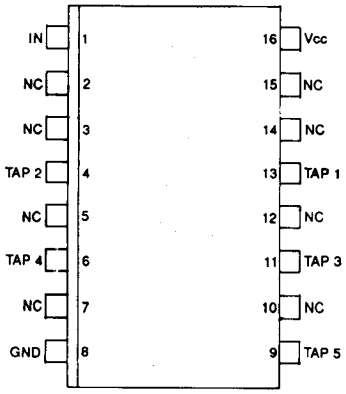
DESCRIPTION

The 3D7000* series delay line is a completely silicon delay line, which features unique circuits to compensate for temperature and power supply variations. It offers 5 & 10 equally spaced taps providing delays from 5 ns to 500 ns. This series comes in a standard 14 pin DIP package, which is compatible with other standard Hybrid delay lines. It is also offered in a 16 pin SOIC package for surface mount technology to reduce P.C. board area.

The 3D7000* series is designed to produce both leading and trailing edge delay time with equal precision. Each tap capable of driving up to ten 74LS type loads.

PIN DESCRIPTION





FEATURES

- **High operating frequency (100 MHz).**
- **Very low ground-bounce noise.**
- **Voltage & temperature compensated.**
- **Auto-Insertable.**
- **TTL/CMOS compatible, Low power CMOS.**
- **Vapor phase, IR and wave solderable.**

SPECIFICATIONS

- **Standard 14 pin DIP & 16 pin SOIC.**
- **Leading & trailing edge accuracy.**
- **Delay tolerance:** ± 5% or ± 2 ns, whichever is greater (others on request).
- **Custom delays available:** Any increment from 5 to 50 ns not listed.
- **Minimum input pulse width:** 20% of total delay.
- **Delay time vs. Vcc:** 1.5 ns or 2% for 5 Vdc ± 5%.
- **Temperature coefficient of delay:** ±1 ns or ± 3%, whichever is greater (0 to 70°C). (Others on request.)

TABLE

Part Number	Total Delay (ns)	Delay/Tap (ns)	Max Operating Freq (MHz)	Part Number	Total Delay (ns)	Delay/Tap (ns)	Max Operating Freq (MHz)
3D7005-25	25	5	67	3D7005-80	80	16	19
3D7005-30	30	6	55	3D7005-100	100	20	16
3D7005-35	35	7	43	3D7005-125	125	25	15
3D7005-40	40	8	41	3D7005-150	150	30	11
3D7005-45	45	9	37	3D7005-200	200	40	8
3D7005-50	50	10	33	3D7005-225	225	45	7
3D7005-60	60	12	26	3D7005-250	250	50	6
3D7005-75	75	15	22				

*Patent Pending

3 Mt. Prospect Avenue, Clifton, New Jersey 07013 ■ (201) 773-2299 ■ FAX (201) 773-9672 ■ TWX 710-989-7008

SERIES: 3D7005 (5 Taps)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vdd	DC Supply Voltage	–0.3	7.0	V	
Vin	Input Pin Voltage	–0.3	Vdd + 0.3	V	
Iin	Input Pin Current	–10.0	10.0	mA	25C
Tstrg	Storage Temperature	–55	150	C	
Tlead	Lead Temperature		300	C	10 sec

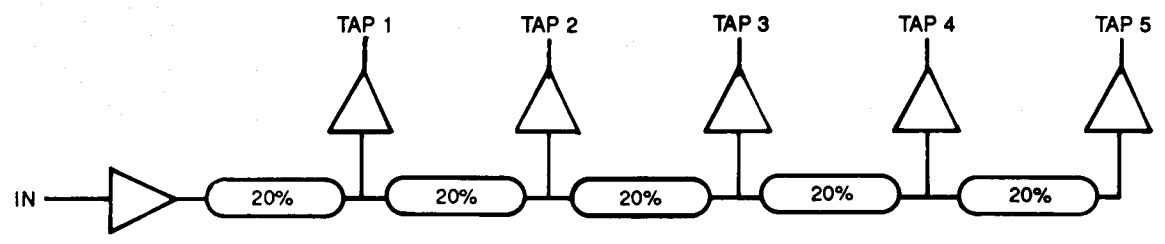
OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vdd	DC Supply Voltage	4.75	5.25	V	
*Idd	Static Supply		5	mA	
Vss	Circuit Ground	0.0	0.0	V	
Ta	Ambient Temperature	0.0	70.0	C	
Vih	High Level Input Voltage	2.0		V	
Vil	Low Level Input Voltage		0.8	V	
Ioh	High Level Output Current		–4.0	mA	Vcc=Min Voh=2.4
Iol	Low Level Output Current		4.0	mA	Vcc=Min Vol=0.4
I_I	Input Leakage Current	–1.0	1.0	µA	$0V \le V_I \le V_{DD}$
I_{IH}	High Level Input Current		10	µA	$V_I = V_{DD}$
I_{IL}	Low Level Input Current		–250	µA	$V_I = 0$

*I_{DD} (Dynamic) = C_{LD} (n) VF
Where: C_{LD} = Average capitance load/tap; n = # taps; V= V_{DD} max.; F = Frequency

Input Capacitance = 10.0 pf typical.
Output Load Capacitance = 25 pf Max.

SCHEMATIC DIAGRAM



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TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	1.5 X total delay
Period:	10 X total delay

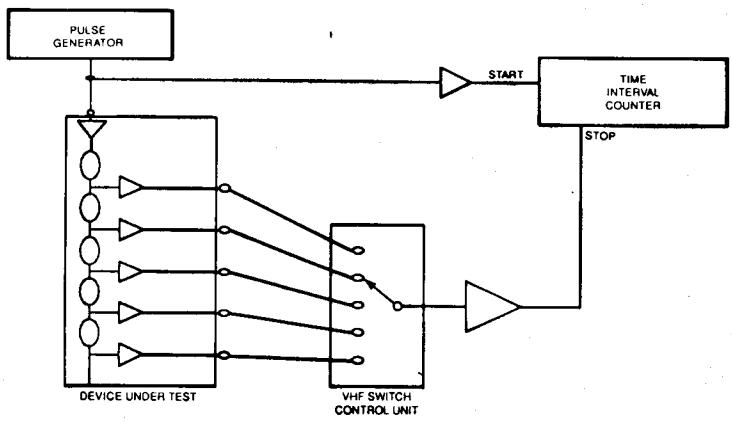
OUTPUT:

Each output is loaded with the equivalent of one 74F04 Input gate. Delay is measured at the 1.5V level on the rising and falling edge.

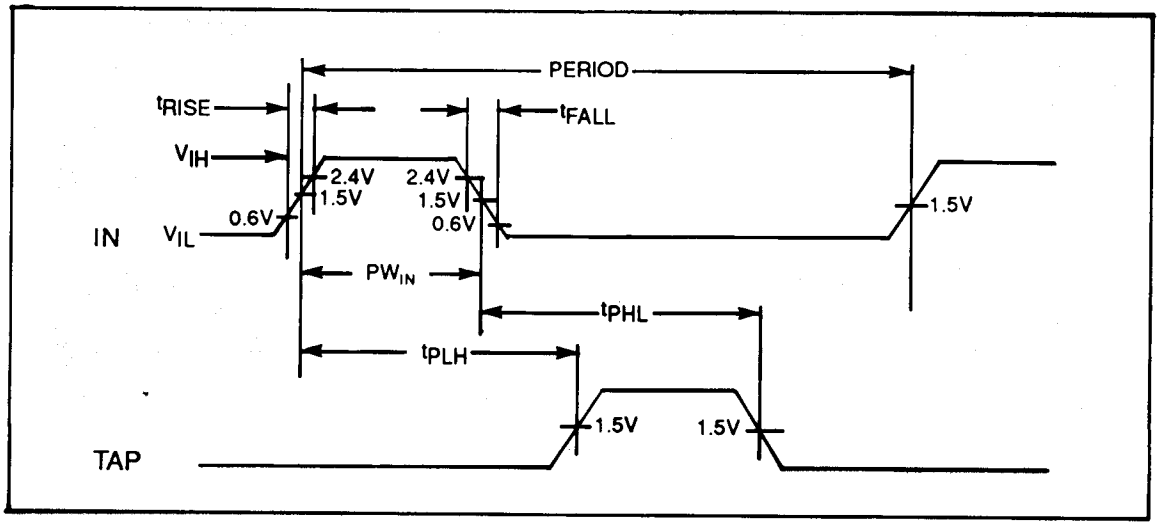
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TEST CIRCUIT



TIMING DIAGRAM



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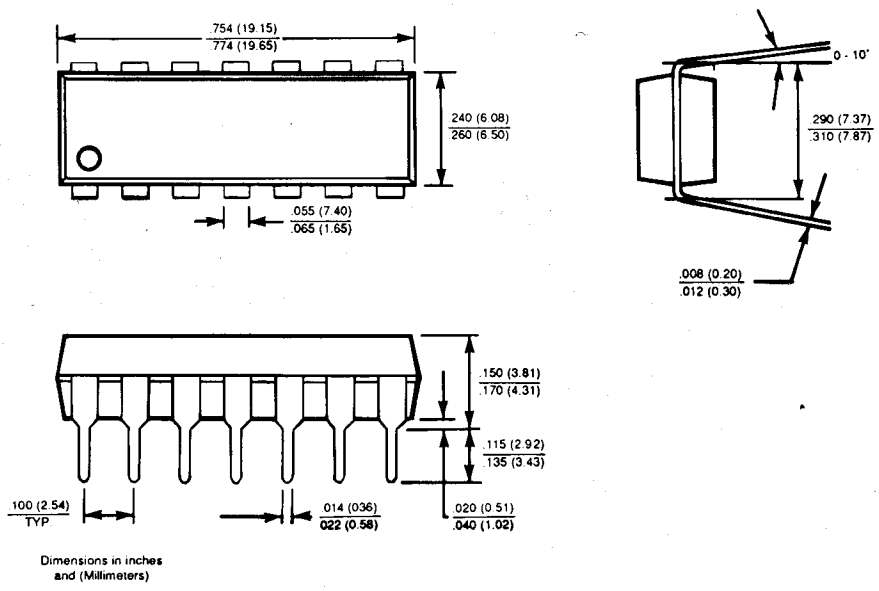
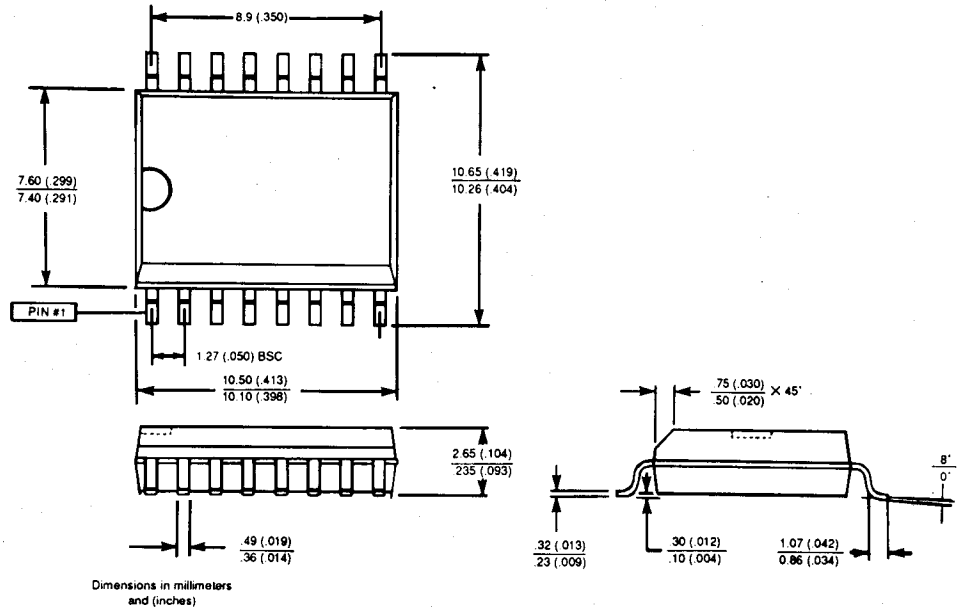
PACKAGES

14-PIN DIP (300 MIL)



Dimensions in inches
and (Millimeters)

16-PIN SOIC (300 MIL)



Dimensions in millimeters
and (inches)

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