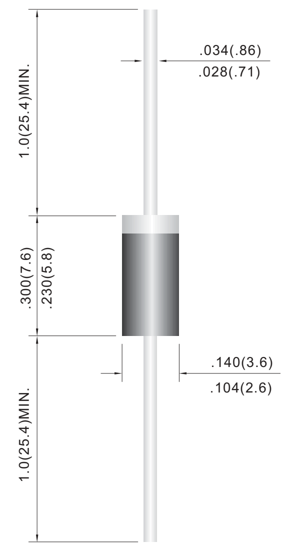
PANJIT SEMI CONDUCTOR

3EZ6.8~3EZ51

SILICON ZENER DIODES

VOLTAGE 6.8 to 51 Volts POWER 3.0 Watts

DO-15 Unit: inch(mm)



FEATURES

- Low profile package
- Built-in strain relief
- Low inductance
- Plastic package has Underwriters Laboratory Flammability Classification 94V-O
- High temperature soldering : 260°C /10 seconds at terminals
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: JEDEC DO-15, Molded plastic
- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: Color band denotes positive end (cathode)
- Standard packing: 52mm tape
- Weight: 0.014 ounce, 0.0397 gram

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbol	Value	Units
Peak Pulse Power Dissipation on T_L=50 °C (Notes A) Derate above 50 °C	P_D	3.0	W atts
Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC method)	I_{FSM}	15	Amps
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 to + 150	°C

NOTES:
A.Mounted on 5.0mm2 (.013mm thick) land areas.
B.Measured on8.3ms, and single half sine-wave or equivalent square wave ,duty cycle=4 pulses per minute maximum

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Part Number	Nominal Zener Voltage			Maximum Zener Impedance				Max Reverse Leakage Current		Marking Code
	V_Z @ I_{ZT}			Z_{ZT} @ I_{ZT}	I_{ZT}	Z_{ZK} @ I_{ZK}	I_{ZK}	I_R @ V_R		
	Nom. V	Min. V	Max. V	Ω	mA	Ω	mA	µA	V	
3.0 Watt ZENER										
3EZ6.8	6.8	6.46	7.14	2	110	700	1	5	4	3EZ6.8
3EZ7.5	7.5	7.13	7.88	2	100	700	0.5	5	5	3EZ7.5
3EZ8.2	8.2	7.79	8.61	2	91	700	0.5	5	6	3EZ8.2
3EZ8.7	8.7	8.27	9.14	2	85	700	0.5	4	6.6	3EZ8.7
3EZ9.1	9.1	8.65	9.56	3	82	700	0.5	3	7	3EZ9.1
3EZ10	10	9.5	10.5	4	75	700	0.25	3	7.6	3EZ10
3EZ11	11	10.45	11.55	4	68	700	0.25	1	8.4	3EZ11
3EZ12	12	11.4	12.6	5	63	700	0.25	1	9.1	3EZ12
3EZ13	13	12.35	13.65	5	58	700	0.25	0.5	9.9	3EZ13
3EZ14	14	13.3	14.7	5	53	700	0.25	0.5	10.6	3EZ14
3EZ15	15	14.25	15.75	6	50	700	0.25	0.5	11.4	3EZ15
3EZ16	16	15.2	16.8	6	47	700	0.25	0.5	12.2	3EZ16
3EZ17	17	16.15	17.85	6	44	750	0.25	0.5	13	3EZ17
3EZ18	18	17.1	18.9	6	42	750	0.25	0.5	13.7	3EZ18
3EZ19	19	18.05	19.95	7	40	750	0.25	0.5	14.4	3EZ19
3EZ20	20	19	21	7	37	750	0.25	0.5	15.2	3EZ20
3EZ22	22	20.9	23.1	8	34	750	0.25	0.5	16.7	3EZ22
3EZ24	24	22.8	25.2	9	31	750	0.25	0.5	18.2	3EZ24
3EZ25	25	23.75	26.25	10	30	750	0.25	0.5	19	3EZ25
3EZ27	27	25.65	28.35	10	28	750	0.25	0.5	20.6	3EZ27
3EZ28	28	26.6	29.4	12	27	750	0.25	0.5	21.3	3EZ28
3EZ30	30	28.5	31.5	16	25	1000	0.25	0.5	22.5	3EZ30
3EZ33	33	31.35	34.65	20	23	1000	0.25	0.5	25.1	3EZ33
3EZ36	36	34.2	37.8	22	21	1000	0.25	0.5	27.4	3EZ36
3EZ39	39	37.05	40.95	28	19	1000	0.25	0.5	29.7	3EZ39
3EZ43	43	40.85	45.15	33	17	1500	0.25	0.5	32.7	3EZ43
3EZ47	47	44.65	49.35	38	16	1500	0.25	0.5	35.8	3EZ47
3EZ51	51	48.45	53.55	45	15	1500	0.25	0.5	38.8	3EZ51

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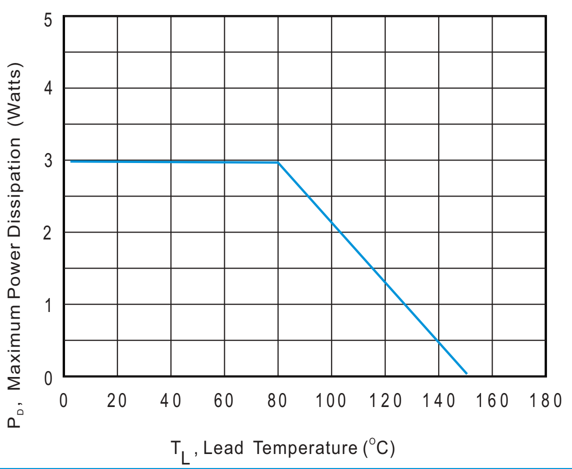

Fig.1 Power Temperature Derating Curve

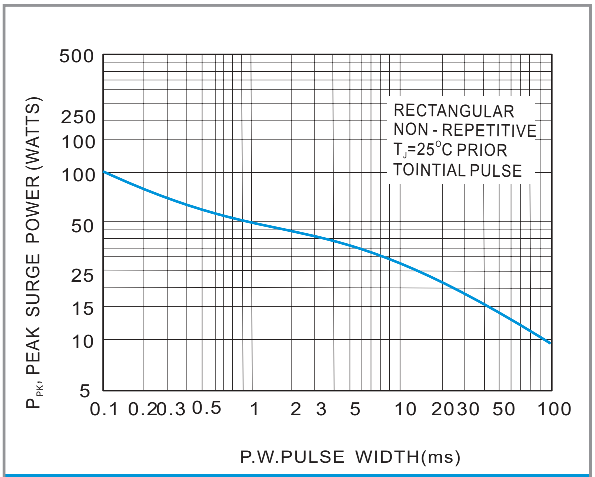

FIGURE 2. MAXIMUM SURGE POWER

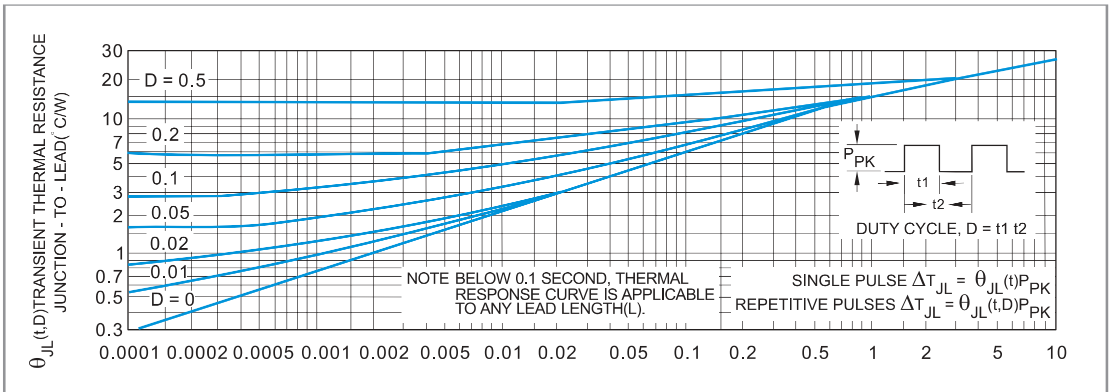

FIGURE 3. TYPICAL THERMAL RESPONSEL,

APPLICATION NOTE:

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determinejunction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = L_A P_D + T_A$$

L_A is the lead-to-ambient thermal resistance (°C/W) and Pd is the power dissipation. The value for L_A will vary and depends on the device mounting method. L_A is generally 30-40 °C/W for the various clips and tie points in common use and for printed circuit board wiring.

The temperature of the lead can also be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of TL, the junction temperature may be determined by:

$$T_J = T_L + \quad T_{JL}$$

T_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 3 for a train of power pulses or from Figure 10 for dc power.

$$T_{JL} = \quad J_L P_D$$

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of T_J(T_J) may be estimated. Changes in voltage, V_Z, can then be found from:

$$V = \quad V_Z \quad T_J$$

V_Z, the zener voltage temperature coefficient, is found from Figures 5 and 6.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 3 should not be used to compute surge capa-bility. Surge limitations are given in Figure 2. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 2 be exceeded.

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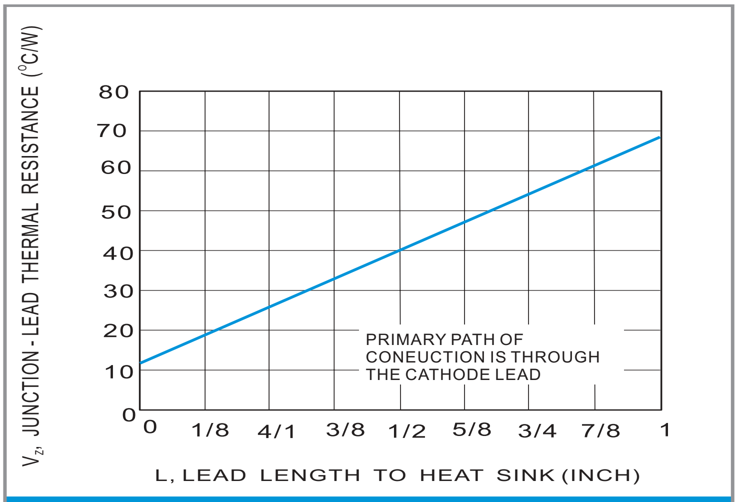

FIGURE 4. TYPLCAL THERMAL RESISTANCE