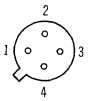
3N157,A (SILICON)
3N158,A

CASE 20
(TO-72)



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

P-channel silicon nitride passivated MOS field-effect enhancement mode transistors designed for chopper and switching application.

MAXIMUM RATINGS

Rating	Symbol	3N157 3N158	3N157A 3N158A	Unit
Drain-Source Voltage	V_{DS}	35	50	Vdc
Drain-Gate Voltage	V_{DG}	35	50	Vdc
Gate-Source Voltage	V_{GS}	50		Vdc
Drain Current	I_D	30		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.7		mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (I_D = -10 μAdc, V_G = V_S = 0)	3N157, 3N158 3N157A, 3N158A	$V_{(BR)DSS}$	35 50	- -	- -	Vdc
Gate Reverse Current (V_{GS} = +25 Vdc, V_{DS} = 0)		I_{GSS}	-	-	10	pAdc
Zero-Gate Voltage Drain Current (V_{DS} = -15 Vdc, V_{GS} = 0)	3N157, 3N158 3N157A, 3N158A	I_{DSS}	- -	- -	1.0 0.25	nAdc
(V_{DS} = -35 Vdc, V_{GS} = 0)	3N157, 3N158		-	-	10	μAdc
(V_{DS} = -50 Vdc, V_{GS} = 0)	3N157A, 3N158A		-	-	10	
Input Resistance (V_{GS} = -25 Vdc)		R_{GS}	-	$1 \times 10^{+12}$	-	Ohms
ON CHARACTERISTICS						
Gate-Source Threshold Voltage (V_{DS} = -15 Vdc, I_D = -10 μAdc)	3N157, 3N157A 3N158, 3N158A	$V_{GS(TH)}$	1.5 3.0	- -	3.2 5.0	Vdc
Gate-Source Voltage (V_{DS} = -15 Vdc, I_D = -0.5 mAdc)	3N157, 3N157A 3N158, 3N158A	V_{GS}	1.5 3.0	- -	5.5 7.0	Vdc
Gate Forward Current (V_{GS} = -25 Vdc, V_{DS} = 0)		$I_{G(f)}$	-	-	10	pAdc
(V_{GS} = -25 Vdc, V_{DS} = 0, T_A = +55°C)			-	-	10	nAdc
"ON" Drain Current (V_{DS} = -15 Vdc, V_{GS} = -10 Vdc)		$I_{D(on)}$	5.0	-	-	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)		$\lvert y_{fs} \rvert$	1000	-	4000	μmhos
(V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 kHz)			1800	-	-	
Output Admittance (V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)		$\lvert y_{os} \rvert$	-	-	60	μmhos
Input Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, f = 140 kHz)		C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, f = 140 kHz)		C_{rss}	-	-	1.3	pF
Drain-Substrate Capacitance ($V_{D(sub)}$ = -10 Vdc, f = 140 kHz)		$C_{d(sub)}$	-	-	4.0	pF
Noise Voltage (R_S = 0, BW = 1.0 Hz, V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 100 Hz)		e_n	-	300	-	$NV/\sqrt{Hz}$
(R_S = 0, BW = 1.0 Hz, V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)			-	120	500	

FIGURE 1 – FORWARD TRANSCONDUCTANCE

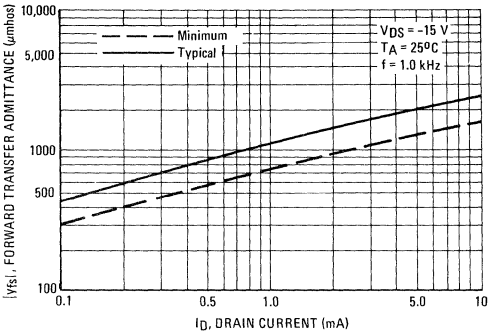


FIGURE 2 – OUTPUT TRANSCONDUCTANCE

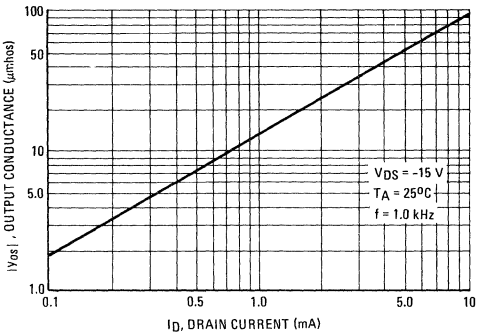


FIGURE 3 – FORWARD TRANSCONDUCTANCE versus TEMPERATURE

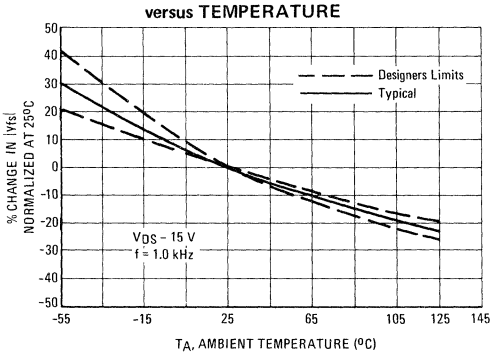


FIGURE 4 – BIAS CURVE

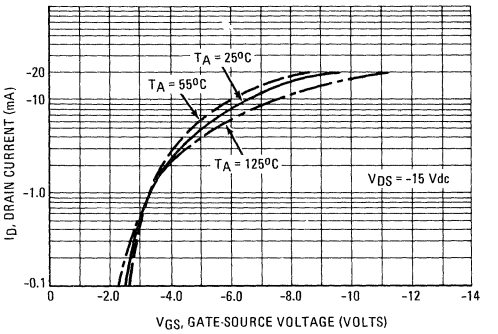


FIGURE 5 – "ON" DRAIN-SOURCE VOLTAGE

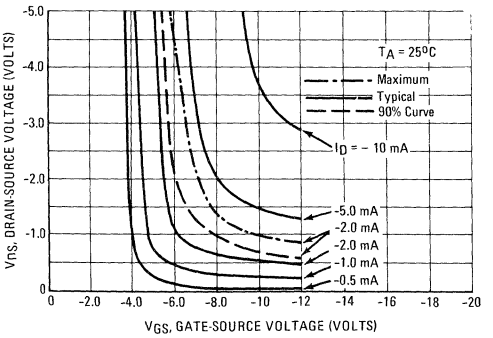
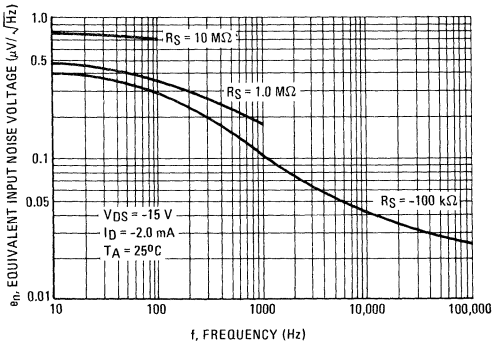


FIGURE 6 – EQUIVALENT INPUT NOISE VOLTAGE



SWITCHING CHARACTERISTICS

(T_A = 25°C)

FIGURE 7 – TURN-ON DELAY TIME

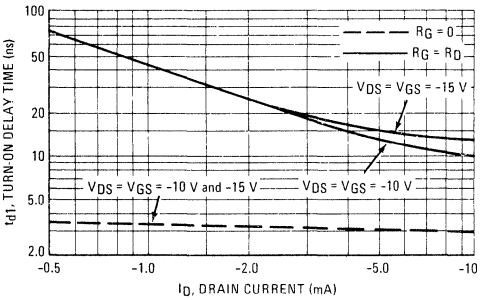


FIGURE 8 – RISE TIME

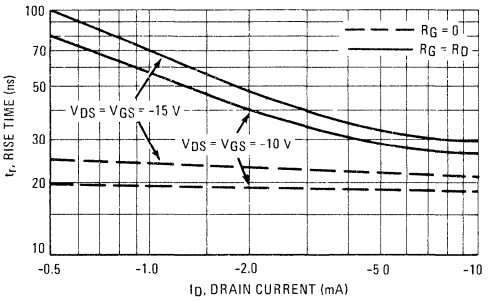


FIGURE 9 – TURN-OFF DELAY TIME

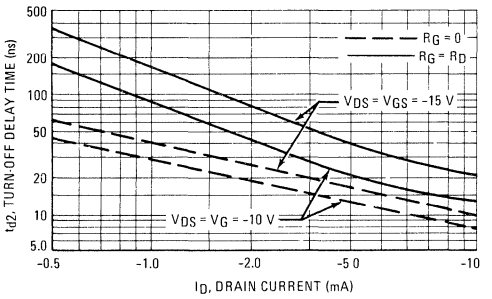


FIGURE 10 – FALL TIME

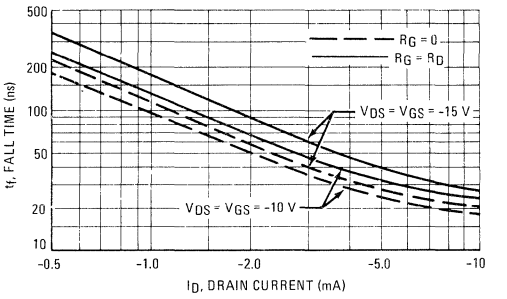
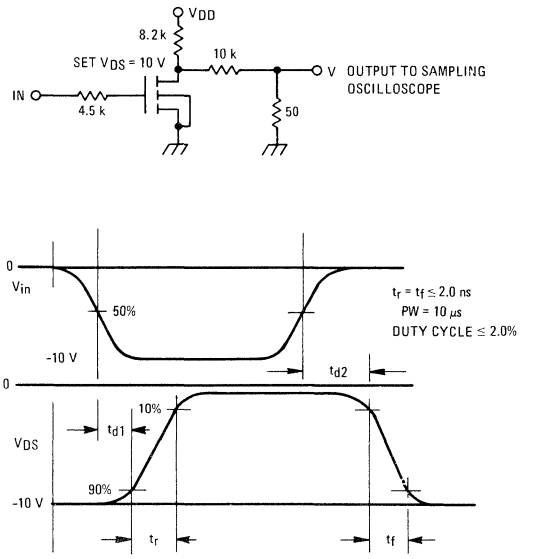


FIGURE 11 – SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 11. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_G (generator impedance) (Figure 12). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_G and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 5) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_G = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_G = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_G = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 12 – SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL