depletion-type n-channel dual gate MOSFETs *designed for . . .*

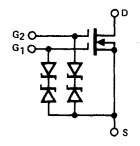
- **VHF Amplifiers**
- **Mixers**
- **IF Amplifiers**

Performance Curves MCB See Section 4

BENEFITS

- High Gain
  g_{fs} Typically 12 mmhos
- No Neutralization Required
  Low $C_{rss} < 0.03$ pF
- Automatic Gain Control with Second Gate

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Gate Voltage	30 V
Gate Current, Forward and Reverse	±10 mA
Drain-to-Source Voltage	25 V
Drain Current, Continuous	50 mA
Device Dissipation at T_{CASE} = 25°C	1.2 W
Device Dissipation at T_A = 25°C	360 mW
Free Air Temperature above 25°C	
Derate Linearly	2.2 mW/°C
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	3N201 Min	3N201 Typ	3N201 Max	3N202 Min	3N202 Typ	3N202 Max	3N203 Min	3N203 Typ	3N203 Max	Unit	Test Conditions	
1	STATIC	I_{G1SS} Gate One to Source Leakage Current			±10			±10			±10	nA	V_{G1S} = ±5 V, V_{G2S} = V_{DS} = 0	
2		I_{G2SS} Gate Two to Source Leakage Current			±10			±10			±10		V_{G2S} = ±5 V, V_{G1S} = V_{DS} = 0	
3		I_{G1SS} Gate One to Source Reverse Leakage Current			-10			-10			-10	µA	V_{G1S} = −5 V, V_{G2S} = V_{DS} = 0	
4		I_{G2SS} Gate Two to Source Reverse Leakage Current			-10			-10			-10		V_{G2S} = −5 V, V_{G1S} = V_{DS} = 0	T_A = 150°C
5		BV_{G1SS} Gate One to Source Breakdown Voltage	±6		±30	±6		±30	±6		±30	V	I_{G1} = ±10 mA, V_{G2S} = V_{DS} = 0	
6		BV_{G2SS} Gate Two to Source Breakdown Voltage	±6		±30	±6		±30	±6		±30		I_{G2} = ±10 mA, V_{G1S} = V_{DS} = 0	
7		BV_{DS} Drain to Source Breakdown Voltage	25			25			25				I_D = 10 µA, V_{G1S} = V_{G2S} = −5 V	
8		$V_{G1S(off)}$ Gate One to Source Cutoff Voltage	-0.5		-5	-0.5		-5	-0.5		-5		V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 20 µA	
9		$V_{G2S(off)}$ Gate Two to Source Cutoff Voltage	-0.2		-5	-0.2		-5	-0.2		-5		V_{DS} = 15 V, V_{G1S} = 0, I_D = 20 µA	
10		I_{DS} Zero Gate One Voltage Drain Current (Note 1)	6		30	6		30	3		15	mA	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0,	
11		g_{fs} Common-Source Forward Transconductance (Note 1)	8		20	8		20	7		15	mmho		f = 1 kHz
12	DYNAMIC	C_{iss} Common-Source Input Capacitance (Note 2)		6			6			6		pF	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 MHz
13		C_{rss} Common-Source Reverse Transfer Capacitance		0.02	0.03		0.02	0.03		0.02	0.03			
14		C_{oss} Common-Source Output Capacitance (Note 2)		2.5			2.5			2.5				
15	HIGH FREQUENCY	NF Common-Source Spot Noise Figure			4.5							dB	V_{DD} = 18 V, V_{GG} = 7 V, f = 200 MHz See Figure 1	
16		G_{ps} Small-Signal Common-Source Insertion Power Gain	15		25							dB		
17		BW Bandwidth	5		9							MHz		
18		$V_{GG(GC)}$ Gain-Control Gate-Supply Voltage	0		3							V	V_{DD} = 18 V, ΔG_{ps} = −30 dB, (Note 3), f = 200 MHz, See Figure 1	
19		$G_{ps(conv)}$ Small-Signal Conversion Power Gain				15		25				dB	V_{DD} = 18 V, f_{LO} = 245 MHz (Note 4), f_{RF} = 200 MHz, See Figure 2	
20		BW Bandwidth				4.5		7.5				MHz		
21		NF Common-Source Spot Noise Figure									6	dB	V_{DD} = 18 V, V_{GG} = 6 V, f = 45 MHz, See Figure 3	
22		G_{ps} Small-Signal Common-Source Insertion Power Gain							20		30	dB		
23		BW Bandwidth							3		6	MHz		
24		$V_{GG(GC)}$ Gain-Control Gate-Supply Voltage							0		-3	V	V_{DD} = 18 V, ΔG_{ps} = −30 dB, (Note 5), f = 45 MHz, See Figure 3	

*JEDEC registered data.

2. Non-JEDEC registered data.
3. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7 V.
4. Amplitude at input from local oscillator is 3V rms.
5. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6 V.

NOTES:
1. Pulse test pulsewidth = 300 µs, duty cycle ≈ 3%.

MCB

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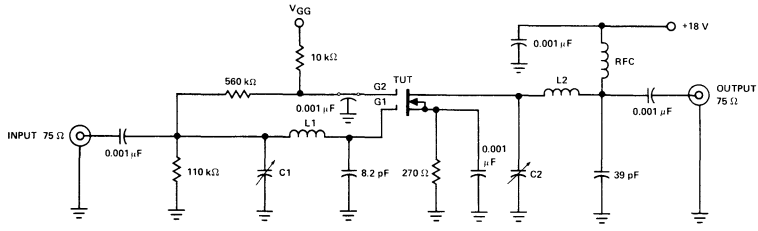
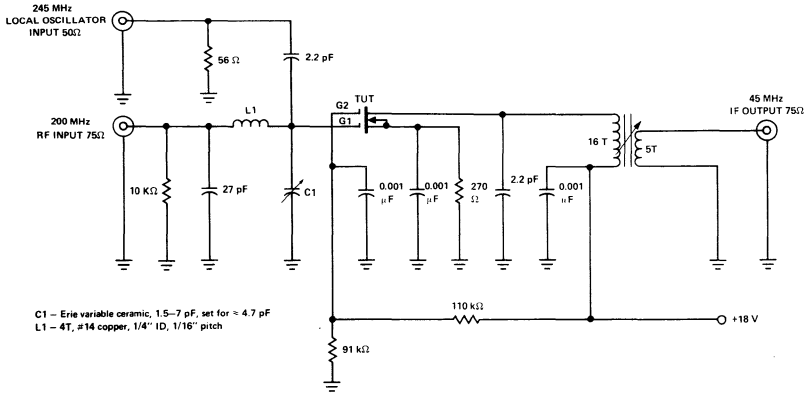
HIGH FREQUENCY TEST CIRCUITS



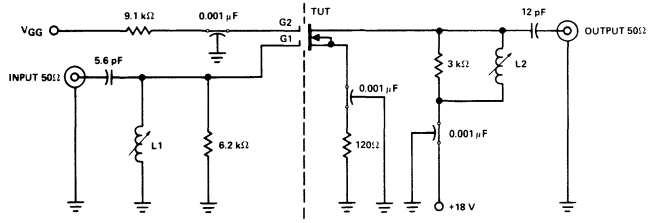
C1 – Erie variable ceramic, 4–30 pF, set for ≈ 22 pF
C2 – Erie variable ceramic, 4–30 pF, set for ≈ 10 pF
L1 – 4T, #14 copper, 1/4" ID, 1/6" pitch
L2 – 3T, #14 copper, 1/4" ID, 1/8" pitch
RFC – Delevan No. 153712 1μH

200 MHz Power Gain, Gain-Control Voltage and Noise Figure Test Circuit for 3N201
Figure 1



C1 – Erie variable ceramic, 1.5–7 pF, set for ≈ 4.7 pF
L1 – 4T, #14 copper, 1/4" ID, 1/16" pitch

200 MHz-to-45 MHz Circuit for Conversion Power Gain for 3N202
Figure 2



L1 – 14 T, #30 copper, close wound on 7/32" OD form with Arnold Engineering type "J" tuning core
L2 – 10 T, #30 copper, close-wound on 7/32" OD form with Arnold Engineering type "J" tuning core

45 MHz Power Gain, Gain-Control Voltage, and Noise Figure Test Circuit for 3N203
Figure 3

3