3N209 (SILICON)
3N210

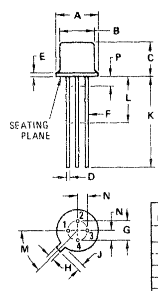
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

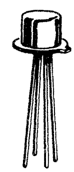
. . . depletion mode dual gate transistors designed and characterized for UHF communications applications

- Two Packages Offered–
  Hermetic Metal TO-72 – 3N209
  Micro-H Plastic – 3N210
- Silicon Nitride Passivation for Excellent Long Term Stability
- Zener Diode Protected Gates
- Third Order Intermodulation Distortion Curve Provided
- Common Source Power Gain –
  G_{ps} = 10 dB (Min) @ f = 500 MHz
- Noise Figure – 6.0 dB Max @ f = 500 MHz

N-CHANNEL DUAL GATE MOS FIELD-EFFECT TRANSISTORS

3N209





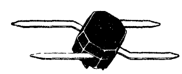
STYLE 9
PIN 1 DRAIN
2 GATE 2
3 GATE 1
4 SOURCE, SUBSTRATE AND CASE

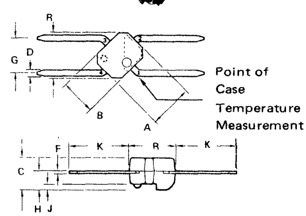
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

3N210





STYLE 1
PIN 1 SOURCE
2 DRAIN
3 GATE 2
4 GATE 1

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.95	5.21	0.195	0.205
B	3.94	4.19	0.155	0.165
C	2.67	2.92	0.105	0.115
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	4.06 BSC		0.160 BSC	
H	1.57	1.83	0.062	0.072
J	0.51	0.76	0.020	0.030
K	6.35	7.62	0.250	0.300
R	5.21	5.46	0.205	0.215

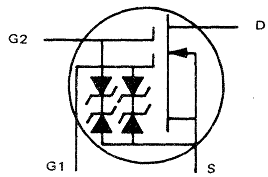
CASE 262-02

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
*Drain – Source Voltage	V_{DS}	25		Vdc
*Drain Gate Voltage	V_{DG1} V_{DG2}	30 30		Vdc Vdc
Gate Current	I_{G1R} I_{G1F} I_{G2R} I_{G2F}	-10 10 -10 10		mAdc mAdc mAdc mAdc
*Drain Current – Continuous	I_D	30		mAdc
		3N209	3N210	
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	350 2.80	mW mW/°C
*Storage Channel Temperature Range	T_{stg}	-65 to +200	-65 to +175	°C
*Operating Channel Temperature	$T_{channel}$	200	150	°C
*Lead Temperature, 1/16″ From Seated Surface for 10 Seconds		260	260	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – MOS FET CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) Substrate Connected to Source

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{G1S} = -4.0 Vdc, V_{G2S} = 4.0 Vdc)	$V_{(BR)DS}$	25	–	–	Vdc
Gate 1 – Source Forward Breakdown Voltage (I_{G1} = 10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SSF}$	7.0	–	22	Vdc
Gate 1 – Source Reverse Breakdown Voltage (I_{G1} = -10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SSR}$	-7.0	–	-22	Vdc
Gate 2 – Source Forward Breakdown Voltage (I_{G2} = 10 mAdc V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SSF}$	7.0	–	22	Vdc
Gate 2 – Source Reverse Breakdown Voltage (I_{G2} = -10 mAdc V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SSR}$	-7.0	–	-22	Vdc
Gate 1 – Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 50 μAdc)	$V_{G1S(off)}$	-0.1	–	-4.0	Vdc
Gate 2 – Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0 Vdc, I_D = 50 μAdc)	$V_{G2S(off)}$	-0.1	–	-4.0	Vdc
Gate 1 – Terminal Forward Current (V_{G1S} = 6.0 Vdc, V_{G2S} = V_{DS} = 0)	I_{G1SSF}	–	–	20	nAdc
Gate 1 – Terminal Reverse Current (V_{G1S} = -6.0 Vdc, V_{G2S} = V_{DS} = 0) (V_{G1S} = -6.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)	I_{G1SSR}	– –	– –	-20 -10	nAdc μAdc
Gate 2 – Terminal Forward Current (V_{G2S} = 6.0 Vdc, V_{G1S} = V_{DS} = 0)	I_{G2SSF}	–	–	20	nAdc
Gate 2 – Terminal Reverse Current (V_{G2S} = -6.0 Vdc, V_{G1S} = V_{DS} = 0) (V_{G2S} = -6.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)	I_{G2SSR}	– –	– –	-20 -10	nAdc μAdc
***ON CHARACTERISTICS**					
Gate 1 – Zero Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	5.0	–	30	mAdc
SMALL SIGNAL CHARACTERISTICS					
*Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	y_{fs}	10	13	20	mmhos
*Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geq$ 5.0 mAdc, f = 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
*Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geq$ 5.0 mAdc, f = 1.0 MHz)	C_{rss}	0.005	0.023	0.03	pF
*Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geq$ 5.0 mAdc, f = 1.0 MHz)	C_{oss}	0.5	2.0	4.0	pF
*Common-Source Noise Figure (Figure 12) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	NF	–	4.5	6.0	dB
*Common-Source Power Gain (Figure 12) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	G_{ps}	10	13	20	dB
Bandwidth (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	BW	7.0	–	17	MHz

*Indicates JEDEC Registered Data.

TYPICAL SCATTERING PARAMETERS

FIGURE 2 – S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

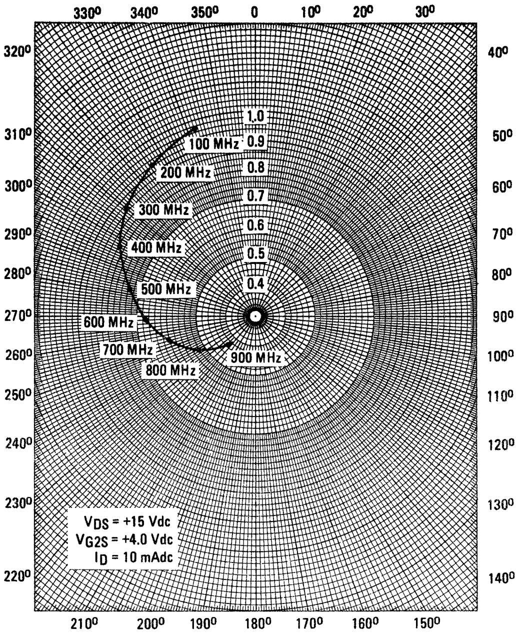


FIGURE 3 – S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

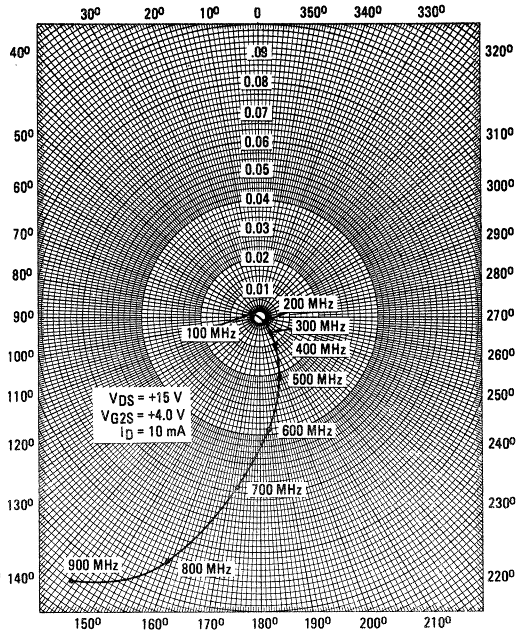


FIGURE 4 – S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

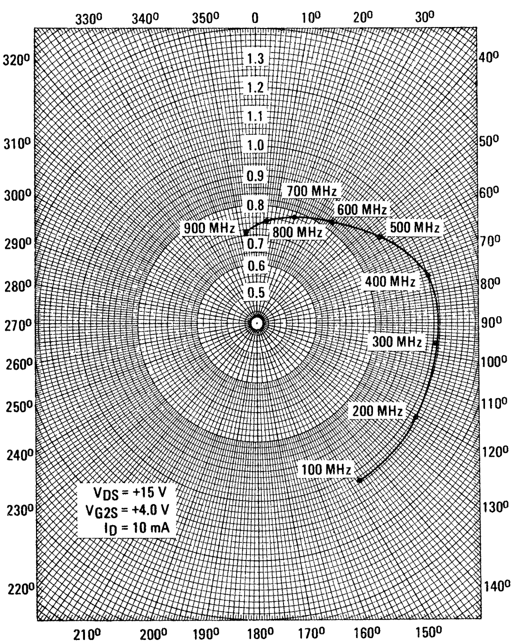
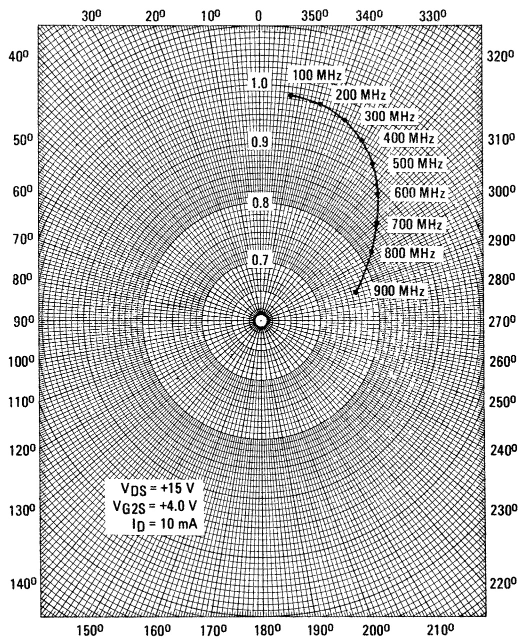


FIGURE 5 – S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY



TYPICAL COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{GS2} = 4.0 Vdc, I_D = 10 mAdc)

FIGURE 6 – Y_{11}, INPUT ADMITTANCE versus FREQUENCY

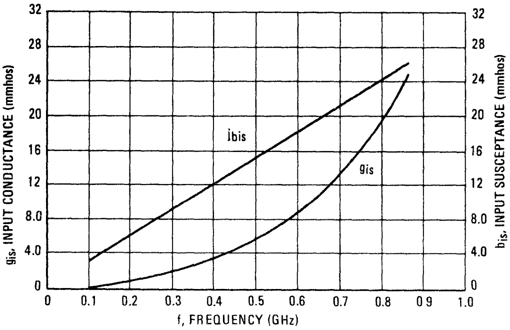


FIGURE 7 – Y_{12}, REVERSE TRANSFER ADMITTANCE versus FREQUENCY

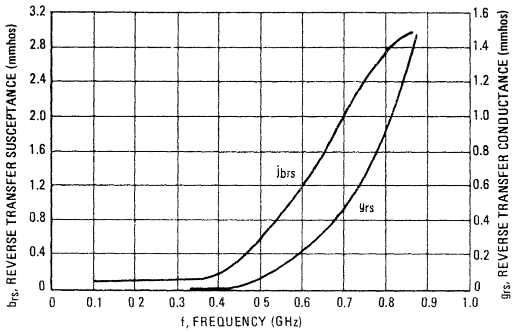


FIGURE 8 – Y_{21}, FORWARD TRANSFER ADMITTANCE versus FREQUENCY

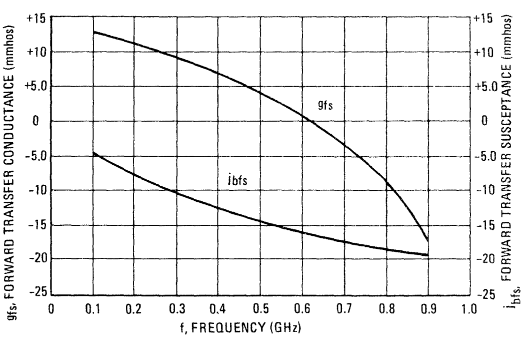
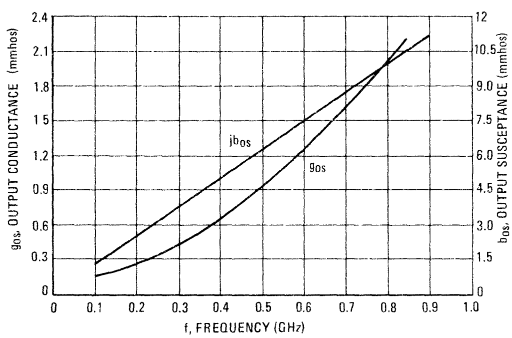


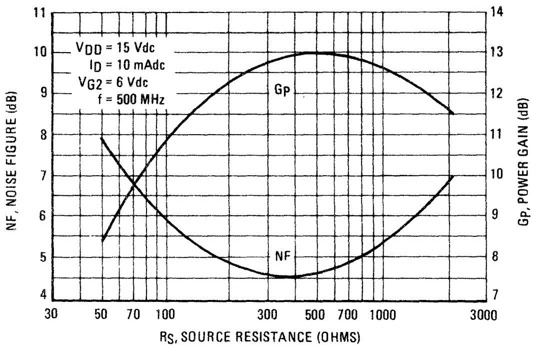
FIGURE 9 – Y_{22}, OUTPUT ADMITTANCE versus FREQUENCY



The S and Y Parameters were Measured with a Hewlett Packard HP8542A Network Analyzer.

FIGURE 10 – POWER GAIN AND NOISE FIGURE versus SOURCE RESISTANCE

(See Schematic Figure 12)



The Test Circuit shown in Figure 12 was used to generate Power Gain and Noise Figure as a function of Source Resistance curves.

FIGURE 11 – THIRD ORDER INTERMODULATION DISTORTION

(See Schematic Figure 12)

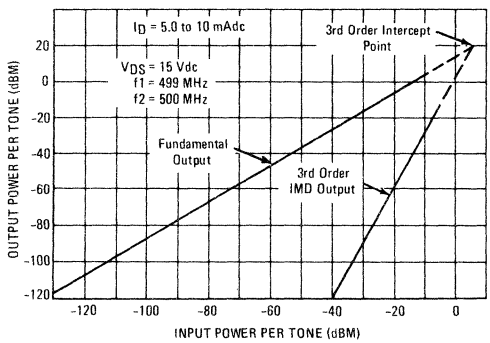
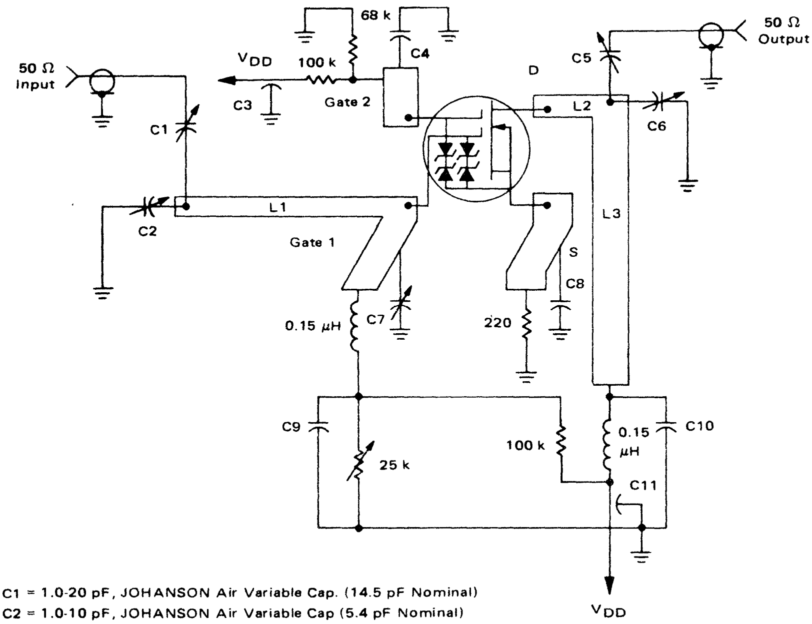


Figure 11 shows the typical third order intermodulation distortion (IMD) performance of the 3N209 and 3N210 at 500 MHz.

Both fundamental output and third order IMD output characteristics are plotted. The curves have been extrapolated to show the third order intermodulation output intercept point.

The performance is typical for I_D between 5.0 mAdc and 10 mAdc. The test circuit shown in Figure 12 was used to generate the IMD Data.

FIGURE 12 – TEST CIRCUIT FOR POWER GAIN, NOISE FIGURE AND THIRD ORDER INTERMODULATION DISTORTION



C1 = 1.0-20 pF, JOHANSON Air Variable Cap. (14.5 pF Nominal)
C2 = 1.0-10 pF, JOHANSON Air Variable Cap (5.4 pF Nominal)
C3, C11 = 470 pF, Low Inductance Feedthru Cap.
C4, C8, C9, C10 = 250 pF, Low Inductance, UNDERWOOD Cap. (J-101)
C5 = 0.4-6.0 pF, JOHANSON Air Variable Cap. (0.92 pF Nominal)
C6 = 1.0-10 pF, JOHANSON Air Variable Cap. (5.9 pF Nominal)
C7 = 1.0-10 pF, JOHANSON Air Variable Cap (3.0 pF Nominal)
L1 = 2.52 x 0.1 inches
L2 = 0.4 x 0.1 inches
L3 = 1.23 x 0.2 inches
} On 2 sided glass Teflon®, 1 oz. copper clad, 1/16″ $\epsilon_R = 2.55$

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