

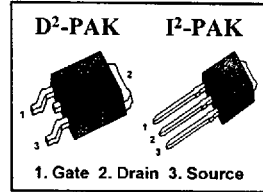
**FEATURES**

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25  $\mu$ A (Max.) @  $V_{DS} = 900V$
- Low  $R_{DS(ON)}$  : 4.679  $\Omega$  (Typ.)

$$BV_{DSS} = 900 V$$

$$R_{DS(on)} = 6.2 \Omega$$

$$I_D = 3 A$$



**Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	900	V
$I_D$	Continuous Drain Current ( $T_c=25^\circ C$ )	3	A
	Continuous Drain Current ( $T_c=100^\circ C$ )	1.9	
$I_{DM}$	Drain Current-Pulsed ①	12	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	286	mJ
$I_{AR}$	Avalanche Current ①	3	A
$E_{AR}$	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ )*	3.1	W
	Total Power Dissipation ( $T_c=25^\circ C$ )	100	W
	Linear Derating Factor	0.8	W/°C
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	°C
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

**Thermal Resistance**

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.25	°C/W
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount).



Electrical Characteristics ( $T_C=25\text{ }^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	900	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	1.13	--	V/°C	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	--	--	-100	nA	$V_{GS}=-30V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=900V$
		--	--	250		$V_{DS}=720V, T_C=125\text{ }^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	6.2	$\Omega$	$V_{GS}=10V, I_D=1.5A$ ④*
$g_{fs}$	Forward Transconductance	--	2.19	--	$\bar{\Omega}$	$V_{DS}=50V, I_D=1.5A$ ④
$C_{iss}$	Input Capacitance	--	590	770	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
$C_{oss}$	Output Capacitance	--	55	65		
$C_{rss}$	Reverse Transfer Capacitance	--	22	28		
$t_{d(on)}$	Turn-On Delay Time	--	16	40	ns	$V_{DD}=450V, I_D=3A,$ $R_G=16\Omega$ See Fig 13 ④ ⑤
$t_r$	Rise Time	--	26	60		
$t_{d(off)}$	Turn-Off Delay Time	--	47	105		
$t_f$	Fall Time	--	24	60		
$Q_g$	Total Gate Charge	--	28	37	nC	$V_{DS}=720V, V_{GS}=10V,$ $I_D=3A$ See Fig 6 & Fig 12 ④ ⑤
$Q_{gs}$	Gate-Source Charge	--	5.5	--		
$Q_{gd}$	Gate-Drain( "Miller" ) Charge	--	11.9	--		

## Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	3	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	12		
$V_{SD}$	Diode Forward Voltage ③	--	--	1.4	V	$T_J=25\text{ }^\circ\text{C}, I_S=3A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	380	--	ns	$T_J=25\text{ }^\circ\text{C}, I_F=3A$
$Q_{rr}$	Reverse Recovery Charge	--	1.9	--	$\mu C$	$di_F/dt=100A/\mu s$ ④

## Notes ;

- Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- $L=60\text{mH}, I_{AS}=3A, V_{DD}=50V, R_G=27\Omega,$  Starting  $T_J=25\text{ }^\circ\text{C}$
- $I_{SD} \leq 3A, di/dt \leq 90A/\mu s, V_{DD} \leq BV_{DSS},$  Starting  $T_J=25\text{ }^\circ\text{C}$
- Pulse Test : Pulse Width =  $250\mu s,$  Duty Cycle  $\leq 2\%$
- Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

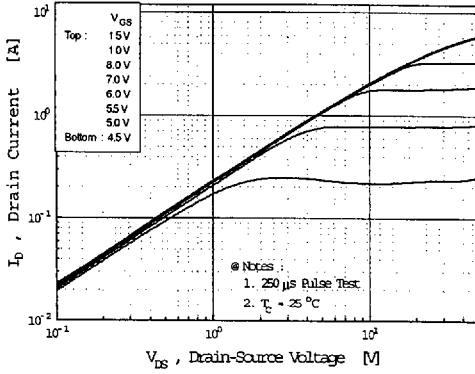


Fig 2. Transfer Characteristics

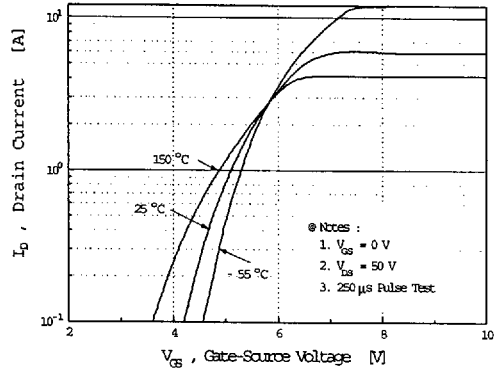


Fig 3. On-Resistance vs. Drain Current

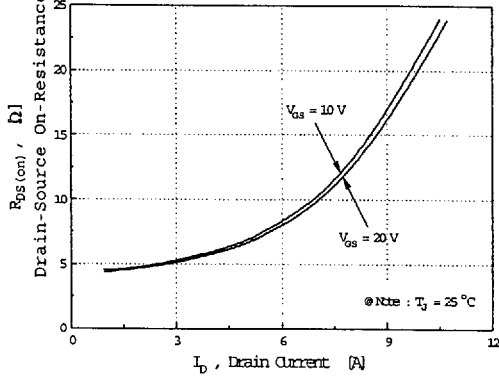


Fig 4. Source-Drain Diode Forward Voltage

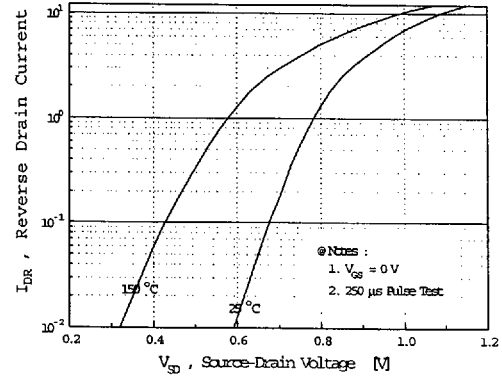


Fig 5. Capacitance vs. Drain-Source Voltage

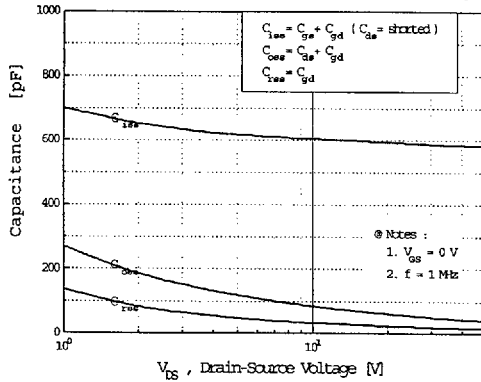
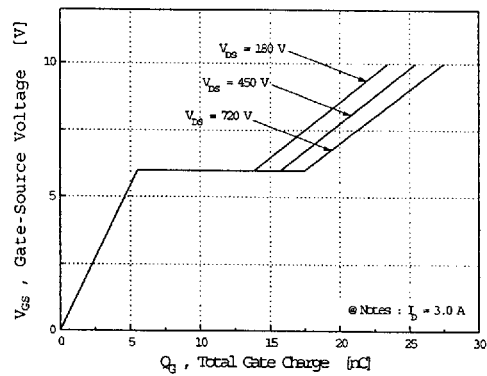


Fig 6. Gate Charge vs. Gate-Source Voltage



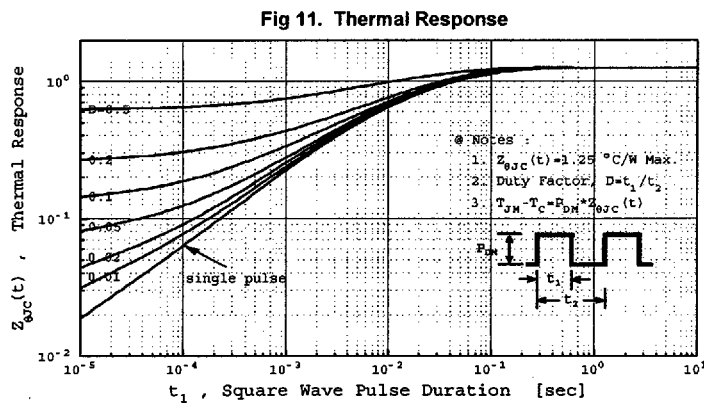
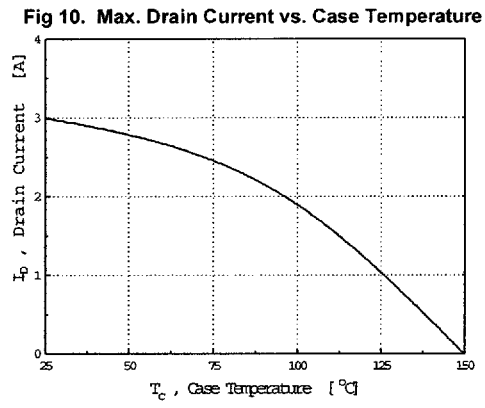
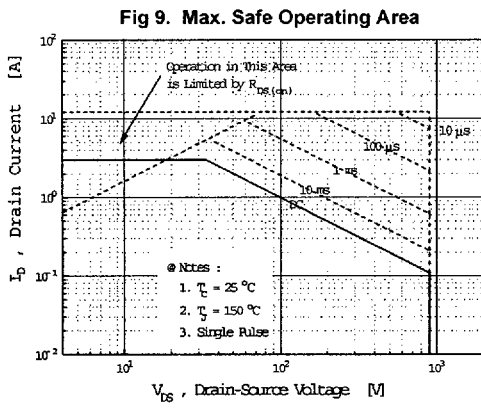
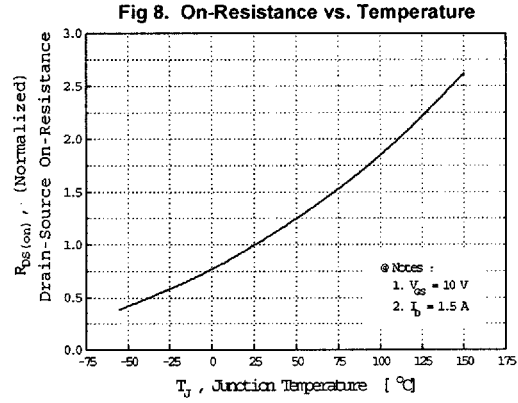
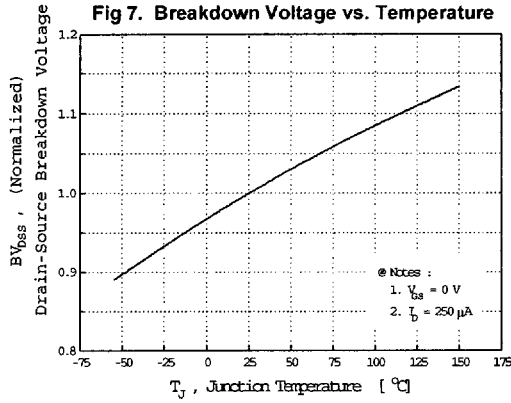


Fig 12. Gate Charge Test Circuit & Waveform

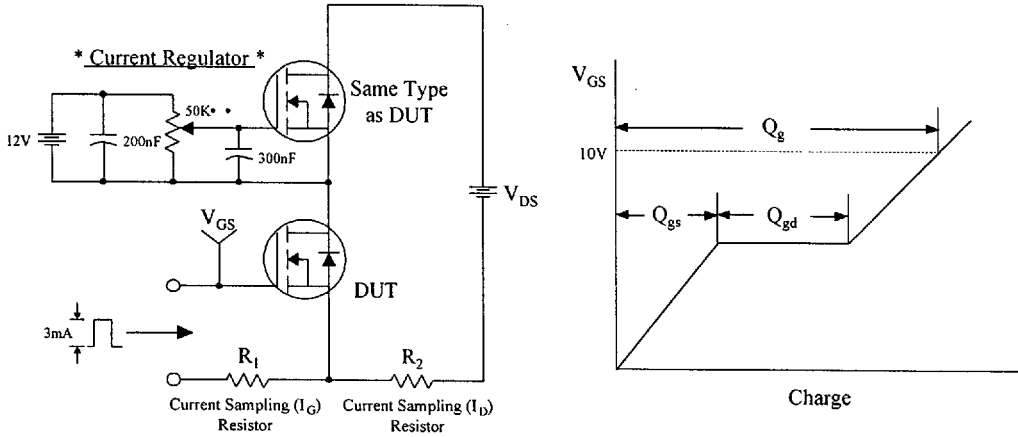


Fig 13. Resistive Switching Test Circuit & Waveforms

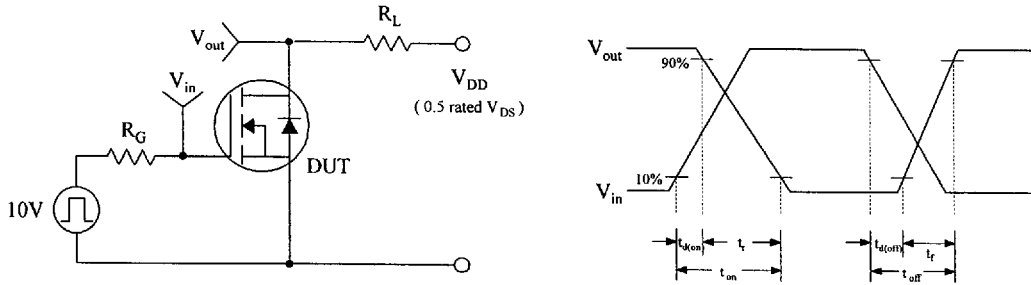


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

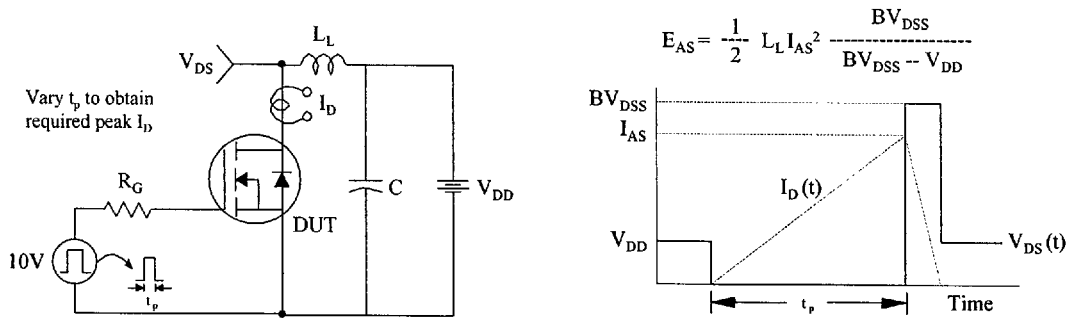


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

