Complete 10-Bit, 50MSPS, CMOS Analog-to-Digital Converter

FEATURES

- CMOS 10-Bit, 50 MSPS Sampling A/D Converter
- Configurable Input: Single-Ended or Differential
- Differential Nonlinearity: 0.3 LSB
- Three State Outputs
- Out of Range Indicator
- Built In Clamp Function (DC Restore)
- Adjustable On Chip Voltage Reference
- IF Under sampling to 135 MHz
- Power Dissipation: 84 mW (3 V Supply)
- Power Down (Sleep) Mode: 10 μW
- Operation Between +2.7 V and +5.5V Supply
- Green, 28-Lead TSSOP Package
- Pin Compatible with THS1030, AD9200 and AD876 Family

PRODUCT HIGHLIGHTS

- **Low Power:** The 3PA1030 speed is 50MSPS but only consumes 84 mW on a 3 V supply. In sleep mode, power is reduced to 10 μW.
- **Pin Compatible with THS1030/TLC876/AD9200/AD876:** The 3PA1030 allows older designs to migrate to higher speed and lower supply voltages.
- **100 MHz On-board Sample-and-Hold:** The versatile SHA input can be configured for either single ended or differential inputs.
- **Out-of-Range Indicator:** The OTR output bit indicates when the input signal is beyond the 3PA1030's input range.
- **Built-In Clamp Function:** Allows dc restoration of video signals.

PRODUCT DESCRIPTION

The 3PA1030 is a monolithic, single supply, 10-Bit, 50 MSPS analog-to-digital converter with an on-chip sample-and-hold amplifier and voltage reference. The 3PA1030 uses multi-stage differential pipeline architecture at 50 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The input of the 3PA1030 has been designed to ease the development of both imaging and communications systems. The user can select a variety of input ranges and offsets and can drive the input either single-ended or differentially.

The sample and hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single channel inputs at frequencies up to and beyond the Nyquist rate. AC coupled input signals can be shifted to a predetermined level, with an on-board 3PEAK proprietary clamp circuit. The dynamic performance is excellent.

The 3PA1030 has an onboard programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

The 3PA1030 can operate with a supply ranging from +2.7 V to +5.5 V, ideally suiting it for low power operation in high speed applications.

The 3PA1030 is specified over the industrial (–40°C to +85°C) temperature range.

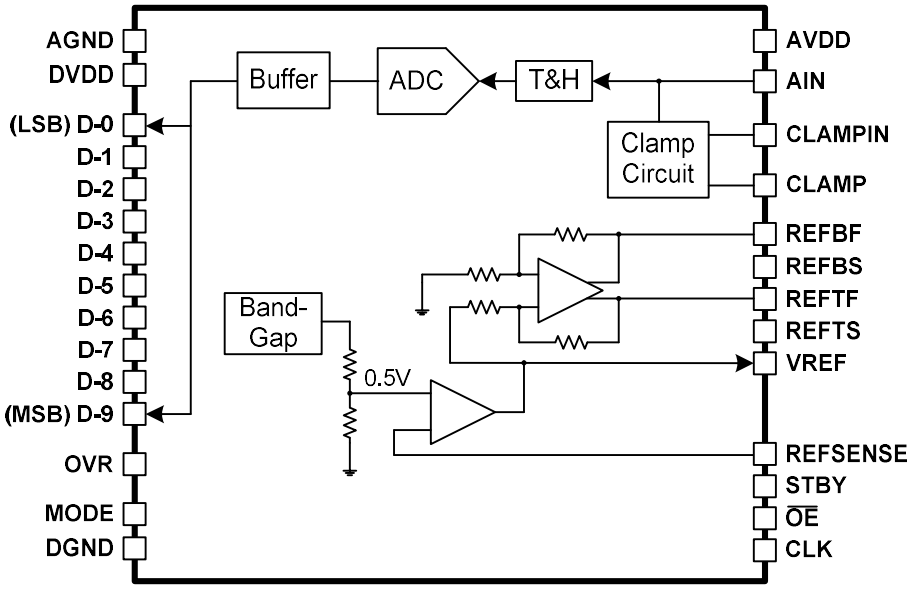


Figure 1. Functional Block Diagram

PIN CONFIGURATION

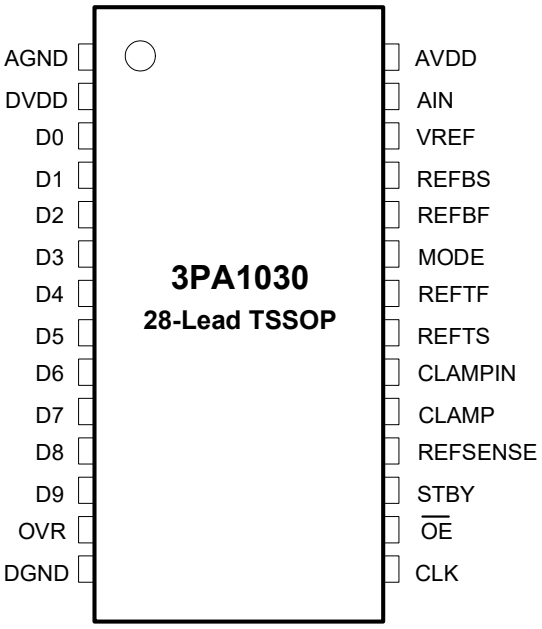


Figure 2. Pin Location

TSSOP Pin. No.	Name	Description
1	AGND	Analog Ground
2	DVDD	Digital Driver Supply
3	D0	Bit 0
4	D1	Bit 1
5	D2	Bit 2
6	D3	Bit 3
7	D4	Bit 4
8	D5	Bit 5
9	D6	Bit 6
10	D7	Bit 7
11	D8	Bit 8
12	D9	Bit 9 Most Significant Bit
13	OVR	Out of Range Indicator
14	DGND	Digital Ground
15	CLK	Clock Input
16	OE	HI: High Impedance State. LO: Normal Operation
17	STBY	HI: Power Down Mode. LO: Normal Operation
18	REFSENSE	Reference Select
19	CLAMP	HI: Enable Clamp Mode. LO: No Clamp
20	CLAMPIN	Clamp Reference Input
21	REFTS	Top reference
22	REFTF	Top Reference Decoupling
23	MODE	Mode select
24	REFBF	Bottom Reference Decoupling
25	REFBS	Bottom reference
26	VREF	Internal Reference Output
27	AIN	Analog Input
28	AVDD	Analog Supply

ORDERING GUIDE

Model	Temperature Range	Package	Transport Media, Quantity
3PA1030	–40°C to+85°C	28-Lead TSSOP	Tape and Reel, 2500

ABSOLUTE MAXIMUM RATINGS *

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	6.5	V
DRVDD	DRVSS	–0.3	6.5	V
AVSS	DRVSS	–0.3	0.3	V
AVDD	DRVDD	–6.5	6.5	V
MODE	AVSS	–0.3	AVDD+0.3	V
CLK	AVSS	–0.3	AVDD+0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD+0.3	V
AIN	AVSS	–0.3	AVDD+0.3	V
VREF	AVSS	–0.3	AVDD+0.3	V
REFSENSE	AVSS	–0.3	AVDD+0.3	V

REFTF,REFTB	AVSS	–0.3	AVDD+0.3	V
REFTS,REFBS	AVSS	–0.3	AVDD+0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	150	°C
Lead Temperature10sec			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS

AVDD = +3 V, DRVDD = +3 V, F_S = 50 MHz (50% Duty Cycle), 2 V Input Span from 0 V to 2 V, Internal Reference, T_{MIN} to T_{MAX} Unless Otherwise Noted)

Parameter	Symbol	Condition	Rating			Units
			Min	Typ	Max	
RESOLUTION				10		Bits
CONVERSION RATE	F_S			50		MHz
DC ACCURACY						
Differential Nonlinearity	DNL			±0.3	±1.0	LSB
Integral Nonlinearity	INL			±0.9	±2.0	LSB
Offset Error	E_{ZS}			±0.2	±1.2	%FSR
Gain Error	E_{FS}			±1.6	±5.0	%FSR
REFERENCE VOLTAGES						
Top Reference Voltage	REFTS		0.75		1.5	V
Bottom Reference Voltage	REFBS		0.25		0.5	V
Differential Reference Voltage			1		2	V p-p
Reference Input Resistance		REFSENSE = AVDD		10		kΩ
		Between REFTF & REFBF		1		kΩ
ANALOG INPUT						
Input Voltage Range	AIN		0		2*(REFT-REFB)	V
Input Capacitance	C_{IN}	Switched		2		pF
Aperture Delay	t_{AP}			4		ns
Aperture Uncertainty (Jitter)	t_{AJ}			2		ps
Input Bandwidth (–3 dB)	BW			300		MHz
DC Leakage Current		V_{IN} > 80mV		5		μA
INTERNAL REFERENCE						
Output Voltage (1 V Mode)	VREF	REFSENSE = VREF		0.5		V
Output Voltage Tolerance (1 V Mode)				±10	±25	mV
Output Voltage (2 V Mode)	VREF	REFSENSE = GND		1		V
POWER SUPPLY						
Operating Voltage	AVDD		2.7		5.5	V
	DRVDD		2.7		5.5	V
Supply Current	IAVDD			28		mA
Power Consumption	P_D	AVDD = 3 V,		84		mW
Power-Down		AVDD = DVDD = 3 V, CLOCK = AVSS, STBY = AVDD		10		μW
Gain Error Power Supply Rejection	PSRR			1		% FS

Parameter	Symbol	Condition	Rating			Units
DYNAMIC PERFORMANCE (AIN = 0.5 dBFS)						
Signal-to-Noise and Distortion	SINAD	f = 3.58 MHz	52.5	56.5		dB
		f = 16 MHz		48.6		dB
Effective Bits		f = 3.58 MHz	8.4	9		Bits
		f = 16 MHz		7.8		Bits
Signal-to-Noise	SNR	f = 3.58 MHz	53	57.5		dB
		f = 16 MHz		53.1		dB
Total Harmonic Distortion	THD	f = 3.58 MHz		–60	–56	dB
		f = 16 MHz		–58		dB
Spurious Free Dynamic Range	SFDR	f = 3.58 MHz		–66	–56	dB
		f = 16 MHz		–61		dB
Differential Phase	DP	NTSC 40 IRE Mod Ramp		0.2		Degree
Differential Gain	DG			0.08		%
DIGITAL INPUTS						
High Input Voltage	V_{IH}		2.4			V
Low Input Voltage	V_{IL}				0.3	V
DIGITAL OUTPUTS						
High-Z Leakage	I_{OZ}	Output = GND to V_{DD}	–10		10	µA
Data Valid Delay	t_{OD}	C_L = 20 pF		25		ns
Data Enable Delay	t_{DEN}			25		ns
Data High-Z Delay	t_{DHZ}			13		ns
CLOCKING						
Clock Pulse-width High	t_{CH}		9.5			ns
Clock Pulse-width Low	t_{CL}		9.5			ns
Pipeline Latency				3		Cycles
CLAMP						
Clamp Error Voltage	E_{OC}	CLAMPIN = +0.5V to +2.0V, R_{IN} = 10 Ω		±60	±80	mV
Clamp Pulse-width	t_{CPW}	C_{IN} = 1 µF (Period = 63.5 µs)		2		µs

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
Integral nonlinearity refers to the deviation of each individual code from a line drawn from “zero” through “full scale.” The point used as “zero” occurs 1/2 LSB before the first code transition. “Full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

Offset Error
Transition should occur at a level 1 LSB above “zero.” Offset is defined as the deviation of the actual first code transition from that point.

Gain Error
The first code transition should occur for an analog value 1 LSB above nominal negative full scale. The last transition should occur for an analog value 1 LSB below the nominal positive full scale. Gain Error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every rising edge.

TYPICAL CHARACTERIZATION CURVES

AVDD = +3 V, DRVDD = +3 V, F_S = 32 MHz (50% Duty Cycle), MODE = AVDD, 2 V Input Span from 0.5 V to 2.5 V, External Reference, Unless Otherwise Noted.

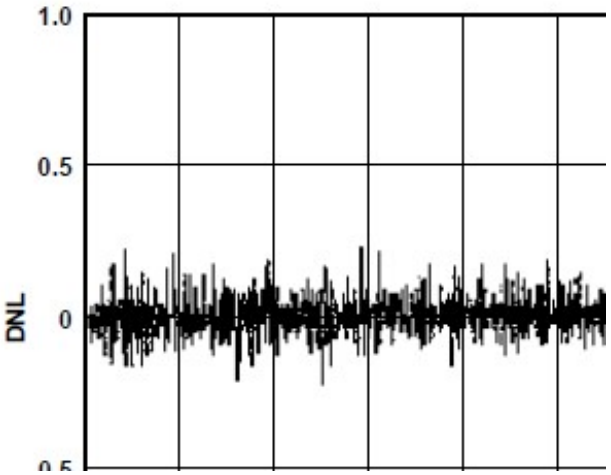


Figure 3. Typical DNL

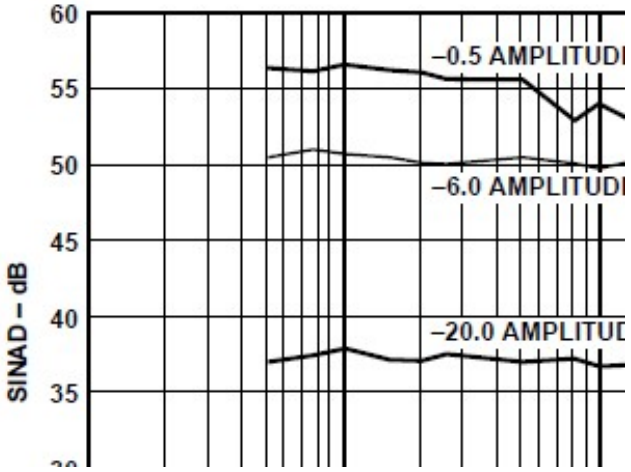


Figure 6. SINAD vs. Input Frequency

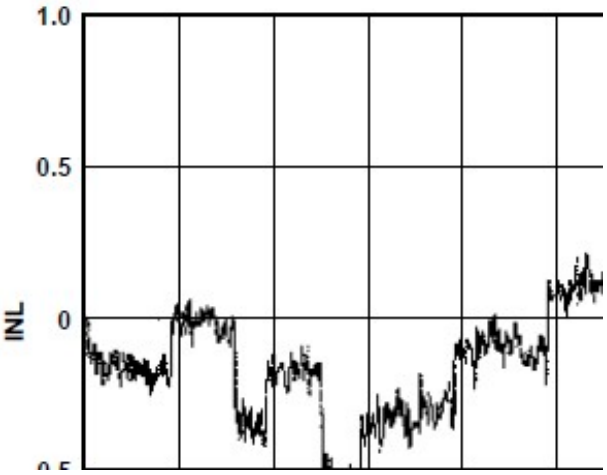


Figure 4. Typical INL

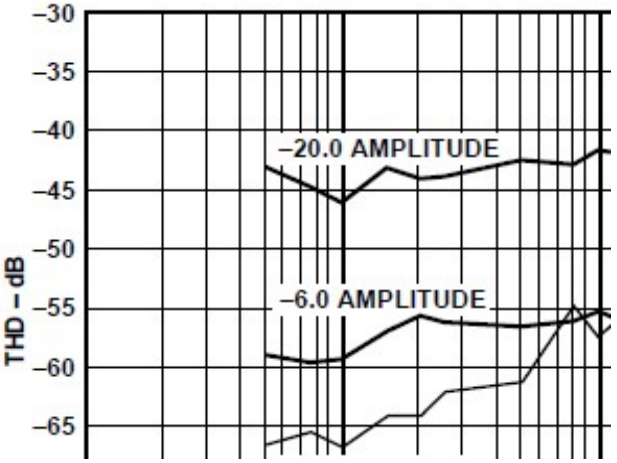


Figure 7. THD vs. Input Frequency

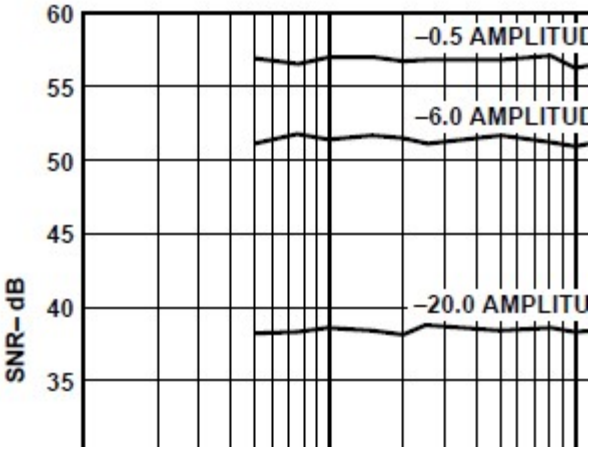


Figure 5. SNR vs. Input Frequency

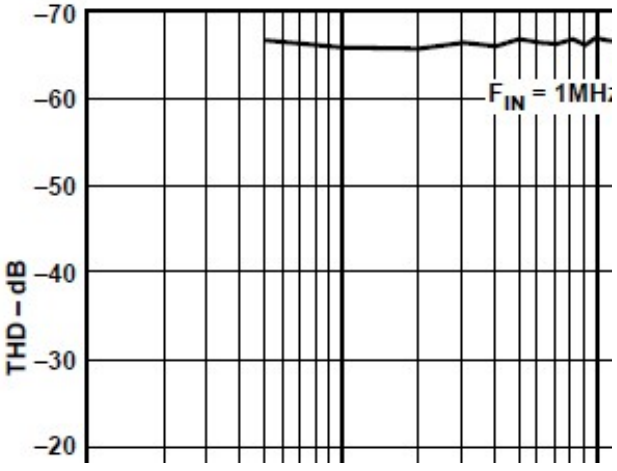


Figure 8. THD vs. Clock Frequency

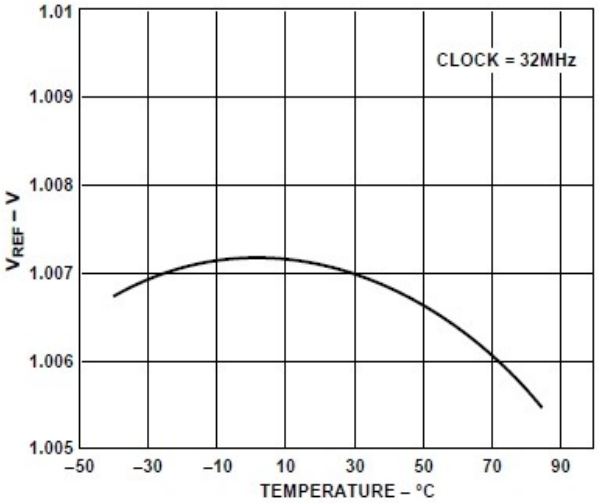


Figure 9. Voltage Reference Error vs. Temperature

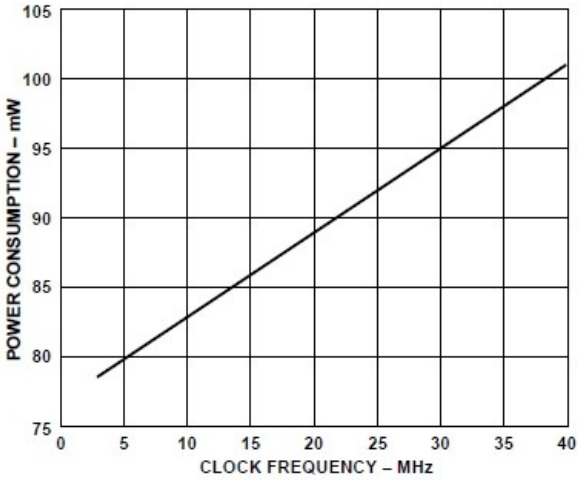


Figure 10. Power Consumption vs. Clock Frequency

APPLICATIONS

THEORY OF OPERATION

The 3PA1030 implements a pipelined multistage architecture to achieve high sample rate with low power. The 3PA1030 distributes the conversion over several smaller A/D sub-blocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the 3PA1030 requires a small fraction of the 256 comparators used in a traditional flash type A/D. A sample and hold function within each of the stages permits the first stage to operate on a new input sample while the second, third and fourth stages operate on the three preceding samples.

OPERATIONAL MODES

The 3PA1030 is designed to allow optimal performance in a wide variety of imaging, communications and instrumentation applications. To realize this flexibility, internal switches on the 3PA1030 are used to reconfigure the circuit into different modes. These modes are selected by appropriate pin strapping. There are three parts of the circuit affected by this modality: the voltage reference, the reference buffer, and the analog input. The nature of the application will determine which mode is appropriate: the descriptions in the following sections, as well as Table I should assist in selecting the desired mode.

Table I. Mode Selection

Modes	Input Connect	Input Span	REFSENSE	REF	REFTS	REFBS	FIGURE
TOP/BOTTOM	AIN	1V	Short REFSENSE, REFTS and VREF Togeter			AGND	18
	AIN	2V	AGND	Short REFTS and VREF Togeter		AGND	19
CENTER SPAN	AIN	1V	Short VREF and REFSENSE Together			AVDD/2	20
	AIN	2V	AGND			AVDD/2	
Differential	AIN Is Input 1 REFTS and REFBS are Shorted Together for input 2	1V	Short VREF and REFSENSE Together			AVDD/2	27
		2V	AGND	No Connect		AVDD/2	
External Ref	AIN	2V max	AVDD	External reference	Span=REFTS-REFBS(2V max)		21
					Short to VREF	Short to VREF	

SUMMARY OF MODES

VOLTAGE REFERENCE

1 V Mode the internal reference may be set to 0.5 V by connecting REFSENSE and VREF together.
2 V Mode the internal reference may be set to 1 V by connecting REFSENSE to analog ground
External Divider Mode the internal reference may be set to a point between 0.5 V and 1 V by adding external resistors. See Figure 12-f.
External Reference Mode enables the user to apply an external reference to VREF pin. This mode is attained by tying REFSENSE to VDD.

REFERENCE BUFFER

Center Span Mode midscale is set by shorting REFTS and REFBS together and applying the midscale voltage to that point. The analog input will swing about that midscale point.
Top/Bottom Mode sets the input range between two points. The two points are between 1 V and 2 V apart.

ANALOG INPUT

Differential Mode is attained by driving the AIN pin as one differential input, shorting REFTS and REFBS together and driving them as the second differential input.
Single Ended is attained by driving the AIN pin while the REFTS and REFBS pins are held at dc points.
Single Ended/Clamped (AC Coupled) the input may be clamped to some dc level by ac coupling the input. This is done by tying the CLAMPIN to some dc point and applying a pulse to the CLAMP pin.

INPUT AND REFERENCE OVERVIEW

Figure 12, a simplified model of the 3PA1030, highlights the relationship between the analog input, AIN, and the reference voltages, REFTS, REFBS and VREF. Like the voltages applied to the resistor ladder in a flash ADC, REFTS and REFBS define the maximum and minimum input voltages to the A/D.
The input stage is normally configured for single ended operation, but allows for differential operation by shorting REFTS and REFBS together to be used as the second input.

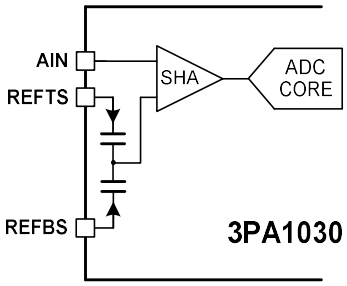
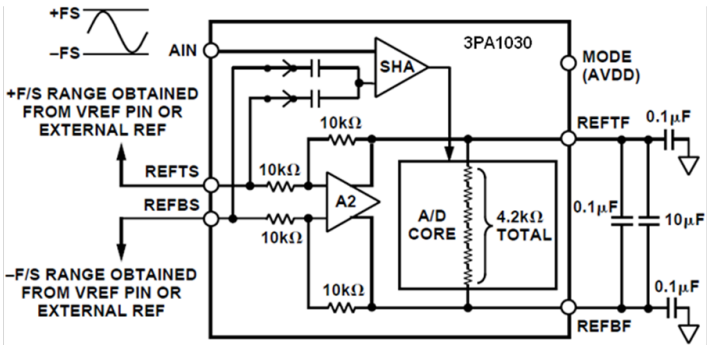


Figure 11. 3PA1030 Equivalent Functional Input Circuit

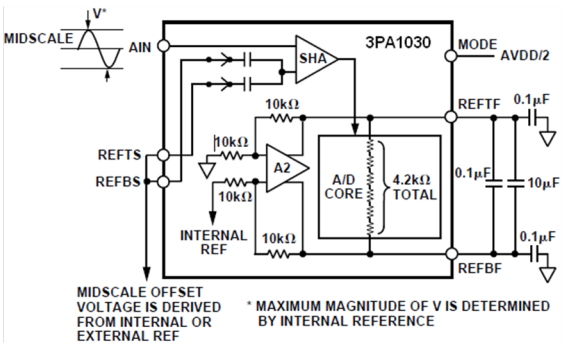
In single-ended operation, the input spans the range, ***0 ≤AIN ≤ 2xVREF.*** Where REFBS can be connected to GND and REFTS connected to VREF. If the user requires a different reference range, REFBS and REFTS can be driven to any voltage within the power supply rails, so long as the difference between the two is between 1 V and 2 V.
In differential operation, REFTS and REFBS are shorted together, and the input span is set by 2xVREF, ***(REFTS – VREF) ≤AIN ≤ (REFTS + VREF).*** Where VREF is determined by the internal reference or brought in externally by the user.
The best noise performance may be obtained by operating the 3PA1030 with a 2 V input range. The best distortion performance may be obtained by operating the 3PA1030 with a 1 V input range.

REFERENCE OPERATION

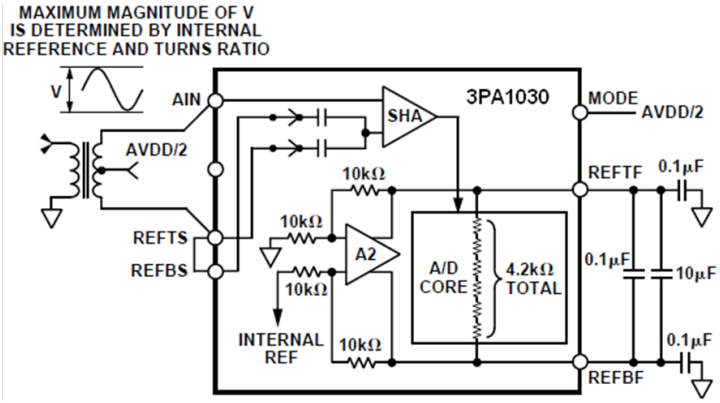
The 3PA1030 can be configured in a variety of reference topologies. The simplest configuration is to use the 3PA1030's onboard bandgap reference, which provides a pin-strappable option to generate either a 0.5 V or 1 V output. If the user desires a reference voltage other than those two, an external resistor divider can be connected between VREF, REFSENSE and analog ground to generate a potential anywhere between 0.5 V and 1 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance.
Figures 12-d, 12-e and 12-f illustrate the reference and input architecture of the 3PA1030. In tailoring a desired arrangement, the user can select an input configuration to match drive circuit. Then, moving to the reference modes at the bottom of the figure, select a reference circuit to accommodate the offset and amplitude of a full scale signal. **Table I outlines pin configurations to match user requirements.**



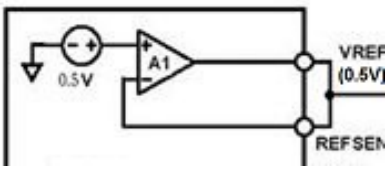
a. Top/Bottom Mode



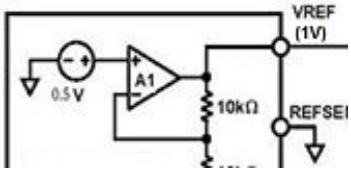
b. Center Span Mode



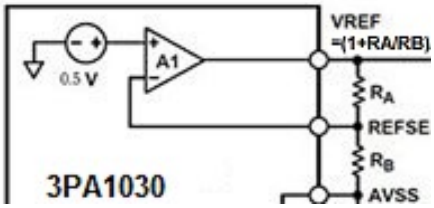
c. Differential Mode



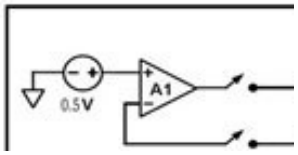
d. 0.5 V Reference



e. 1 V Reference



f. Variable Reference (Between 0.5 V and 1 V)



g. Internal Reference Disable(Power Reduction)

Figure 12.

The actual reference voltages used by the internal circuitry of the 3PA1030 appear on REFTF and REFBF. For proper operation, it is necessary to add a capacitor network to decouple these pins. The REFTF and REFBF should be decoupled for all internal and external configuration as shown in Figure 13.

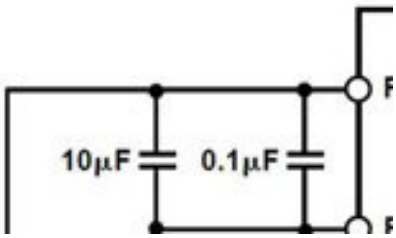


Figure 13. Reference Decoupling Network

Note:

REFTF = reference top, force
REFBF = reference bottom, force
REFTS = reference top, sense
REFBS = reference bottom, sense

INTERNAL REFERENCE OPERATION

Figures 14, 15 and 16 show sample connections of the 3PA1030 internal reference in its most common configurations. (Figures 14 and 15 illustrate top/bottom mode while Figure 16 illustrates center span mode). Figure 23 shows how to connect the 3PA1030 for 1 V_{P-P} differential operation. Shorting the VREF pin directly to the REFSENSE pin places the internal reference amplifier, A1, in unity-gain mode and the resultant reference output is 0.5 V. In Figure 14 REFBS is grounded to give an input range from 0 V to 1 V. These modes can be chosen when the supply is either +3 V or +5 V. The VREF pin must be bypassed to AVSS (analog ground) with a 1.0 uF tantalum capacitor in parallel with a low inductance, low ESR, 0.1uF ceramic capacitor.

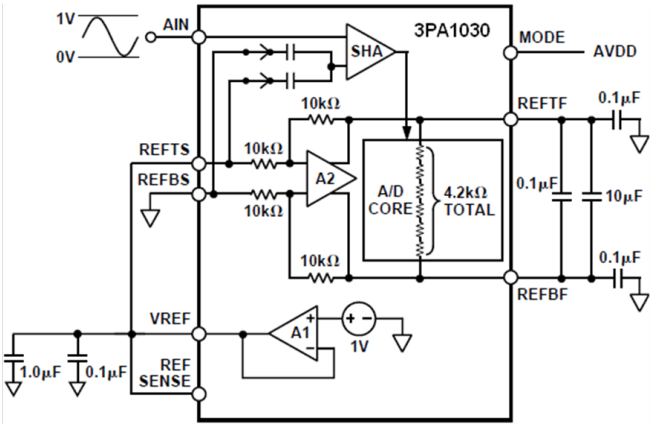


Figure 14. Internal Reference, 1V p-p Input Span (Top/Bottom Mode)

Figure 15 shows the single-ended configuration for 2 V_{P-P} operation. REFSENSE is connected to GND, resulting in a 1 V reference output.

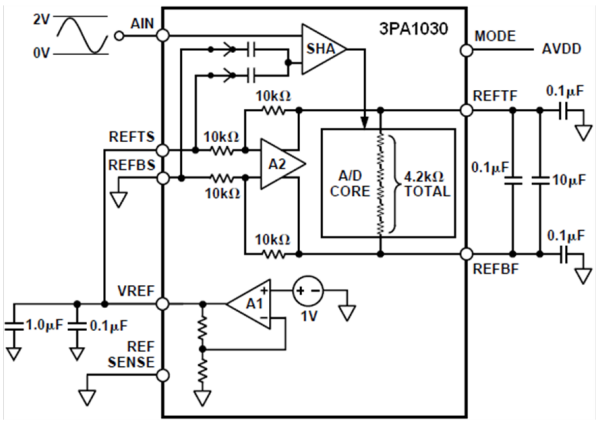


Figure 15. Internal Reference, 2 V_{P-P} Input Span (Top/Bottom Mode)

Figure 16 shows the single-ended configuration that gives the good high frequency dynamic performance (SINAD, SFDR). To optimize dynamic performance, center the common-mode voltage of the analog input at approximately 1.5 V. Connect the shorted REFTS and REFBS inputs to a low impedance 1.5 V source. Maximum reference drive is 1 mA. An external buffer is required for heavier loads.

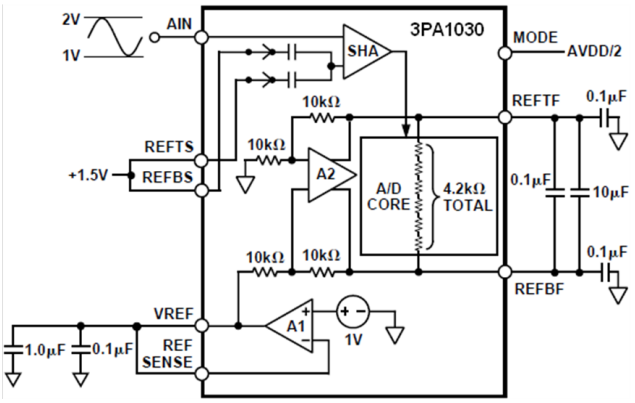


Figure 16. Internal Reference 1 V_{P-P} Input Span (Center Span Mode)

EXTERNAL REFERENCE OPERATION

Using an external reference may provide more flexibility and improve drift and accuracy. Figures 17 show examples of how to use an external reference with the 3PA1030. To use an external reference, the user must disable the internal reference amplifier by connecting the REFSENSE pin to VDD and drive the VREF pin with user-defined reference voltage.

The 3PA1030 contains an internal reference buffer (A2), that simplifies the drive requirements of an external reference. The external reference must simply be able to drive a 10 kΩ load.

Figure 17 shows an example of an external reference generating 2.5 V at the shorted REFTS and REFBS inputs. In this instance, a REF43 2.5 V reference drives REFTS and REFBS. A resistive divider generates a 1 V VREF signal that is buffered by A3. A3 must be able to drive a 10 kΩ, capacitive load. Choose this op-amp based on noise and accuracy requirements.

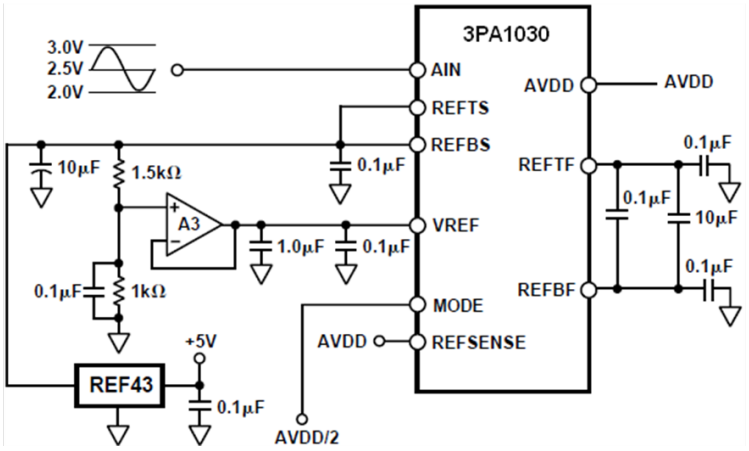


Figure 17. External Reference Mode—1 V_{P-P} Input Span 2.5 V_{CM}

STANDBY OPERATION

The ADC may be placed into a powered down (sleep) mode by driving the STBY (standby) pin to logic high potential and holding the clock at logic low. In this mode the typical power drain is approximately 4mW. The ADC will “wake up” in 400ns (typ.) after the standby pulse goes low.

CLAMP OPERATION

The 3PA1030 may be driven with a dc-coupled or ac-coupled input signal. When the input signal is ac-coupled, it features a flexible bottom-level clamp circuit for dc restoration of the signal. Figure 18 shows the external control signals needed for clamp operation. In ac-coupled cases, when a logic high or a pulse such as the H-sync in video systems is applied to the CLAMP pin, the bottom level of the signal AIN is clamped to the voltage provided at the CLAMP IN pin (Figure 18-a). The allowable voltage range that can be applied to CLAMPIN depends on the operational limits of the internal clamp amplifier. The recommended clamp range is between 0 volts and 1.0 volts. The logic high CLAMP control might be useful for some video applications since H-sync generating circuitry may be omitted. When a logic low is applied to CLAMP pin (Figure 18-b), the bottom level of the signal AIN is clamped to ground level. When the input is dc-coupled, CLAMP is recommended to be shorted to logic low (Figure 18-c). The dc input signal level needs to be higher than 0V.

The input capacitor should be sized to allow sufficient acquisition time of the clamp voltage at AIN within the CLAMP interval, but also be sized to minimize droop between clamping intervals. For video applications, input capacitor of 0.1uF is recommended.

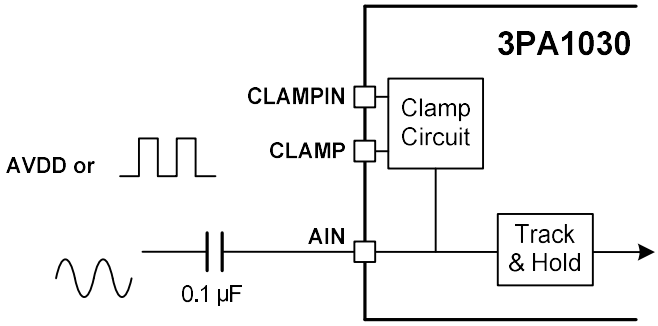


Figure 18-a, Bottom signal level clamped to CLAMPIN

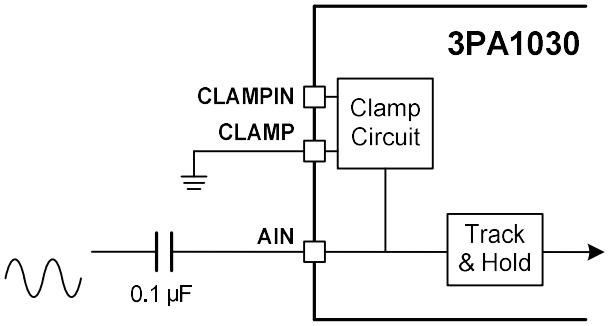


Figure 18-b, Bottom signal level clamped to ground

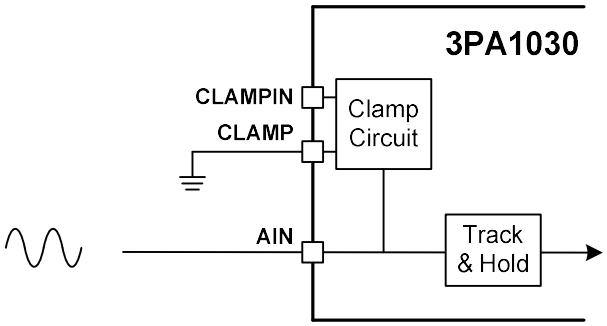


Figure 18-c, DC-coupled input

DRIVING THE ANALOG INPUT

Figure 19 shows the equivalent analog input of the 3PA1030, a sample-and-hold amplifier (switched capacitor input SHA). Bringing CLK to a logic low level closes Switches 1 and 2 and opens Switch 3. The input source connected to AIN must charge capacitor CH during this time. When CLK transitions from logic "low" to logic "high," Switches 1 and 2 open, placing the SHA in hold mode. Switch 3 then closes, forcing the output of the op amp to equal the voltage stored on CH. When CLK transitions from logic "high" to logic "low," Switch 3 opens first. Switches 1 and 2 close, placing the SHA in track mode.

The structure of the input SHA places certain requirements on the input drive source. The combination of the pin capacitance, CP, and the hold capacitance, CH, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 8-bit accuracy in one half of a clock cycle. When the SHA goes into track mode, the input source must charge or discharge capacitor CH from the voltage already stored on CH to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the RON (50 Ω) of Switch 1 and quickly (within 1/2 CLK period) settle. This situation corresponds to driving a low input impedance. On the other hand, when the source voltage equals the value previously stored on CH, the hold capacitor requires no input current and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN pin reduces the drive requirements placed on the source. Figure 20 shows this configuration. The bandwidth of the particular application limits the size of this resistor. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to 20 Ω or less. For applications with signal bandwidths less than 16 MHz, the user may proportionally increase the size of the series resistor. Alternatively, adding a shunt capacitance between the AIN pin and analog ground can lower the ac load impedance. The value of this capacitance will depend on the source resistance and the required signal bandwidth. The input span of the 3PA1030 is a function of the reference voltages. For more information regarding the input range, see the Internal and External Reference sections of the data sheet.

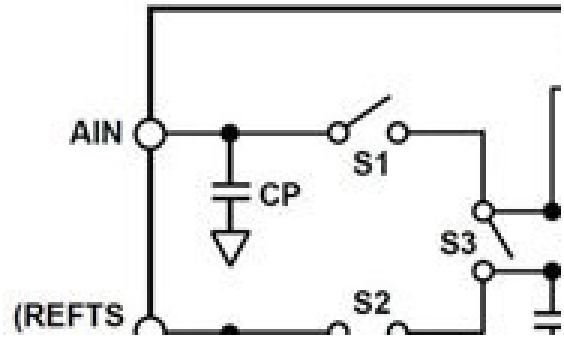


Figure 19. 3PA1030 Equivalent Input Structure

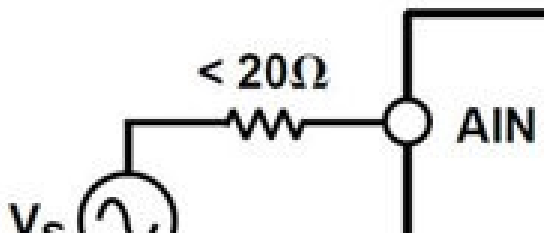


Figure 20. Simple 3PA1030 Drive Configuration

In many cases, particularly in single-supply operation, ac coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 21 shows a typical configuration for ac-coupling the analog input signal to the 3PA1030. Maintaining the specifications outlined in the datasheet requires careful selection of the component values. The most important is the $f_{-3\,dB}$ high-pass corner frequency. It is a function of R2 and the parallel combination of C1 and C2. The $f_{-3\,dB}$ point can be approximated by the equation: $f_{-3\,dB} = 1/(2 \times pi \times [R2]\, C_{EQ})$. Where C_{EQ} is the parallel combination of C1 and C2. Note that C1 is typically a large electrolytic or tantalum capacitor that becomes inductive at high frequencies. Adding a small ceramic or polystyrene capacitor (on The order of 0.01F) that does not become inductive until negligibly higher frequencies, maintains a low impedance over a wide frequency range.

NOTE: AC coupled input signals may also be shifted to a desired level with the 3PA1030's internal clamp. See Clamp Operation.

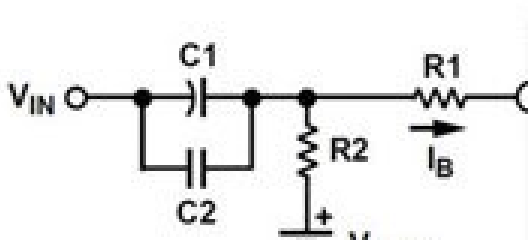


Figure 21. AC Coupled Input

There are additional considerations when choosing the resistor values. The ac-coupling capacitors integrate the switching transients present at the input of the 3PA1030 and cause a net dc bias current, I_B, to flow into the input. The magnitude of the bias current increases as the signal magnitude deviates from V midscale and the clock frequency increases; i.e., minimum bias current flow when AIN = V midscale. This bias current will result in an offset error of (R1 + R2) X I_B. If it is necessary to compensate this error, consider making R2 negligibly small or modifying VBIAS to account for the resultant offset.

In systems that must use dc coupling, use an op-amp to level-shift a ground-referenced signal to comply with the input requirements of the 3PA1030. Figure 22 shows an AD8041 configured in non-inverting mode.

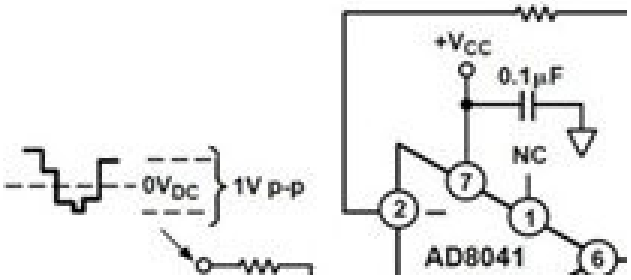


Figure 22. Bipolar Level Shift

DIFFERENTIAL INPUT OPERATION

The 3PA1030 will accept differential input signals. This function may be used by shorting REFTS and REFBS and driving them as one leg of the differential signal (the top leg is driven into AIN). In the configuration below, the 3PA1030 is accepting a 1 V_{P-P} signal. See Figure 23.

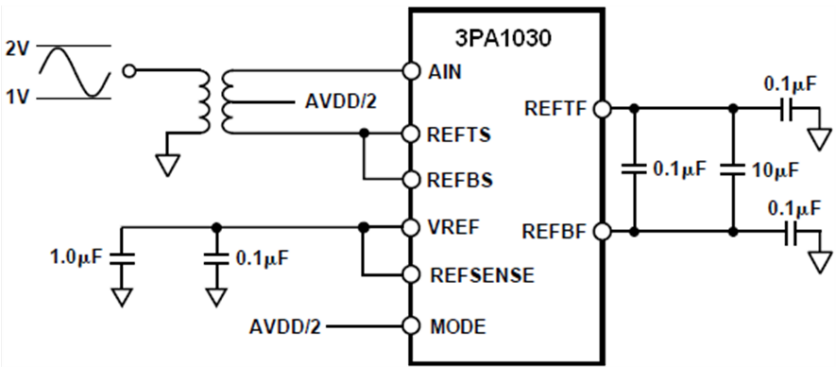


Figure 23. Differential Input

CLOCK INPUT

The 3PA1030 clock input is buffered internally with an inverter powered from the AVDD pin. This feature allows the 3PA1030 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at AVDD/2 as Figure

24.

The pipelined architecture of the 3PA1030 operates on both rising and falling edges of the input clock. To minimize duty cycle variations the recommended logic family to drive the clock input is high speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 50 MSPS operation. The 3PA1030 is designed to support a conversion rate of 50 MSPS; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the 3PA1030 at slower clock rates.

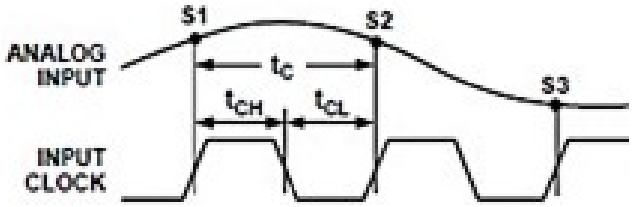


Figure 24. Timing Diagram

The power dissipated by the output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption.

DIGITAL INPUTS AND OUTPUTS

The ADC's baseband region. A tradeoff exists between the complexity of this image rejection filter and the sample rate as well as dynamic range of the ADC. Each of the 3PA1030 digital control inputs, 3-STATE (OE) and STBY are reference to analog ground. The clock is also referenced to analog ground. The format of the digital output is straight binary (see Figure 25). A low power mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the 3PA1030 will drop below 5 mW.

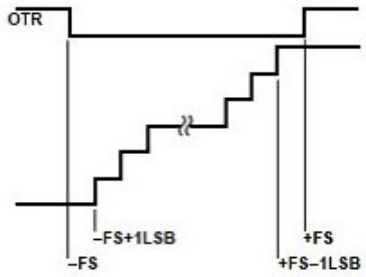


Figure 25. Output data format

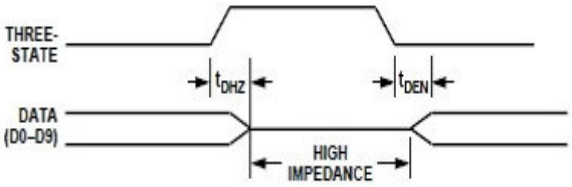


Figure 26. Three-State Timing Diagram

DIRECT IF DOWN CONVERSION USING THE 3PA1030

Sampling IF signals above an ADC's baseband region (i.e., dc to $F_S/2$) is becoming increasingly popular in communication applications. This process is often referred to as "Direct IF Down Conversion" or "Under-sampling". There are several potential benefits in using the ADC to alias (i.e., or mix) down a narrowband or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, detection, etc.

In Direct IF Down Conversion applications, one exploits the inherent sampling process of an ADC in which an IF signal lying outside the baseband region can be aliased back into the baseband region in a similar manner that a mixer will down convert an IF signal. Similar to the mixer topology, an image rejection filter is required to limit other potential interfering signals from also aliasing back into The 3PA1030 is well suited for various narrowband IF sampling applications. The 3PA1030's low distortion input SHA has a full-power bandwidth extending to 300 MHz thus encompassing many popular IF frequencies. The 3PA1030 will typically yield an improvement in SNR when configured for the 2 V span, the 1 V span provides the optimum full-scale distortion performance. Furthermore, the 1 V span reduces the performance

requirements of the input driver circuitry and thus may be more practical for system implementation purposes.

Figure 27 shows a simplified schematic of the 3PA1030 configured in an IF sampling application. To reduce the complexity of the digital demodulator in many quadrature demodulation applications, the IF frequency and/or sample rate are selected such that the band-limited IF signal aliases back into the center of the ADC's baseband region (i.e., $F_S/4$). For example, if an IF signal centered at 45 MHz is sampled at 20 MSPS, an image of this IF signal will be aliased back to 5.0 MHz which corresponds to one quarter of the sample rate (i.e., $F_S/4$). This demodulation technique typically reduces the complexity of the post digital demodulator ASIC which follows the ADC.

To maximize its distortion performance, the 3PA1030 is configured in the differential mode with a 1 V span using a transformer. The center tap of the transformer is biased at mid-supply via a resistor divider. Preceding the 3PA1030 is a band-pass filter as well as a 32 dB gain stage. A large gain stage may be required to compensate for the high insertion losses of a SAW filter used for image rejection. The gain stage will also provide adequate isolation for the SAW filter from the charge "kick back" currents associated with 3PA1030's input stage.

The gain stage can be realized using one or two cascaded op-amps of "1 GHz, current-feedback op-amp having a 3rd order intercept characterized up to 250 MHz". A passive band-pass filter following the op-amps attenuates its dominant 2nd order distortion products which would otherwise be aliased back into the 3PA1030's baseband region. Also, it reduces any out-of-band noise which would also be aliased back due to the 3PA1030's noise bandwidth of 220+ MHz. Note, the band-pass filters specifications are application dependent and will affect both the total distortion and noise performance of this circuit.

The distortion and noise performance of an ADC at the given IF frequency is of particular concern when evaluating an ADC for a narrowband IF sampling application. Both single-tone and dual-tone SFDR vs. amplitude are very useful in assessing an ADC's noise performance and noise contribution due to aperture jitter. In any application, one is advised to test several units of the same device under the same conditions to evaluate the given applications sensitivity to that particular device.

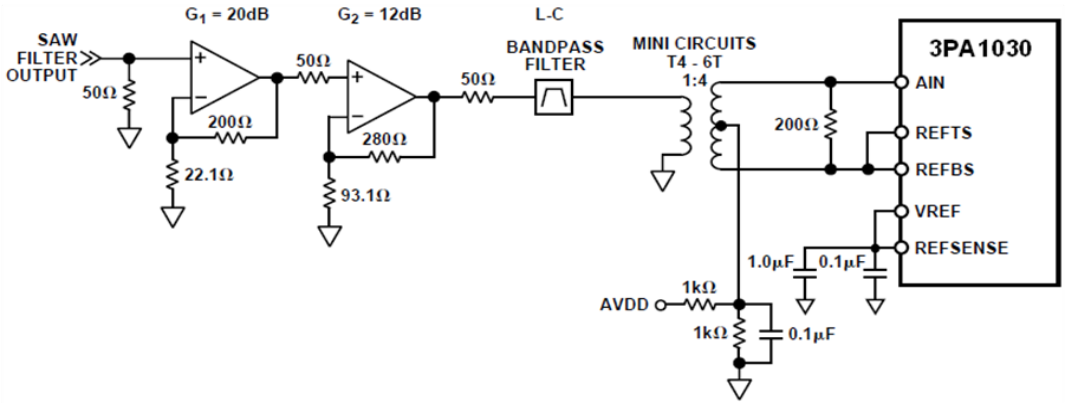


Figure 27. Simplified 3PA1030 IF Sampling Circuit

Figures 28-31 combine the dual-tone SFDR as well as single tone SFDR and SNR performance at IF frequencies of 45 MHz, 70 MHz, 85 MHz and 135 MHz. Note, the SFDR vs. amplitude data is referenced to dBFS while the single tone SNR data is referenced to dBc.

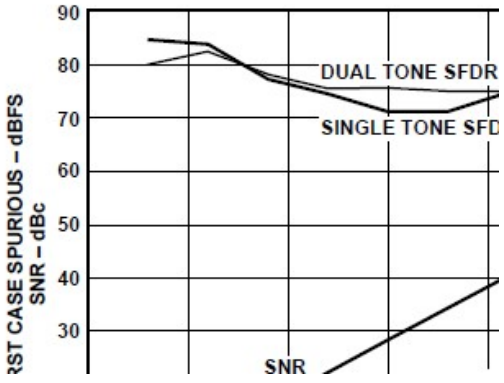


Figure 28. SNR/SFDR for IF @ 45 MHz

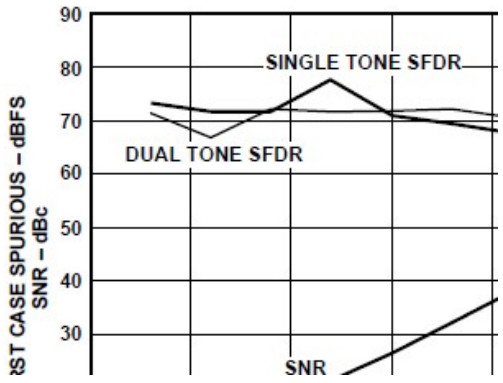


Figure 29. SNR/SFDR for IF @ 70 MHz

The 3PA1030 was operated in the differential mode (via transformer) with a 1 V span. The analog supply (AVDD) and the digital supply (DRVDD) were set to +5 V and 3.3 V, respectively.

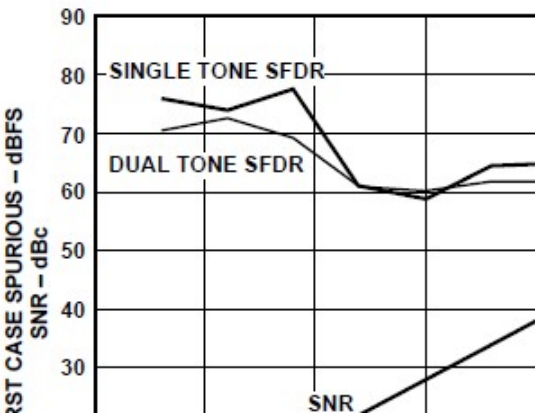


Figure 30. SNR/SFDR for IF @ 85 MHz

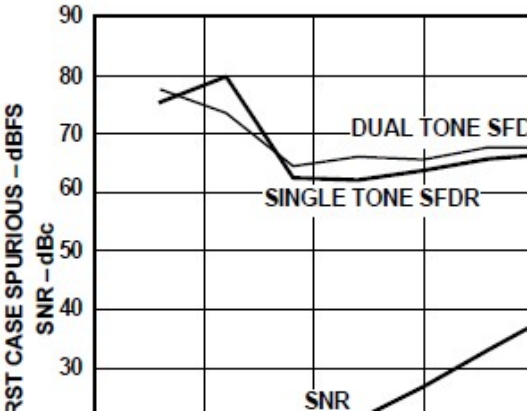


Figure 31. SNR/SFDR for IF @ 135 MHz

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the 3PA1030 have been separated to optimize the management of return currents in a system. Grounds should be connected near the ADC. It is recommended that a printed circuit board (PCB) of at least four layers, employing a ground plane and power planes, be used with the 3PA1030. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. Separate analog and digital grounds should be joined together directly under the 3PA1030 in a solid ground plane. The power and ground return currents must be carefully managed. A general rule of thumb for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry.

DIGITAL OUTPUTS

Each of the on-chip buffers for the 3PA1030 output bits (D0–D9) is powered from the DRVDD supply pins, separate from AVDD. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20 pF level.

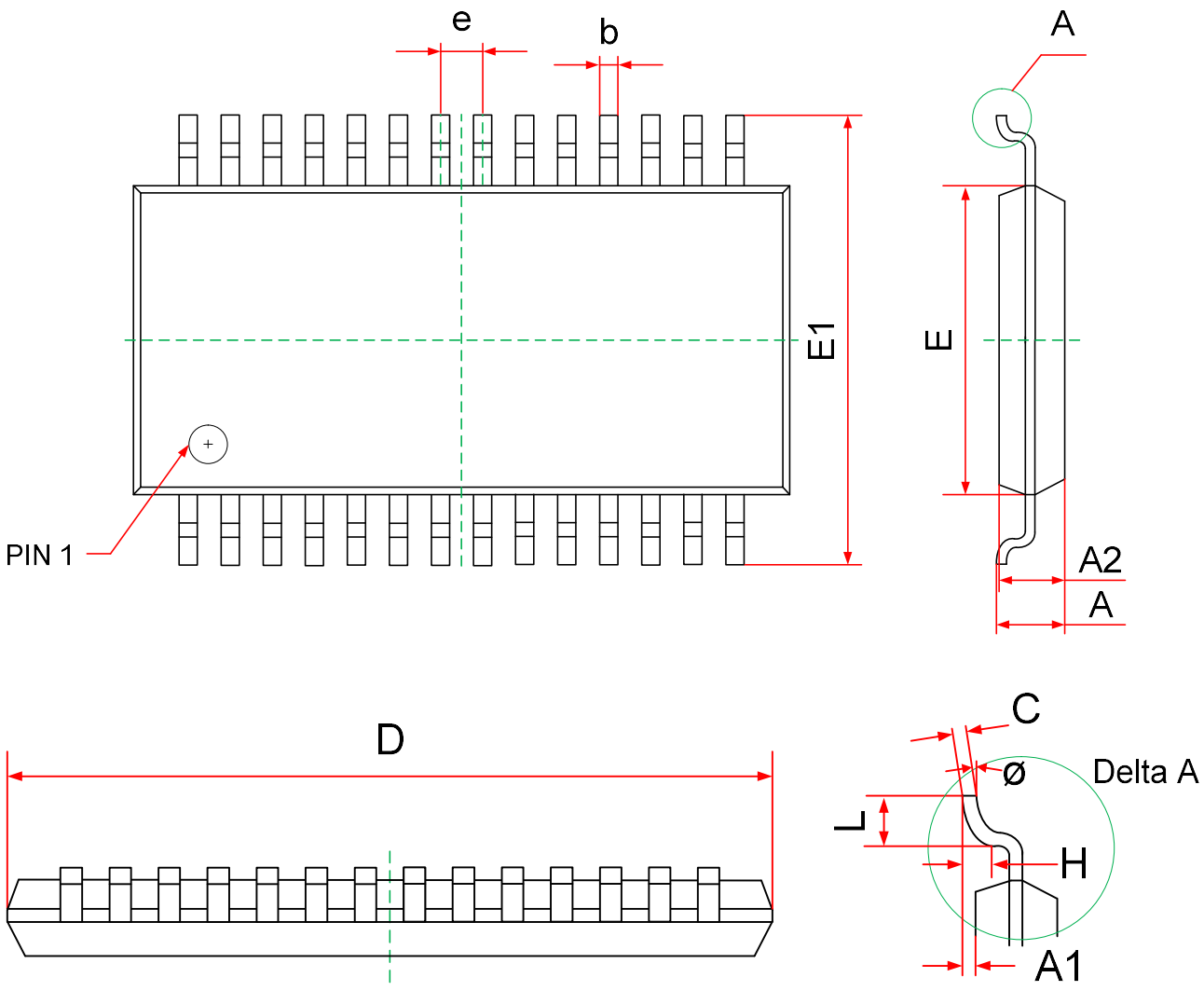
For DRVDD = 5 V, the 3PA1030 output signal swing is compatible with both high speed CMOS and TTL logic families. For TTL, the 3PA1030 on-chip, output drivers were designed to support several of the high speed TTL families (F, AS, S). For applications where the clock rate is below 50 MSPS, other TTL families may be appropriate. For interfacing with lower voltage CMOS logic, the 3PA1030 sustains 50 MSPS operation with DRVDD = 3 V. In all cases, check your logic family data sheets for compatibility with the 3PA1030 Digital Specification table.

THREE-STATE OUTPUTS

The digital outputs of the 3PA1030 can be placed in a high impedance state by setting the THREE-STATE pin to HIGH. This feature is provided.

OUTLINE DIMENSIONS

28-Lead Thin Shrink Small Outline Package (TSSOP) --Dimensions are shown in millimeters and inches.



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

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