

3-Phase Synchronous PWM Controller IC Provides an Integrated Solution for Intel VRM 9.0 Design Guidelines

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The fundamental reason for the rapid change and growth in information technology power requirements is the increase in volume of data processed, stored, transmitted, and displayed. As a result, power requirements have grown very rapidly. To control the increase in power dissipation, operating voltages have been reduced. Power scales as the square of the voltage: cut the voltage in half, and the power dissipation is reduced to one fourth. As circuit output voltages approach the one-volt mark, operating currents are increasing exponentially. Today, feeding this much “ultraclean” current at these low voltages with tremendous transient response capability is the key technology driver of power management for IT.

CPUs used in servers, advance desktop computers and motherboards such as the Intel Pentium™ 4 or Xeon™ or AMD K7™ typically require currents up to 60A at output voltages around 1V, with transient response in the order of 50A/us. Designers prefer a multiphase DC-DC converter topology to address the higher

current requirements and faster transient response problem,

This article will discuss the specific requirements for DC-DC converters required to power today’s GHz class CPUs, the benefits of the multiphase topology, and an example of implementation of Intel VRM 9.0 using an integrated 3-phase synchronous PWM controller IC.

An Overview of Intel VRM 9.0 Design Guidelines

With today’s microprocessor voltage below 2V, they cannot be powered directly out of the conventional silver box that typically provides 5V and 12V. Located in proximity to the CPU, the voltage regulator module (VRM) delivers regulated, stepped down voltage to the CPU. The Intel VRM 9.0 definition is specifically intended to meet the needs of systems based on the Intel ® Xeon™ and Pentium ® 4 processors. Table 1 provides a summary of the output requirements for VRM 9.0.

Symbol	Parameter	VID	Minimum	Maximum	Unit
V _{out-VRM}	Output voltage measured at the solder side of the VRM mating connector ^{1,2,3}	1.70	1.609	1.70	V
		1.50	1.408	1.50	
V _{CC_CORE}	Output voltage measured at the processor sense pins on the solder side of the processor socket ^{1,2,3}	1.70	1.560	1.70	V
		1.50	1.330	1.50	
V _{MAX}	Maximum, non-operating (failure) voltage	1.70		2.1	V
		1.50		1.75	
I _{out_MAX}	Maximum static VRM current for V _{out} ^{4,5}	1.70		60	A
		1.50		65	
dI _{out} /dt _{MAX}	Output slew rate ⁶			50	A/μs

Table 1 - Summary of the VRM 9.0 output requirements (Source: Intel VRM9.0 DC-DC converter design guidelines).

Other requirements include VID voltage identification and Power Good feedback. The VRM must accept five lines to set the nominal maximum voltage. Five processor package pins

will have a high-low pattern corresponding to the voltage required by the individual processor. The VRM should provide an open collector

Power Good signal consistent with TTL DC levels.

Multiphase Synchronous Buck Converters

Multiphase topologies are a necessary approach to achieve the power needs of today's microprocessors with high efficiency and without large, expensive and bulky magnetics and capacitors. Multiple buck converters are usually connected in parallel to reduce the power capability for each individual converter as well as alleviate the thermal stress on each of the power devices. Each phase-leg carries $1/N$ of the total current supplied, where N is the number of phases. Each leg operates out-of-phase with all others allowing the sum of the legs to add up to a regulated DC level with significantly less ripple and faster transient response capability than a single-phase converter. This is achieved without increasing the switching frequency per leg since the effective output frequency of a multiphase converter is the N times the frequency per phase.

A multiphase topology also allows the use of smaller input and output filters since ripple currents cancellation. It also produces faster transient response due to multiple inductors in parallel. Multiphase converters generally result in lower cost, smaller footprint or lower profile due to smaller inductors and capacitors. Finally, multiphase converters are comparatively more efficient than single-phase converter at equivalent output current ripple frequency and output current level. The reduced power loss from the ESR of the input capacitor and the low switching losses of the MOSFETs at the relatively low switching frequencies helps achieve high conversion efficiency and provides even heat distribution.

The designer always faces the dilemma of choosing the right amount of phases for his

application. More phases operating at a lower switching frequency saves on converter input/output capacitor cost without reducing efficiency, but also increases complexity, layout difficulty, and at some point total solution cost. With current MOSFET technology, the ideal current-per-phase ranges from 10 to 30 Amps. Designs operating at lower switching frequencies, using state-of-the-art MOSFETs, and having low thermal impedance, such as using heat sinks, tend to be in the upper end of this current range. Designs targeting compact size, minimal input and output capacitors, and maximum efficiency tend to be in the lower end of this current range.

One way to determine the optimal number of phases is by the number of MOSFETs required to handle the per-phase current. If it is necessary to use 2 or more MOSFETs for both high and low side, consider adding an additional phase. The cost and size of the additional phase is compensated for by the reduction in input and output capacitors. Design goals such as current ripple and transient response will provide further selection criteria for the determination of the right number of phases for the application.

Implementation of VRM9.0 compatible circuit using IRU3055 3-phase multiphase controller ICs

With power MOSFETs able to efficiently and cost-effectively deliver 20A per phase, 3-phase has emerged as the preferred number of phases to deliver 60A while meeting the design guidelines of Intel VRM 9.0. The IRU3055 is a five-bit programmable, three-phase synchronous PWM controller IC with integrated MOSFET drivers that enables a straight forward implementation of an efficient 3 phase converter delivering 60A at voltage as low as 1.075V (Fig 1).

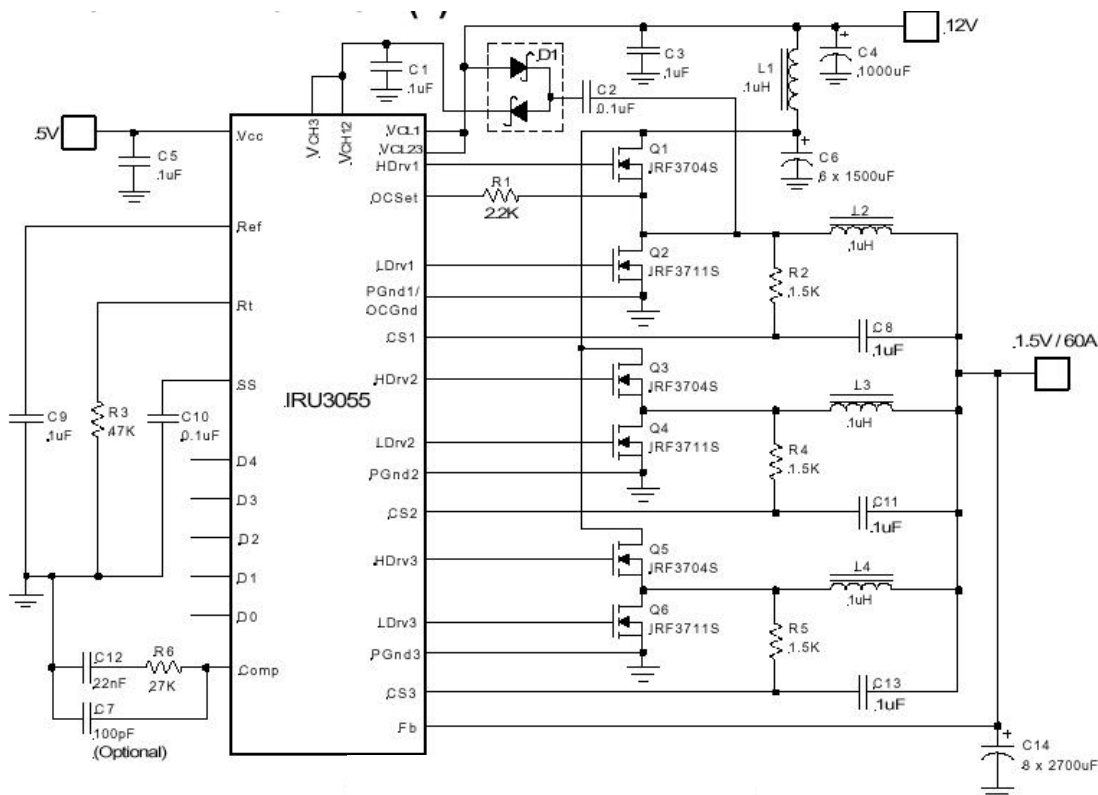


Figure 1 – Typical application of IRU3055

The IRU3055 has on-board MOSFET drivers, making it cost-effective compared to the majority of multiphase controllers, which require external MOSFET drivers. When used with IR’s HEXFET® power MOSFETs like the IRF3704S in the control FET socket and the IRF3711S in the synchronous FET socket, the IRU3055 can provide up to 60A for microprocessor V_{CORE} requirements at 80% efficiency or above.

The new controller IC is a fixed-frequency voltage mode controller with 50kHz to 500kHz programmable operating frequency by using an external resistor. The output voltage is selectable in 25mV steps from 1.075 to 1.85V with up to 1.5% output voltage accuracy using a programmable VID code to the five-bit digital-to-analog converter (DAC).

The new device has a number of features to provide protection and monitoring for the power system and the microprocessor. It features under-voltage lockout (UVLO) for the 5V and

12V supplies as well as an externally programmable soft-start function. Another feature is the PGOOD monitor circuit, which is held low if the output of the converter is not within $\pm 10\%$ of the programmed voltage.

The IRU3055 also provides over-voltage protection. If the output voltage exceeds the DAC-programmed voltage by 20%, the low-side MOSFETs turn on and shunt the output voltage to ground, protecting the CPU from damage. The IRU3055 features loss-less inductor current sensing and sharing while over-current protection is achieved by synchronous FET $R_{DS(on)}$ sensing, eliminating the need for a separate sense resistor. The IRU3055 can also be easily configured for voltage droop compensation so that the output voltage will linearly decrease as load current increases and vice versa, as required by Intel VRM design guidelines.

Operation of IRU3055

PWM Signal

The 3-phase oscillator provides a constant frequency up to 500kHz/phase, programmable by external resistor. The three PWMs ramp signals with 120 degree phase shift. The three comparators and three PWM latches will generate three PWM outputs to the drivers, which are built inside the IC. A typical 3-phase PWM signal is shown in Figure 2.

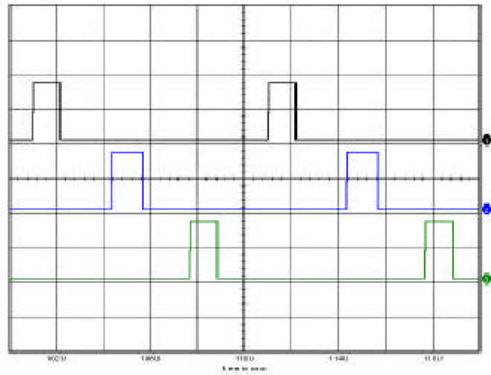


Figure 2 - The 3-phase PWM signal

Voltage and Current Loop

IRU3055 has three transconductance error amplifiers. The master Error amplifier is used to regulate the output voltage. The output voltage can connect directly, or through a resistor divider, to the Fb pin of the error amplifier. The compensation network at the output of the amplifier (Comp Pin) helps to stabilize the voltage loop. The non-inverting pin of the master amplifier is connected to the output of the DAC, which interfaces with the microprocessor core and determines the desired output voltage. Two additional transconductance

amplifiers are used to balance the output inductor current among 3-phases.

Output Current Ripple Reduction

One of advantages of multiphase converters is that the output current ripple is significantly reduced. The current ripple from multiple converters tend to cancel each other so that the total output current ripple flowing into the output capacitor is reduced. In this case, the output inductor in each individual buck converter can be selected smaller to improve the load transient response without increasing the output current ripple. Figure 3 shows a 3-phase inductor current and current ripple in the capacitor for 12V input 1.5V, 50A, 3-phase buck converter. The effective output ripple has three times frequency and smaller amplitude compared with each individual converter. Figure 4 indicates the total ripple current, as a function of duty cycle, normalized to the parameter $V_o/(L*F_s)$ at zero duty cycle.

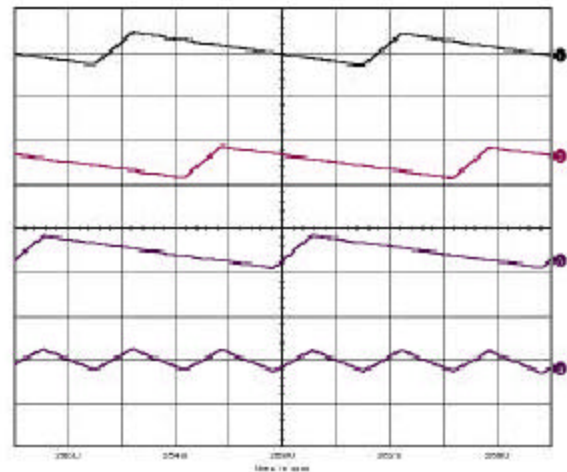


Figure 3- Output inductor currents and output capacitor ripple current.

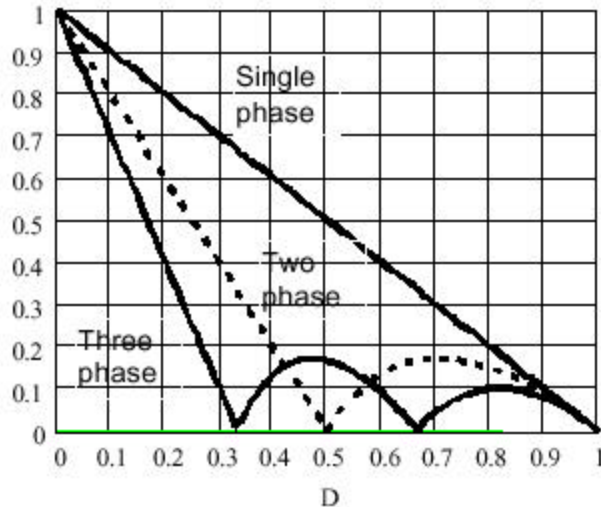


Figure 4 - Normalized output current across output capacitor, as a function of duty cycle, (Peak to peak current normalized to the $V_o/(L3Fs)$ at zero duty cycle).

It is shown that the output current ripple is greatly reduced by multi-phase operation. At the certain duty cycle $D=1/N$, where N is the phase number, the output ripple will be near zero due to complete cancellation of inductor current ripple. The optimum number of phases exists for different applications.

Built-in Synchronous-Rectifier Driver

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode with a low on-resistance MOSFET switch. The synchronous rectification also ensures good transient dynamic. The 3-phase synchronous rectifier MOSFET drivers are built inside the IRU3055.

Transient Response

The IRU3055 delivers transient response that meets Intel VRM 9.0 design guidelines with no oscillation and a voltage drop $<100\text{mV}$ for a 60A step load.

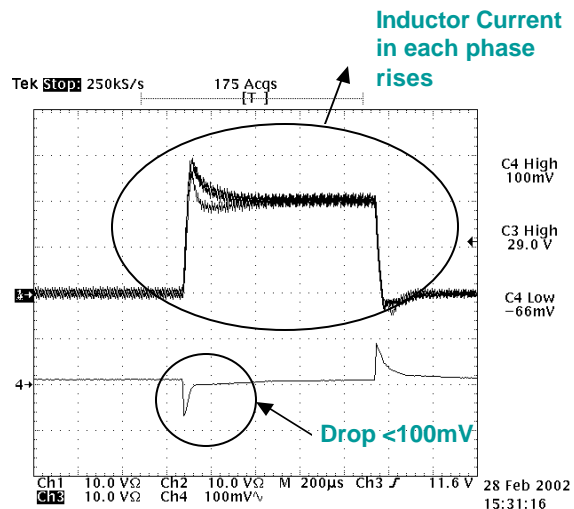


Figure 5 - 3-phase inductor current and V_{out} at 60A dynamic load response

Conclusion

With the development of new microprocessors always requiring more power, voltage are dropping to reduce power dissipation, driving currents upward exponentially. Higher currents also lead to faster transient response requirements and higher switching frequencies. Multiphase topology is the preferred topology to address the functionality of today's microprocessors voltage regulation requirements in a compact footprint at an acceptable cost. 3-phase converters appear to be the preferred way of economically meeting the design guidelines for Intel VRM9.0. The IRU3055 3-phase synchronous PWM controller IC provides an integrated solution for a straightforward implementation of Intel VRM 9.0.

As next generation processors emerge with more stringent power supply requirements and additional functionality, new approaches and advances in technology will be needed. More phases might be needed to meet the ever-increasing currents. With more phases come more design complexity, power dissipation and response delay. The partitioning of functionalities within voltage regulators will need to be optimized to provide the best performance at the best cost in compact footprints.