

## CD4017BC • CD4022BC

### Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

#### General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

#### Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45  $V_{DD}$  (typ.)
- Low power Fan out of 2 driving 74L TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.) with 10V  $V_{DD}$
- Low power: 10  $\mu$ W (typ.)
- Fully static operation

#### Applications

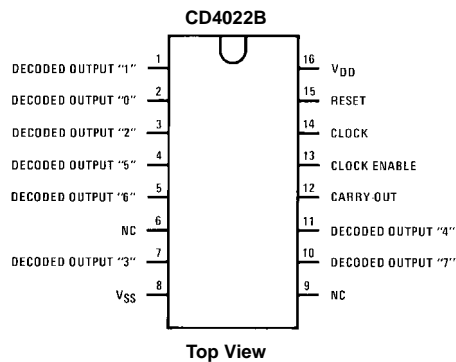
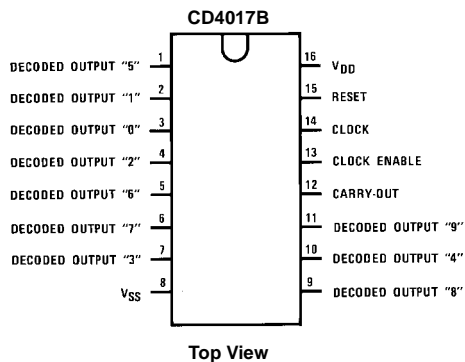
- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

#### Ordering Code:

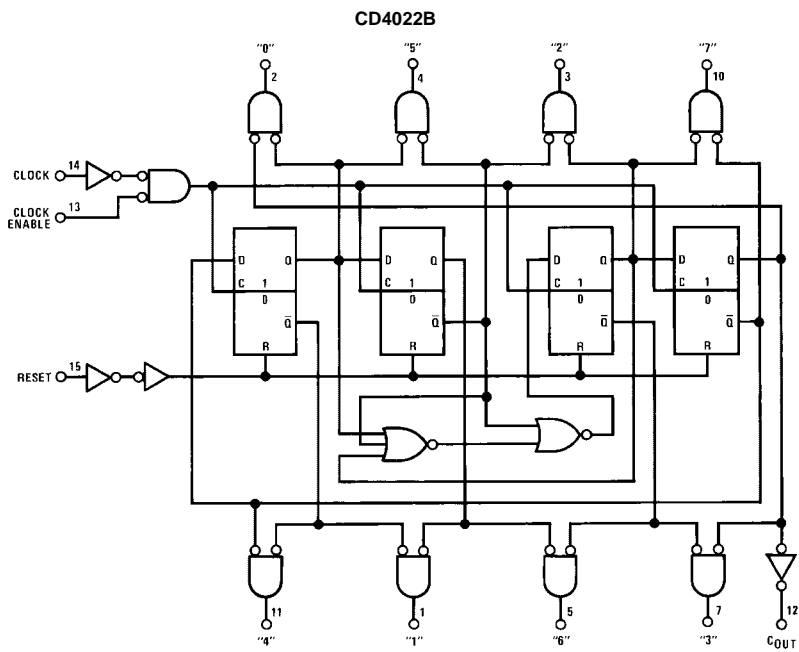
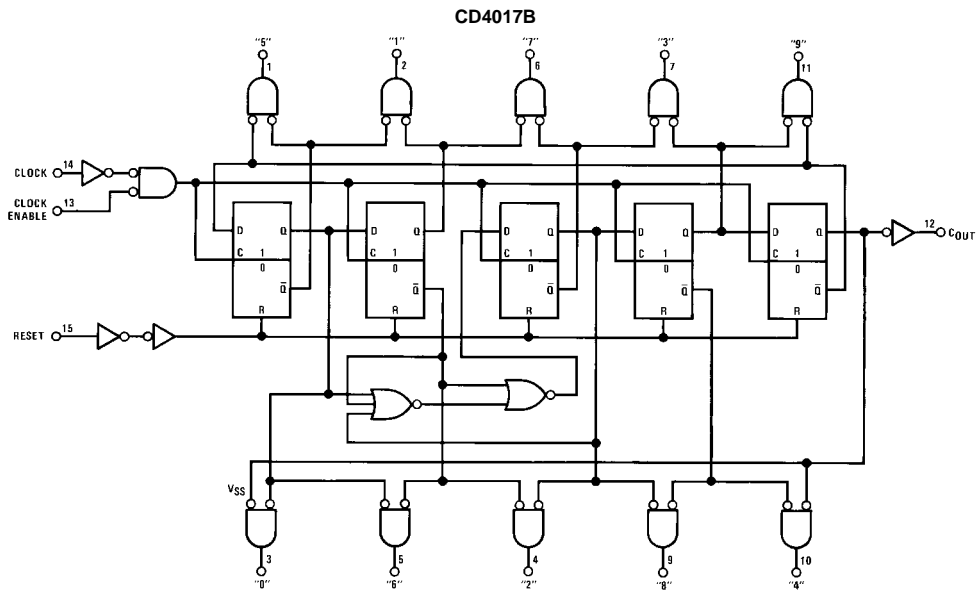
Order Number	Package Number	Package Description
CD4017BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4017BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4022BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4022BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagrams



Logic Diagrams



### Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage ( $V_{DD}$ )	-0.5 $V_{DC}$ to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 $V_{DC}$ to $V_{DD}$ +0.5 $V_{DC}$
Storage Temperature ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	+3 $V_{DC}$ to +15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	-55°C to +125°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

### DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		5		0.3	5		150	$\mu A$
		$V_{DD} = 10V$		10		0.5	10		300	
		$V_{DD} = 15V$		20		1.0	20		600	
$V_{OL}$	LOW Level Output Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V$		0.05		0	0.05		0.05	
		$V_{DD} = 10V$		0.05		0	0.05		0.05	
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
$V_{OH}$	HIGH Level Output Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V$	4.95		4.95	5		4.95		
		$V_{DD} = 10V$	9.95		9.95	10		9.95		
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
$V_{IL}$	LOW Level Input Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	
$V_{IH}$	HIGH Level Input Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.25		-0.2	-0.36		-0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	-0.62		-0.5	-0.9		-0.35		
		$V_{DD} = 15V, V_O = 13.5V$	-1.8		-1.5	-3.5		-1.1		
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	

**Note 3:**  $I_{OL}$  and  $I_{OH}$  are tested one output at a time.

**AC Electrical Characteristics** (Note 4)  
 $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}$ ,  $t_{rCL}$  and  $t_{fCL} = 20\text{ ns}$ , unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CLOCK OPERATION</b>						
$t_{PHL}, t_{PLH}$	Propagation Delay Time Carry Out Line	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		415 160 130	800 320 250	ns
	Carry Out Line	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	$C_L = 15\text{ pF}$	240 85 70	480 170 140	ns
	Decode Out Lines	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		500 200 160	1000 400 320	ns
$t_{TLH}, t_{THL}$	Transition Time Carry Out and Decode Out Lines					
	$t_{TLH}$	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 100 80	360 180 130	ns
	$t_{THL}$	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
$f_{CL}$	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	Measured with Respect to Carry Output Line	1.0 2.5 3.0	2 5 6	MHz
$t_{WL}, t_{WH}$	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 45 35	250 90 70	ns
$t_{rCL}, t_{fCL}$	Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$			20 15 5	$\mu\text{s}$
$t_{SU}$	Minimum Clock Inhibit Data Setup Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		120 40 32	240 80 65	ns
$C_{IN}$	Average Input Capacitance			5	7.5	pF

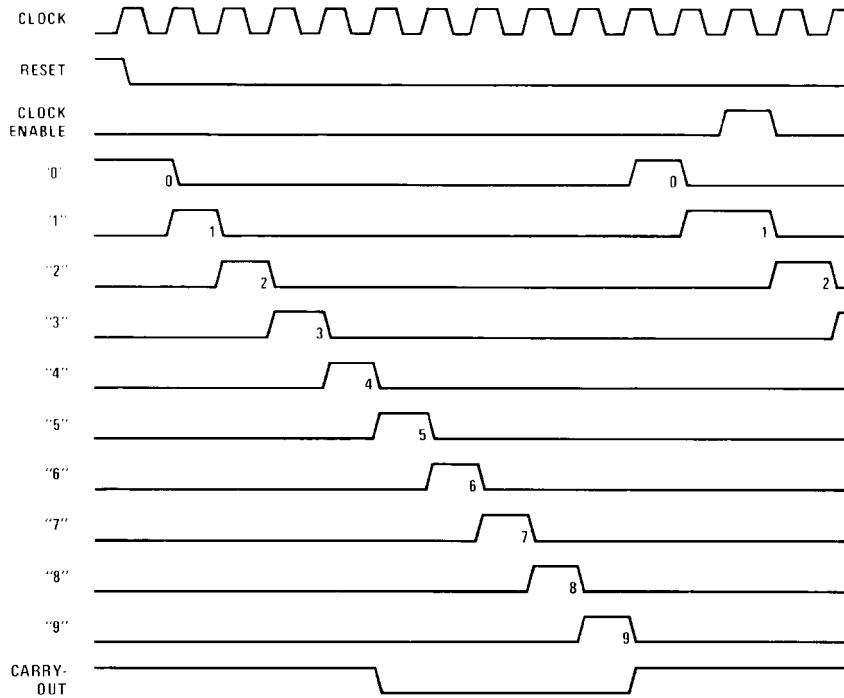
Note 4: AC Parameters are guaranteed by DC correlated testing.

**AC Electrical Characteristics** (Note 4)  
 $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}$ ,  $t_{rCL}$  and  $t_{fCL} = 20\text{ ns}$ , unless otherwise specified

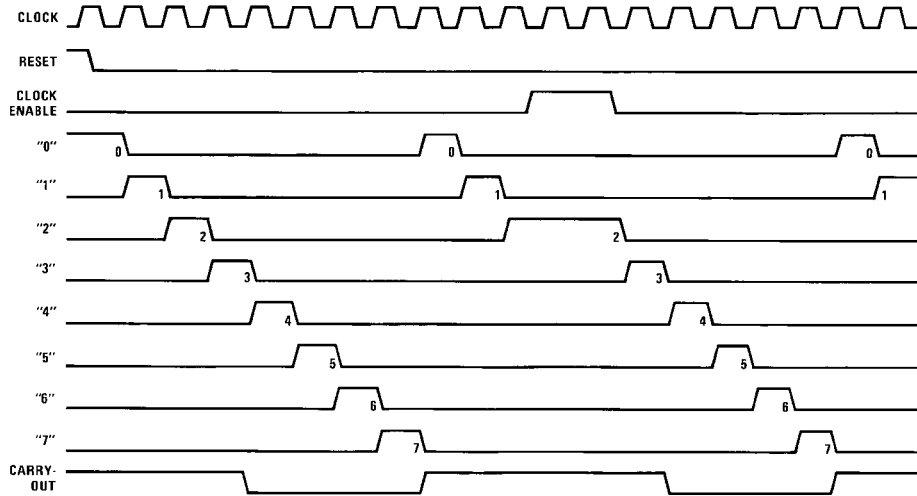
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>RESET OPERATION</b>						
$t_{PHL}, t_{PLH}$	Propagation Delay Time Carry Out Line	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		415 160 130	800 320 250	ns
	Carry Out Line	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	$C_L = 15\text{ pF}$	240 85 70	480 170 140	ns
	Decode Out Lines	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		500 200 160	1000 400 320	ns
$t_W$	Minimum Reset Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 70 55	400 140 110	ns
$t_{REM}$	Minimum Reset Removal Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		75 30 25	150 60 50	ns

Timing Diagrams

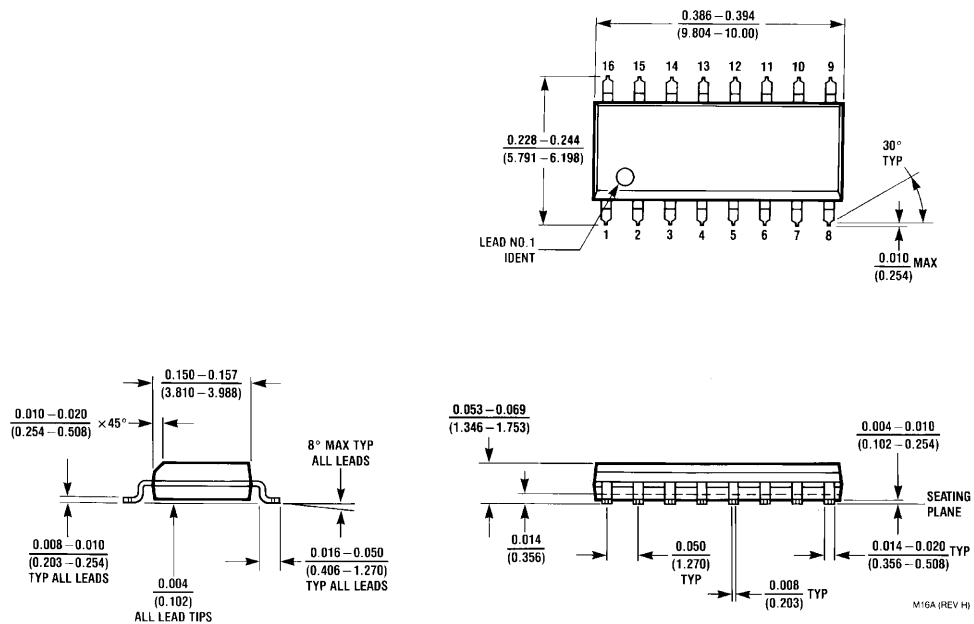
CD4017B



CD4022B

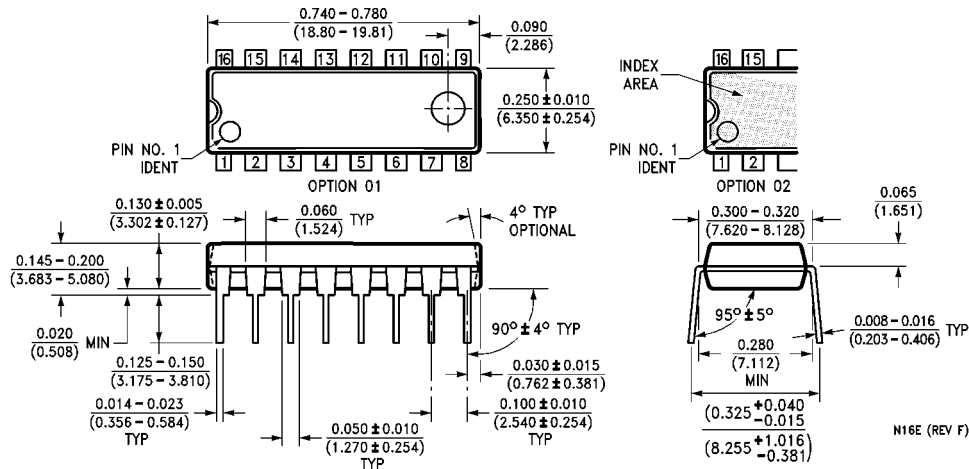


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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