8-BIT ADDRESSABLE LATCH

FEATURES

- Serial data input
- Active parallel output
- Storage register capability
- Master clear
- Can function as demultiplexer

APPLICATIONS

- Multi-line decoders
- A/D converters

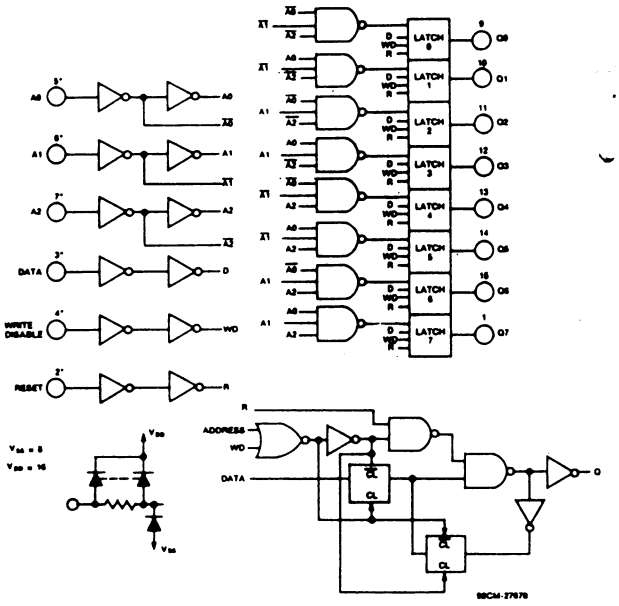
DESCRIPTION

The 4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

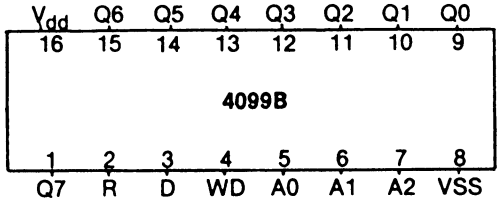
A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

LOGIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COSMOS PROTECTION NETWORK

CONNECTION DIAGRAM



TRUTH TABLE

WD	R	Addressed Latch	Unaddressed Latch
0	0	D	Holds previous data
0	1	D	0
1	0	Holds previous data	
1	1	0	0

TIMING DIAGRAMS

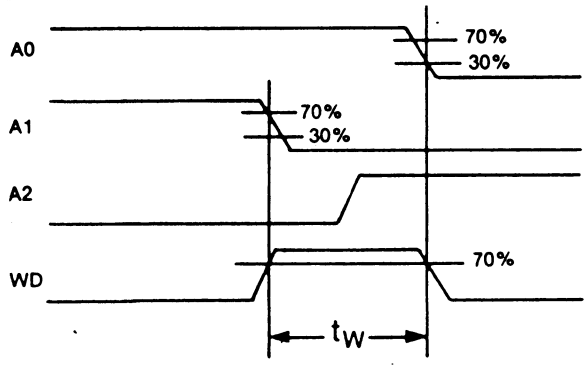


Fig.1 — Definition of WRITE DISABLE ON time.

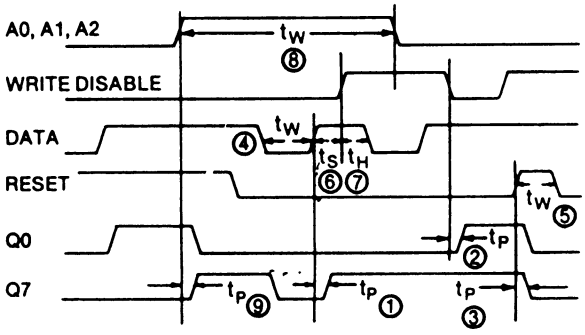


Fig. 2 — Master timing diagram.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1, 2]

PARAMETER	V_{DD}	I_{LOW2}		+25°C			T_{HIGH}		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I_{DD}	5	—	5	—	0.02	5	—	150	μA
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	

DYNAMIC CHARACTERISTICS

T_A = 25° C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 K

CHARACTERISTIC	SEE FIG 2*	V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output	(1)	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output. t_{PLH}, t_{PHL}	(2)	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	(3)	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	(9)	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, T_{THL}, (Any Output) t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	(4)	5	100	200	ns
		10	50	100	
		15	40	80	
Address	(8)	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	(5)	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	(6)	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	(7)	5	75	150	ns
		10	40	75	
		15	25	50	
Average Input Capacitance C_I	Any Input		5	—	pF

*Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 1).