Data Sheet

41KP Latched Serial Register

Benefits

- Combines functions of the LS373 and LS164 devices on a single chip
- Cost and space saving

Features

- Typical shift frequency of 35 MHz
- Asynchronous master reset
- Non-latched output for synchronous cascaded operation
- Synchronous data transfers
- Useful as input or output port for microprocessors
- TTL and CMOS compatible
- Typical power consumption of 350 mW
- Water soluble flux and total immersion cleaning compatible
- Class II ESD Protection: >500 V, <2500 V

Description

The 41KP Latched Serial Register (LSR) integrated circuit is organized as an internal connection of an 8-bit shift register, an 8-bit level-triggered latch, and an 8-bit, 3-state output driver. The latch, which may be connected to a data bus via the output driver, provides storage for an 8-bit byte within the device. The LSR effectively combines the functions of the LS164 (8-bit serial-in parallel-out shift register) and the LS373 (3-state bus-driving outputs) integrated circuits.

The 41KP LSR is designed to interface output circuits to parallel buses. Typical applications include serial-to-parallel conversion systems, data concentration, scanning and communication subsystems, data communication subsystems, digital trunk subsystems, and reduction of physical interconnection wiring in microprocessor systems. The LSR is compatible with existing parallel-to-serial registers and may be used to form an efficient data serialization system. The devices can be cascaded to produce a register that can handle multiples of 8-bit bytes. The LSR output port can be used to drive discrete circuits, LEDs, relays, logic circuits, or independent buses. The device, fabricated using LSTTL technology, is available in a 16-pin plastic DIP or SOJ package for surface mounting.

User Information

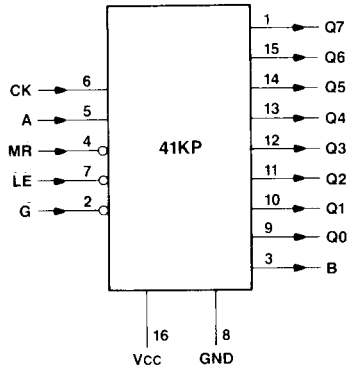


Figure 1. 41KP LSR Logic Symbol

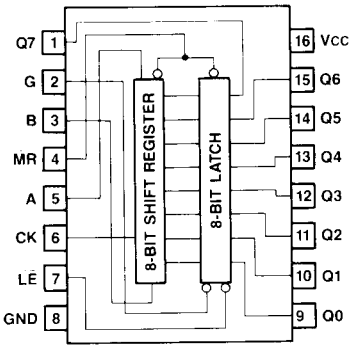


Figure 2. 41KP LSR Pin Function Diagram

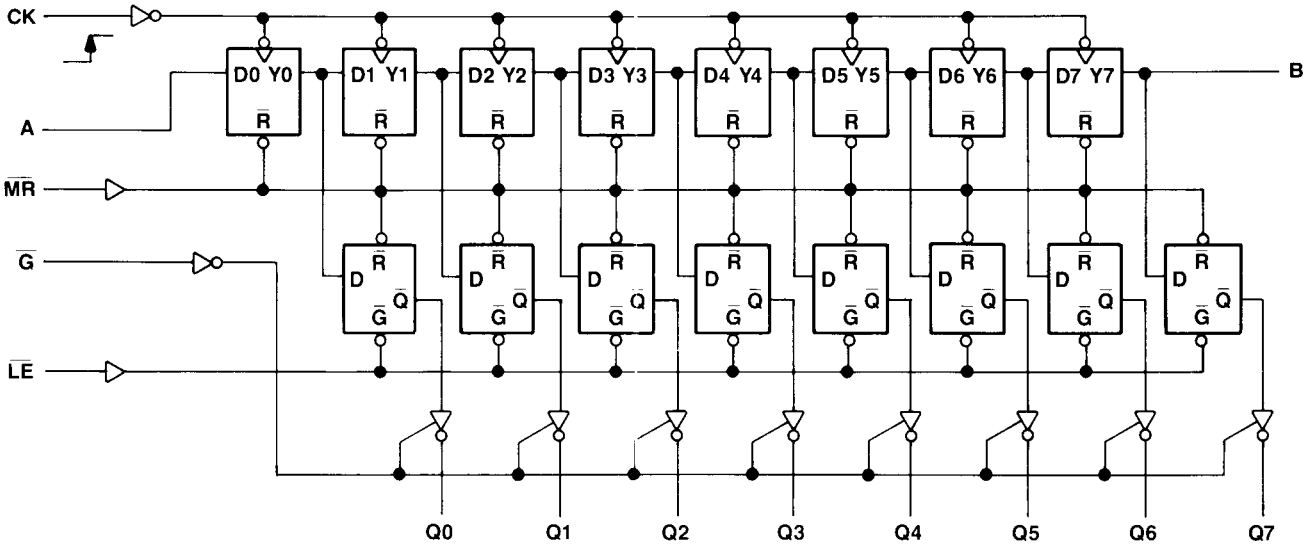


Figure 3. 41KP LSR Logic Diagram

Table 1. 41KP LSR Pin Descriptions

Pin	Symbol	Type	Name/Function
1, 9—15	Q7, Q0—Q6	O	**Parallel Data Outputs.** 8-bit parallel output port.
2	$\overline{G}$	I	**Output Enable.** This input controls the 3-state capability of the output driver. When $\overline{G}$ is low, the output pins of the 41KP LSR are in the active state and reflect the data contents of the storage latch. When $\overline{G}$ is high, the output pins of the LSR are in the high impedance state.
3	B	O	**Serial Data Output.** This output reflects the data on the output of the last or rightmost flip-flop of the shift register. The output is used to allow cascading of several LSRs in an expanded system.
4	$\overline{MR}$	I	**Master Reset.** A low at this input overrides all inputs and asynchronously clears the shift register and the storage latch. A high at this input is required for all other LSR operations.
5	A	I	**Serial Data Input.** This input accepts serial data as input to the LSR. Data on this input shifts into the first of the eight flip-flops that make up the shift register on the low-to-high transition of the clock (CK) input.
6	CK	I	**Serial Clock Input.** A low-to-high transition on this input causes data stored in the shift register to shift one place to the right.

Pin	Symbol	Type	Name/Function
7	$\overline{LE}$	I	**Latch Enable.** A high on this input causes the latch to be transparent. Data on the input to the latch (from the shift register) appears on the latch output if $\overline{LE}$ is high. When $\overline{LE}$ is low, data at the latch output remains constant regardless of the data input to the latch. In this state, the shift register data is latched, allowing a new data byte to be assembled into the shift register.
8	GND	—	**Ground.** The power and signal ground connection for the LSR.
16	V_{CC}	—	**+5 V Supply.**

Overview

The 41KP LSR effectively combines the features of serial shifting and storage into a single 16-pin, plastic DIP or SOJ. The 8-bit shift register is functionally identical to the LS164 8-bit serial-in parallel-out shift register. Serial data is entered into the shift register synchronously with a low-to-high transition of the shift register clock input. Each transition shifts data one place to the right, entering the data at D_N into Y_N just prior to transition.

The 8-bit latch is a transparent D-type. While the latch enable ($\overline{LE}$) control signal is high, the output of the latch follows the input from the shift register. When $\overline{LE}$ is low, the output of the latch is held at the current level.

The output driver features "totem-pole," 3-state outputs specifically designed for driving high-capacitive loads. The high-impedance 3-state and increased high-logic-level drive provides the LSR with the capability of being connected directly to bus-organized systems. The output port may be used to drive discrete circuits, LEDs, relays, logic circuits, or independent buses.

The latch and output driver have separate control signals to facilitate interconnection of the device within a system environment. The control signals do not affect the operation of the serial shift register. Old data can be retained while new data is being assembled in the shift register, or new data can be assembled and subsequently transferred to the storage latch while the output is in the off state.

The data that appears on the output pins is true data from the shift register. No inversion takes place from serial input to parallel output.

On power-up, the internal flip-flops of the shift register and storage latch assume a random state. Therefore, the system should assert a master reset for an initial condition.

Characteristics

Electrical Characteristics

T_A = 0 °C to 85 °C, V_{CC} = 5.0 ± 0.5 V

Parameter	Symbol	Min	Max	Unit
Input Voltages:				
Low Level	V_{IL}	—	0.7	V
High Level	V_{IH}	2.0	7.5	V
Input Clamp Diode Voltage (V_{CC} = 4.5 V, I_I = −5 mA)	V_{IK}	—	−1.5	V
Output Voltages (except B output):				
Low Level (V_{CC} = 4.5 V, V_I = 2.0 V, I_{CL} = 12 mA)	V_{OL}	—	0.4	V
Low Level (V_{CC} = 4.5 V, V_I = 2.0 V, I_{OL} = 24 mA)	V_{OL}	—	0.5	V
High Level (V_{CC} = 4.5 V, V_I = 0.7 V, I_{OH} = −3.0 mA)	V_{OH}	2.4	—	V
Output Voltages (B output):				
Low Level (V_{CC} = 4.5 V, V_I = 2.0 V, I_{CL} = 0.4 mA)	V_{OL}	—	0.4	V
Low Level (V_{CC} = 4.5 V, V_I = 2.0 V, I_{OL} = 0.8 mA)	V_{OL}	—	0.5	V
High Level (V_{CC} = 4.5 V, V_I = 0.7 V, I_{OH} = −0.1 mA)	V_{OH}	2.4	—	V
D_N Off-State Current:				
Low Level at D_N (V_{OL} = 0.3 V)	I_{OZL}	−20	20	μA
High Level at D_N (V_{OH} = 5.5 V)	I_{OZH}	−20	20	μA
Input Currents:				
Low Level (V_{CC} = 5.5 V, V_I = 0.4 V)	I_{IL}	—	−0.40	mA
High Level (V_{CC} = 5.5 V, V_I = 2.7 V)	I_{IH}	—	0.02	mA
High Level (V_{CC} = 5.5 V, V_I = 7.5 V)	I_I	—	0.1	mA
Output Short-Circuit Current (V_{CC} = 5.5 V):				
Except B Output	I_{OS}	−20	−100	mA
B Output	I_{OS}	−20	−165	mA
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	—	85	mA

Maximum Ratings

Power Supply Voltage (V_{CC}) . . . . . 7.0 Vdc
Operating Temperature Range (T_A) . . . . . 0 °C to 85 °C
Storage Temperature Range (T_{stg}) . . . . . −55 °C to +150 °C

Maximum Ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Human-Body Model ESD Threshold	
Device	**Voltage**
41KP	>500 V, <2500 V

Timing Characteristics

T_A = 25 °C, C_L = 15 pF, V_{CC} = 5.0 V

Symbol	Description	Min	Max	Unit
fmax	Maximum Clock Frequency	25	—	MHz
tPCK	Propagation Delay, Positive Clock to Output	—	59	ns
tPMR	Propagation Delay, Negative $\overline{MR}$ to Output	—	46	ns
tPLE	Propagation Delay, $\overline{LE}$ to Output	—	36	ns
tPZH	Output Enable Time to HIGH Level	—	28	ns
tPZL	Output Enable Time to LOW Level	—	36	ns
tPLZ	Output Disable Time from LOW Level	—	90	ns
tPHZ	Output Disable Time from HIGH Level	—	40	ns
tSD	Set-Up Time, A-Input to Positive Clock	15	—	ns
tHD	Hold Time, A-Input to Positive Clock	5	—	ns
tWCH	Clock Pulse Width, HIGH	20	—	ns
tWCL	Clock Pulse Width, LOW	20	—	ns
tWMR	$\overline{MR}$ Pulse Width	20	—	ns
tREC	Recovery Time, Positive $\overline{MR}$ to Positive Clock	30	—	ns
tWLE	$\overline{LE}$ Pulse Width	15	—	ns
tSLE	Set-Up Time, $\overline{LE}$ to Clock	32	—	ns
tHLE	Hold Time, $\overline{LE}$ to Clock	0	—	ns

Timing Diagrams

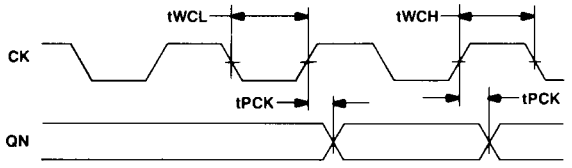


Figure 4. Propagation Delay — Clock to Output

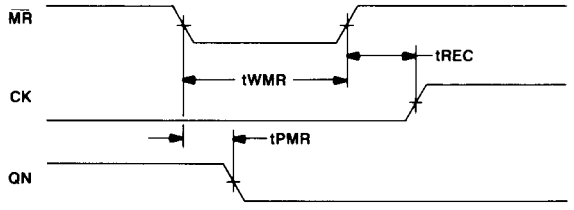


Figure 5. Propagation Delay — Negative Master Reset to Output

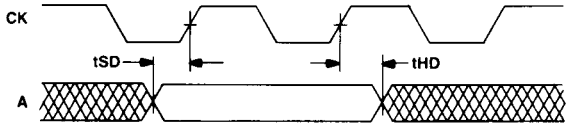


Figure 6. Set-Up and Hold Times — A Input to Positive Clock

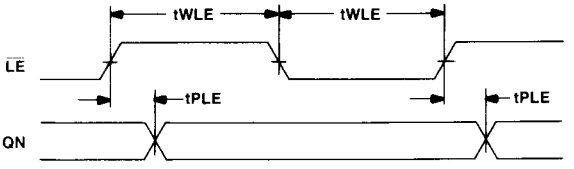


Figure 7. Propagation Delay — Latch Enable to Output

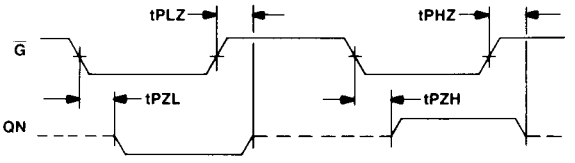


Figure 8. Propagation Delay — Output Enable to Output

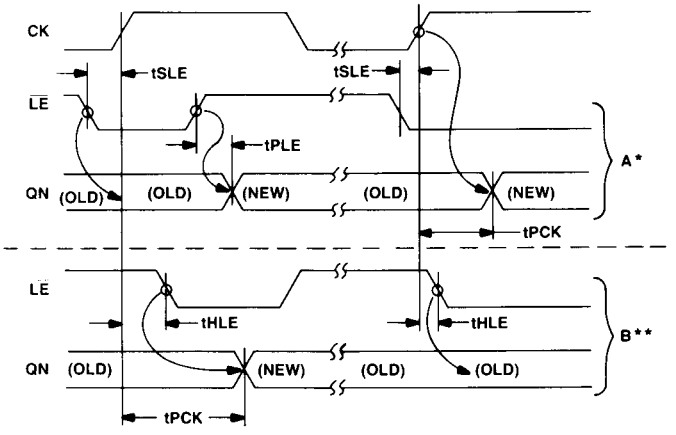


Figure 9. Set-Up Times — Clock to Latch Enable

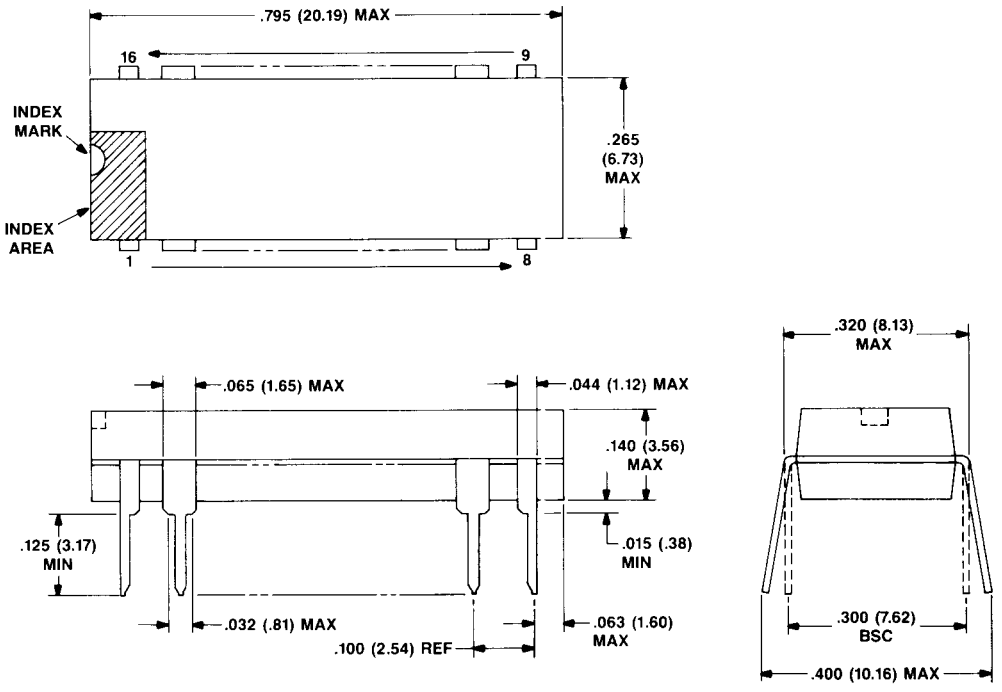
* Bracket "A" waveforms show when $\overline{LE}$ must be made low to latch current data (tSLE). This must occur prior to new data entry. If $\overline{LE}$ is made low close to the rising edge of CK, output will change reflecting new data.

** Bracket "B" waveforms show minimum time needed (tHLE) before $\overline{LE}$ may be made low to latch new data. If $\overline{LE}$ is made low too soon after rising edge of CK, old data is retained rather than entry of new data by rising edge of CK.

Outline Diagrams

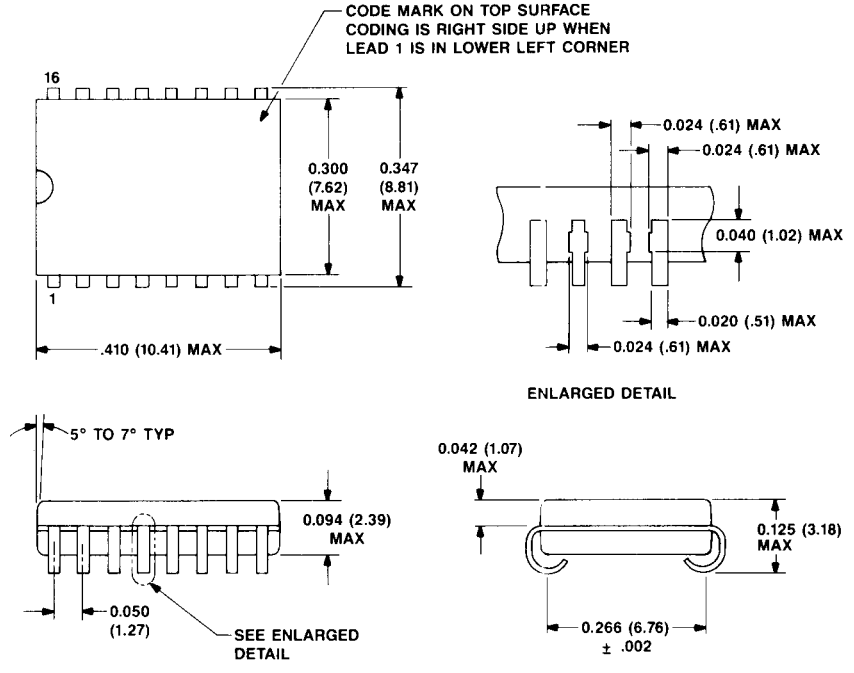
16-Pin Plastic DIP

Dimensions are in inches and (millimeters).



16-Pin Plastic SOJ, Surface Mounting

Dimensions are in inches and (millimeters).



Note: Pin numbers are shown for reference only.

Ordering Information

Device Code	Package	Comcode
41KP	16-Pin Plastic DIP	103157103
41KP-B*	16-Pin Plastic DIP	103836771

* "B" denotes burned-in devices.

Note: The 41KP LSR is available in a 16-pin SOJ. The proper code will be provided upon ordering.

For additional information, contact your AT&T Account Manager, or call:

☐ AT&T Microelectronics
Dept. 51AL230230
555 Union Boulevard
Allentown, PA 18103
1-800-372-2447

In Canada, call:
1-800-553-2448

☐ AT&T Microelectronics GmbH
Freischützstrasse 92
D-8000 Munich 81
West Germany
Tel. 0 89/95 97 0
Telex 5 216 884

☐ AT&T Microelectronics Asia/Pacific
4 Shenton Way #20-00
Shing Kwan House
Singapore 0106
Tel. 225-5233
Telex RS 42898
FAX 225-8725

☐ AT&T Microelectronics Japan
7F, Fukoku Seimei Bldg.,
2-2-2, Uchisaiwai-cho,
Chiyoda-ku, Tokyo 100 Japan
Tel. (03) 502-3055
Telex J32562 ATTIJ
FAX (03) 593-3307

July 1988

DS88-88DBIP

AT&T
The right choice.