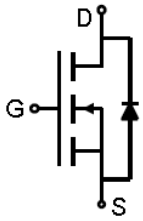
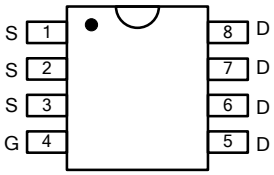
N-channel Enhancement Mode MOSFET 4512 DATASHEET

DESCRIPTION

The 4512 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.



Schematic diagram



Marking and pin assignment

GENERAL FEATURES

- RDS(ON) <16mΩ @ VGS=4.5V
  RDS(ON) <12mΩ @ VGS=10V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management

ABSOLUTE MAXIMUM RATINGS(T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	45	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current @ Continuous(Note 2)	I_D（25℃）	40	A
	I_D（100℃）	30	A
Drain Current @ Current-Pulsed (Note 1)	I_{DM}	130	A
Maximum Power Dissipation (T_A=25℃)	P_D	35	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	35	℃/W

ELECTRICAL CHARACTERISTICS (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	45			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250μA	1		2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=15A		14	16	mΩ
		V_{GS}=10V, I_D=15A		10	12	mΩ
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz		1800	2300	PF
Output Capacitance	C_{oss}			135	190	PF
Reverse Transfer Capacitance	C_{rss}			110	160	PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=15V, V_{GS}=10V,R_{GEN}=3.3Ω Ids=15A		4.5		nS
Turn-on Rise Time	t_r			9		nS
Turn-Off Delay Time	$t_{d(off)}$			32		nS
Turn-Off Fall Time	t_f			5		nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=15A,V_{GS}=4.5V		15		nC
Gate-Source Charge	Q_{gs}			4.5		nC
Gate-Drain Charge	Q_{gd}			7		nC
Body Diode Reverse Recovery Time	T_{rr}	I_F=5A, dI/dt=100A/μs		20		nS
Body Diode Reverse Recovery Charge	Q_{rr}			10		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1A		0.80	1.2	V

NOTES:

1. **Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.**
2. **$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.**

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

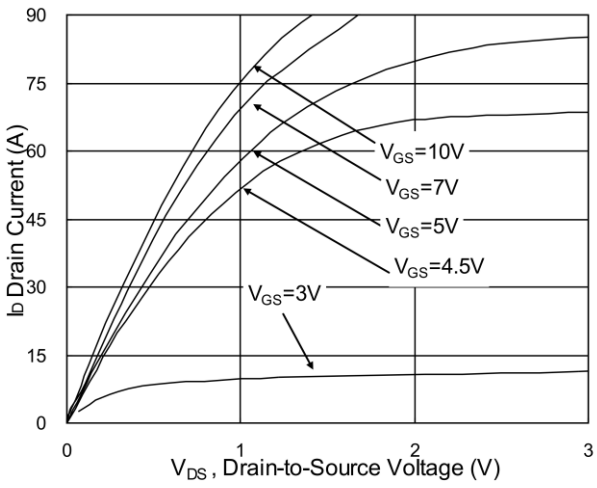


Fig.1 Typical Output Characteristics

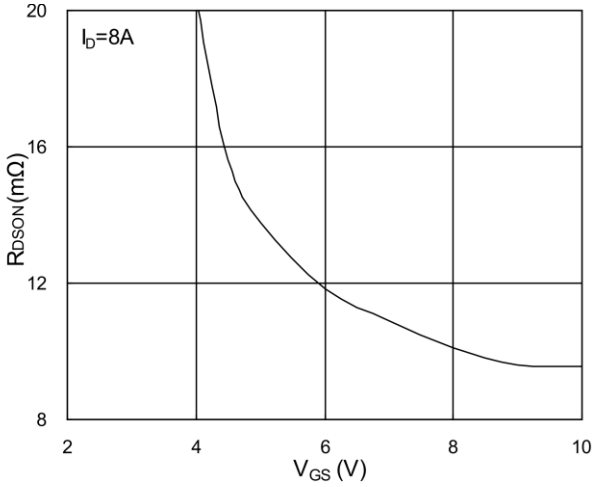


Fig.2 On-Resistance vs. G-S Voltage

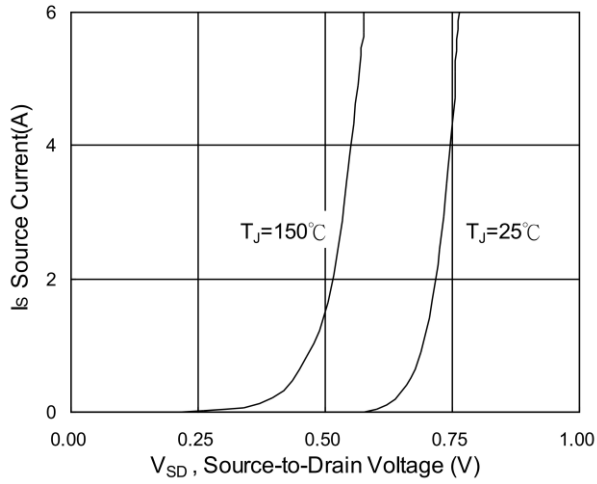


Fig.3 Forward Characteristics of Reverse

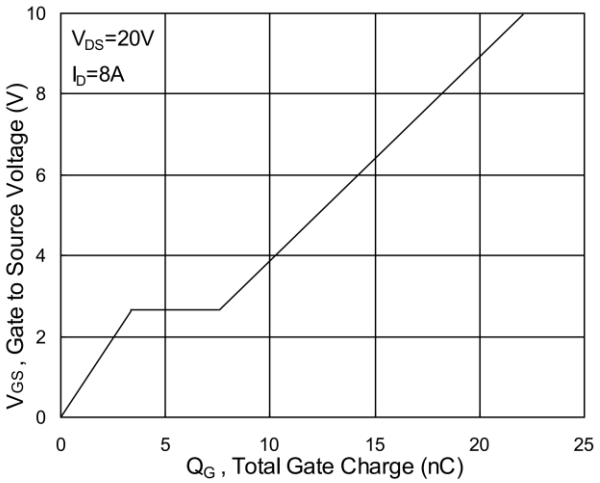


Fig.4 Gate-Charge Characteristics

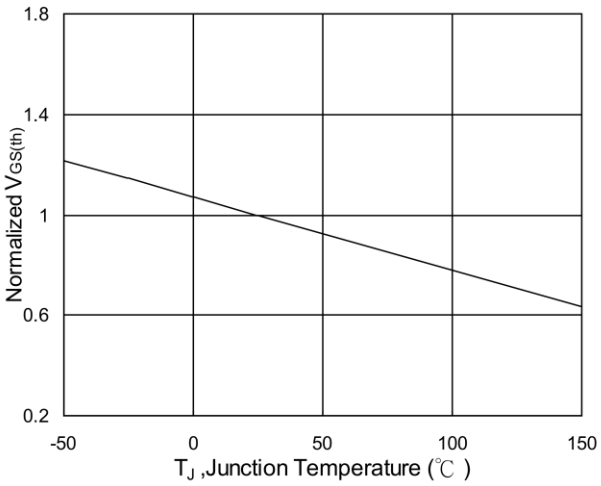


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

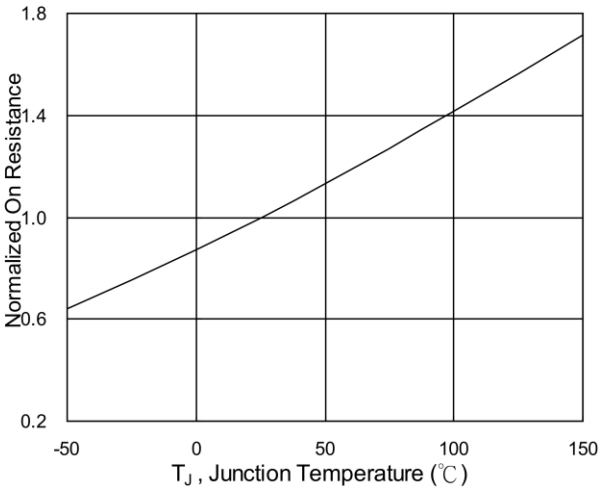


Fig.6 Normalized R_{DSON} vs. T_J

TYPIC

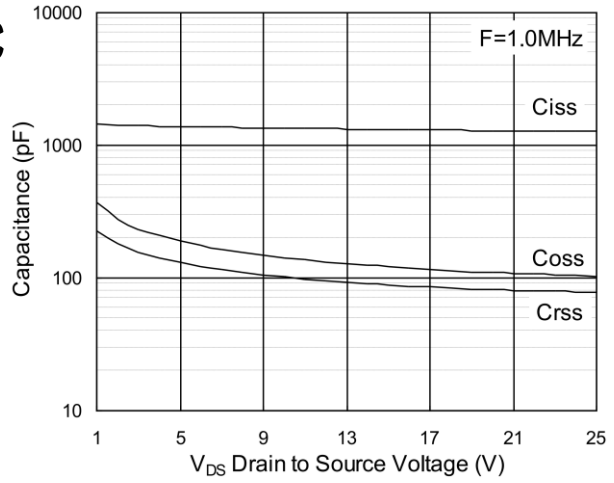


Fig.7 Capacitance

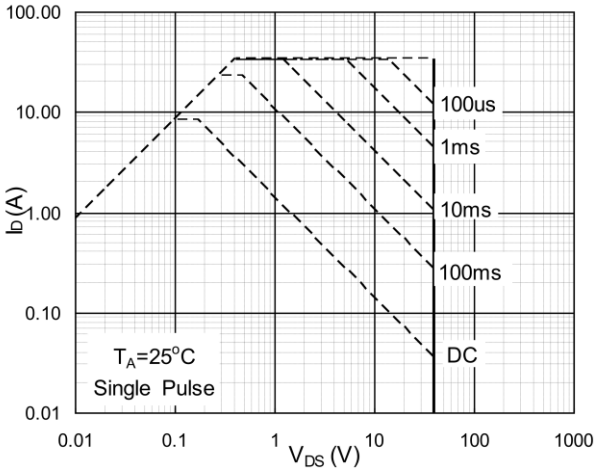


Fig.8 Safe Operating Area

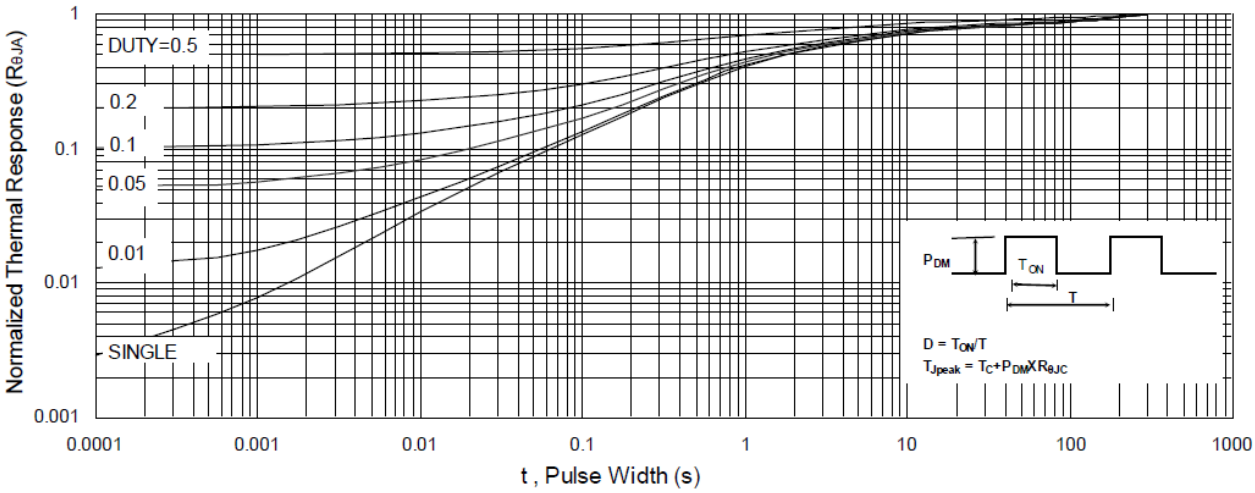


Fig.9 Normalized Maximum Transient Thermal Impedance

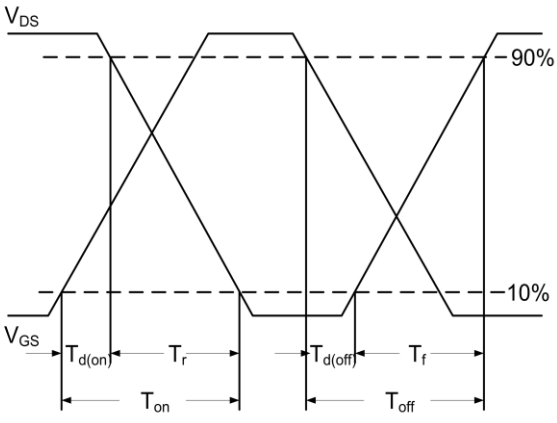


Fig.10 Switching Time Waveform

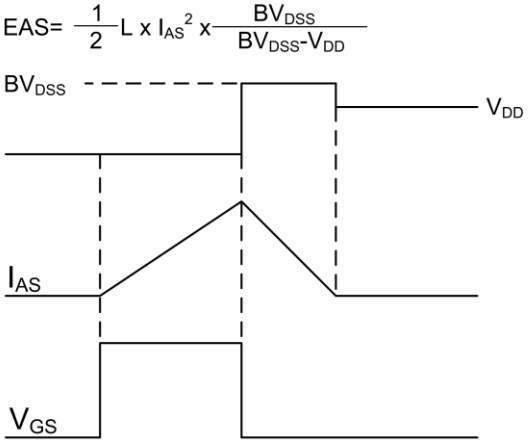
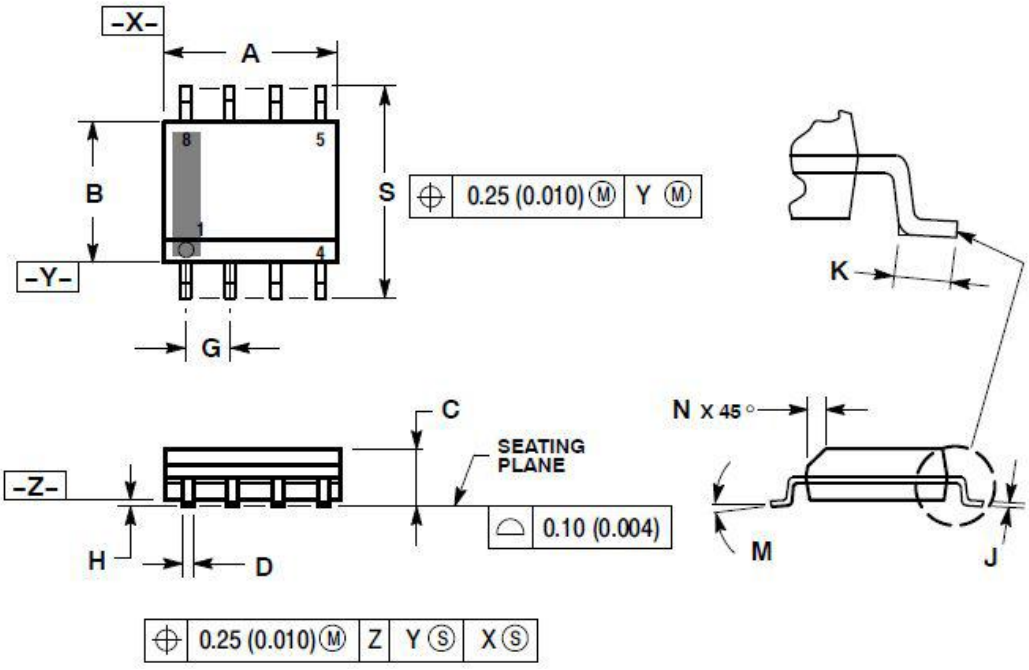


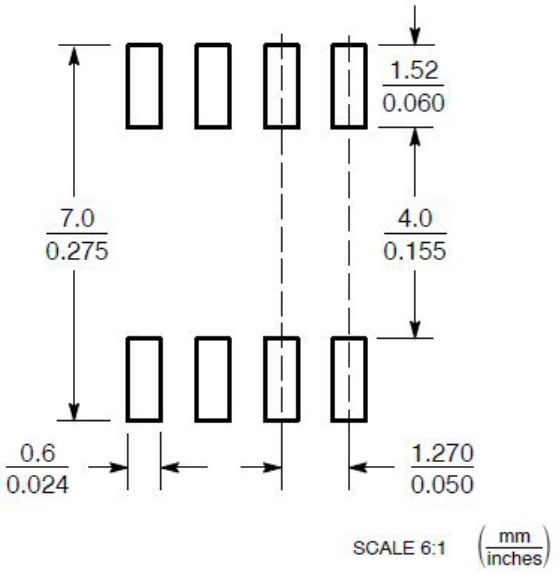
Fig.11 Unclamped Inductive Switching Waveform

Package Information

SOP-8



SOLDERING FOOTPRINT*



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244