

DESCRIPTION

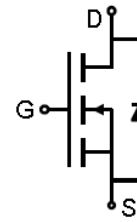
The 4515 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

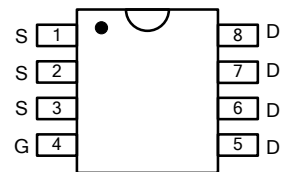
- $R_{DS(ON)} < 22m\Omega$ @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 15m\Omega$ @ $V_{GS}=10V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management



Schematic diagram



Marking and pin assignment

ABSOLUTE MAXIMUM RATINGS($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	45	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current @ Continuous (Note 2)	$I_D (25^\circ C)$	30	A
	$I_D (100^\circ C)$	20	A
Drain Current @ Current-Pulsed (Note 1)	I_{DM}	112	A
Maximum Power Dissipation ($T_A=25^\circ C$)	P_D	35	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	35	$^\circ C/W$
--	-----------------	----	--------------

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	45			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μ A
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =15A		16	22	mΩ
		V _{GS} =10V, I _D =15A		12	15	mΩ
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz		930	1350	PF
Output Capacitance	C _{oss}			135	190	PF
Reverse Transfer Capacitance	C _{rss}			110	160	PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DS} =15V, V _{GS} =10V, R _{GEN} =3.3Ω I _{DS} =15A		4.5		nS
Turn-on Rise Time	t _r			9		nS
Turn-Off Delay Time	t _{d(off)}			32		nS
Turn-Off Fall Time	t _f			5		nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =15A, V _{GS} =4.5V		15		nC
Gate-Source Charge	Q _{gs}			4.5		nC
Gate-Drain Charge	Q _{gd}			7		nC
Body Diode Reverse Recovery Time	T _{rr}	I _F =5A, dI/dt=100A/μs		20		nS
Body Diode Reverse Recovery Charge	Q _{rr}			10		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =1A		0.80	1.2	V

NOTES:

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.**
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design. R_{θJA} shown below for single device operation on FR-4 in still air.**

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

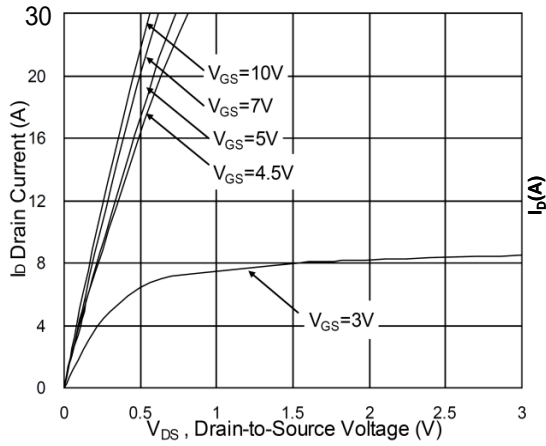


Fig.1 Typical Output Characteristics

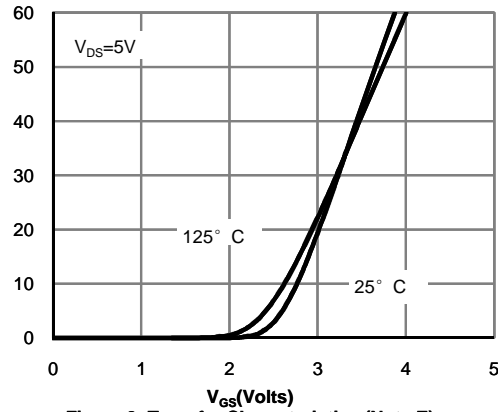


Figure 2: Transfer Characteristics (Note E)

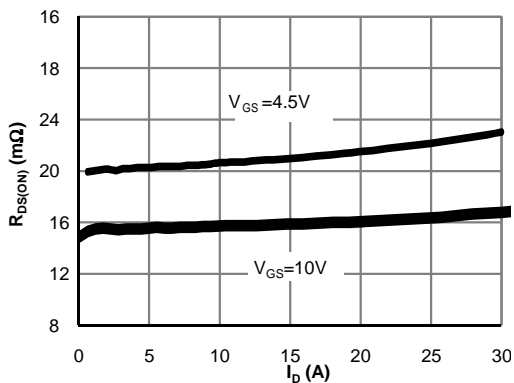


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

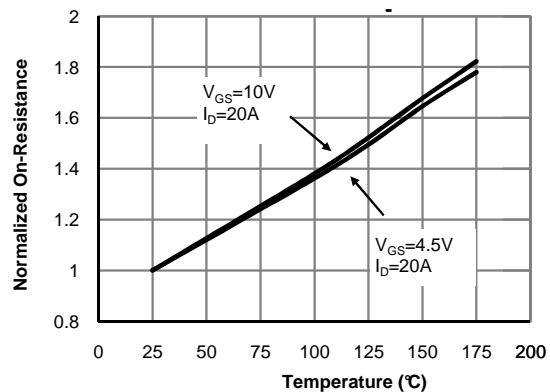


Figure 4: On-Resistance vs. Junction Temperature (Note E)

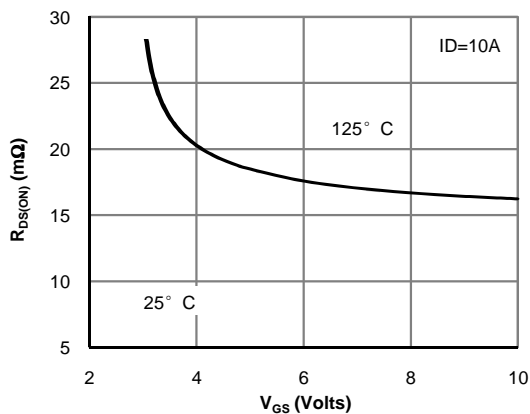


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

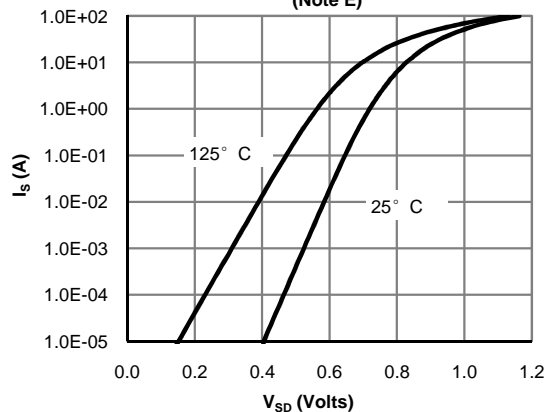


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

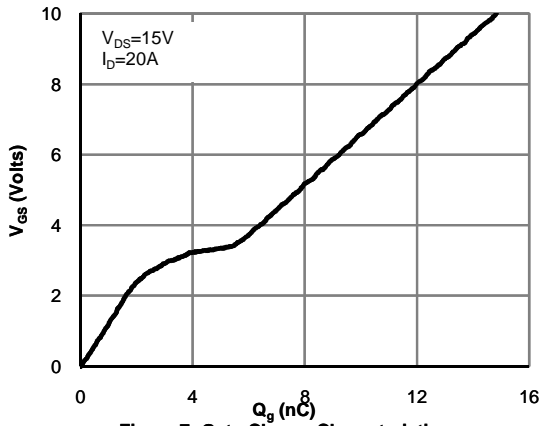


Figure 7: Gate-Charge Characteristics

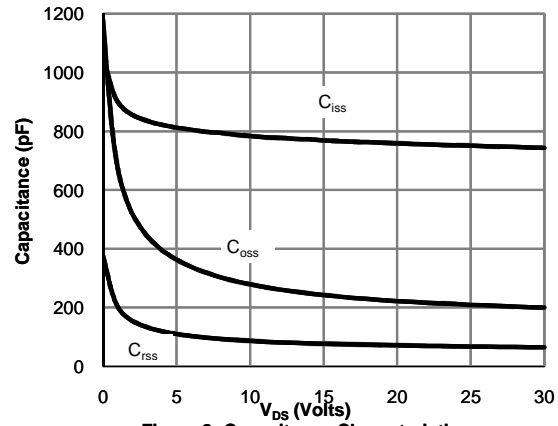


Figure 8: Capacitance Characteristics

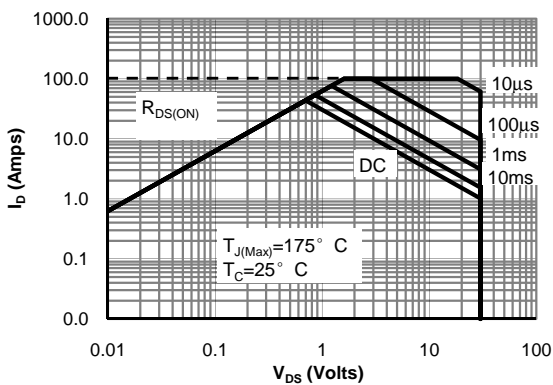


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

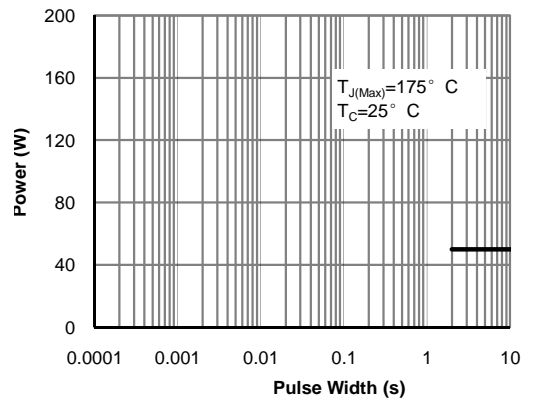


Figure 10: Single Pulse Power Rating

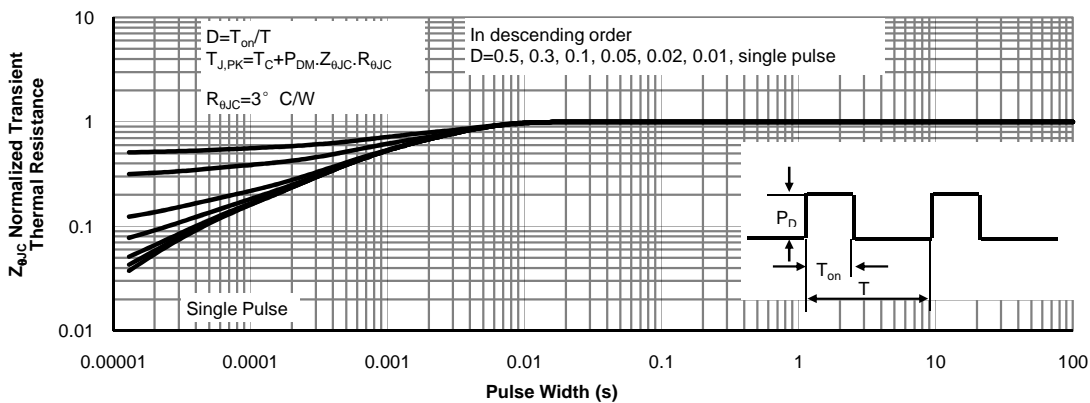


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

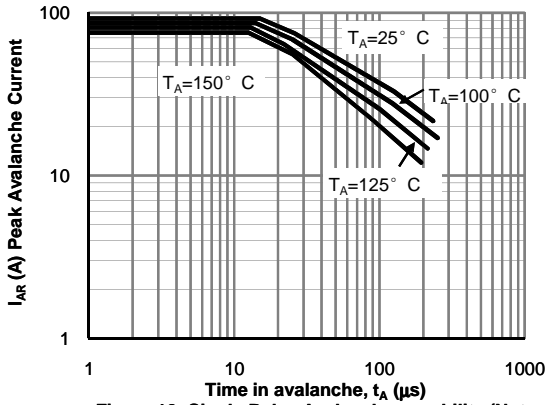


Figure 12: Single Pulse Avalanche capability (Note C)

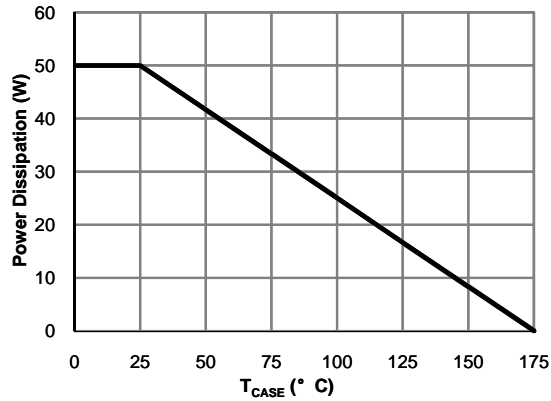


Figure 13: Power De-rating (Note F)

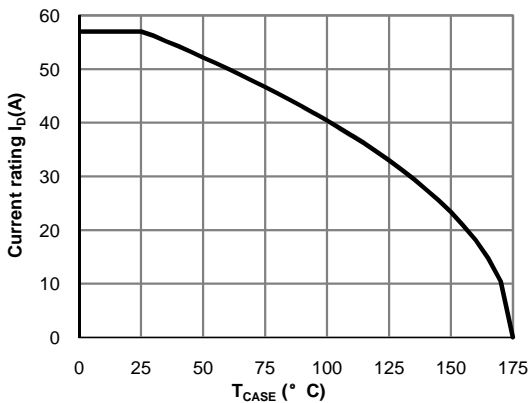


Figure 14: Current De-rating (Note F)

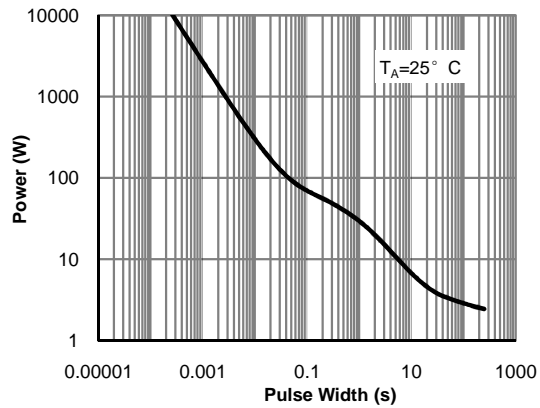


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

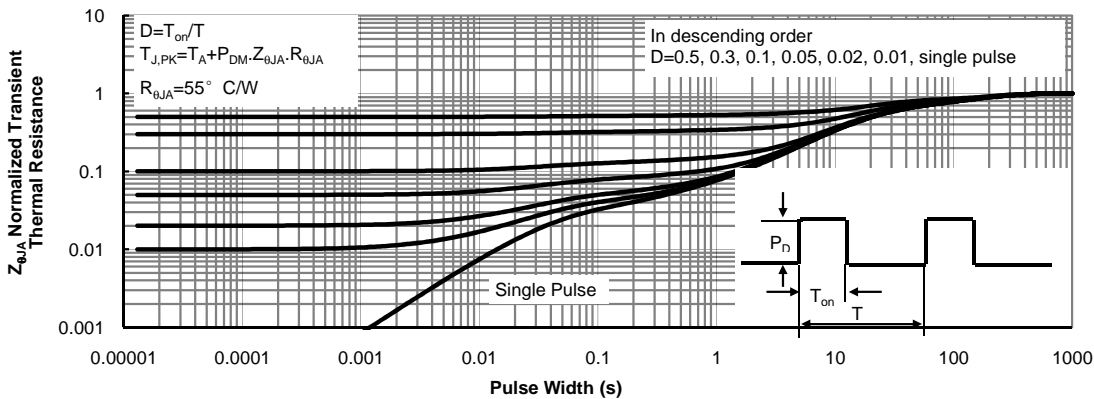
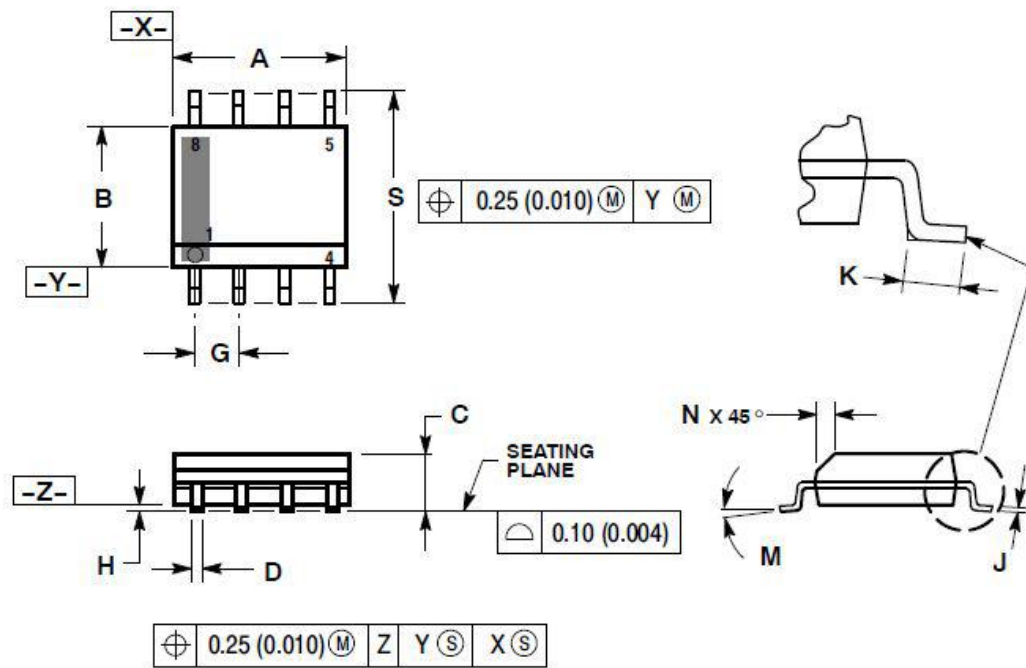


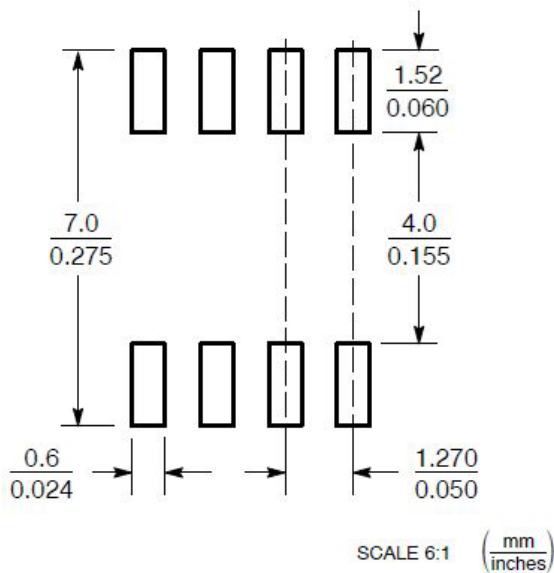
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Package Information

SOP-8



SOLDERING FOOTPRINT*



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244