CMOS BCD RATE MULTIPLIER

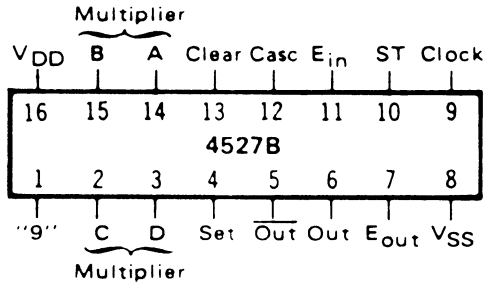
FEATURES

- Internally Synchronous for High Speed
- Strobe for Enabling or Inhibiting Outputs
- Enable and Cascade Inputs
- "9" Output Available for Cascading
- Complementary Outputs
- Clear and Set-To-Nine Inputs

DESCRIPTION

The 4527B is a BCD Digital Rate Multiplier (DRM) which provides an output pulse rate of the clock input pulse rate multiplied by 1/10 of the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. The output is clocked on the negative-going edge of the input clock. This device may be used to perform arithmetic operations, solve algebraic and differential equations, generate logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

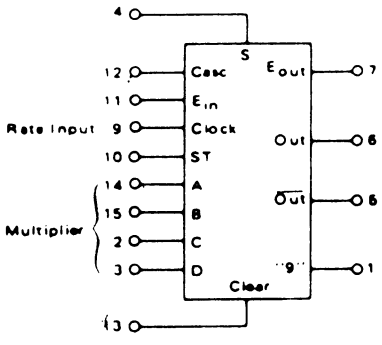
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

TRUTH TABLE

Inputs									Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	E_{IN}	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 $\overline{OUT}$	Pin 7 E_{OUT}	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

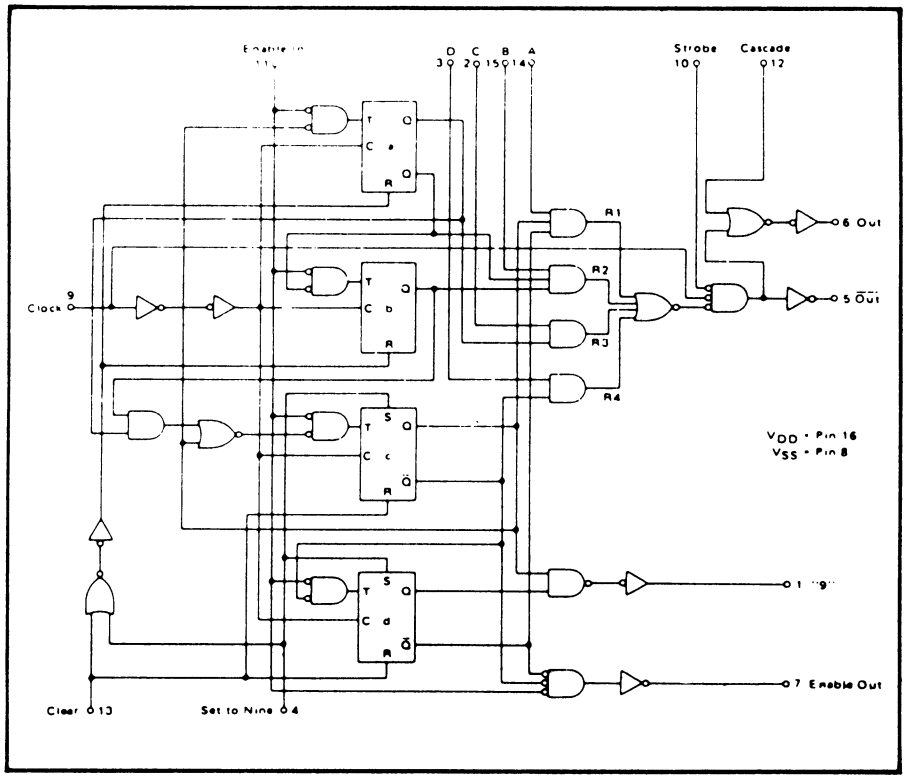
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

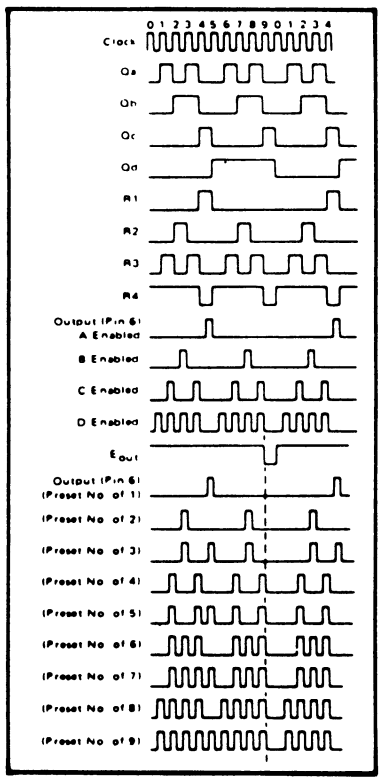
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}					
Clock to Out		5	–	150	300	ns
		10	–	75	150	
		15	–	60	120	
Clock to Out		5	–	95	190	ns
		10	–	50	100	
		15	–	35	70	
Clock to E_{out}		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Clock to "9"		5	–	300	600	ns
		10	–	125	250	
		15	–	100	200	
Cascade to Out		5	–	95	190	ns
		10	–	50	100	
		15	–	35	70	
Strobe to Out		5	–	175	350	ns
		10	–	80	160	
		15	–	60	120	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	165	330	ns
		10	–	85	170	
		15	–	65	130	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM ENABLE IN SETUP TIME	t_{setup}	5	–	175	350	ns
		10	–	60	120	
		15	–	45	90	
SET OR CLEAR OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	350	700	ns
		10	–	150	300	
		15	–	115	230	
MINIMUM SET OR CLEAR PULSE WIDTH	PW_S, PW_C	5	–	90	180	ns
		10	–	35	70	
		15	–	30	60	
SET OR CLEAR REMOVAL TIME	t_{rem}	5	–	-20	0	ns
		10	–	-10	0	
		15	–	- 7.5	0	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

LOGIC DIAGRAM



TIMING DIAGRAM

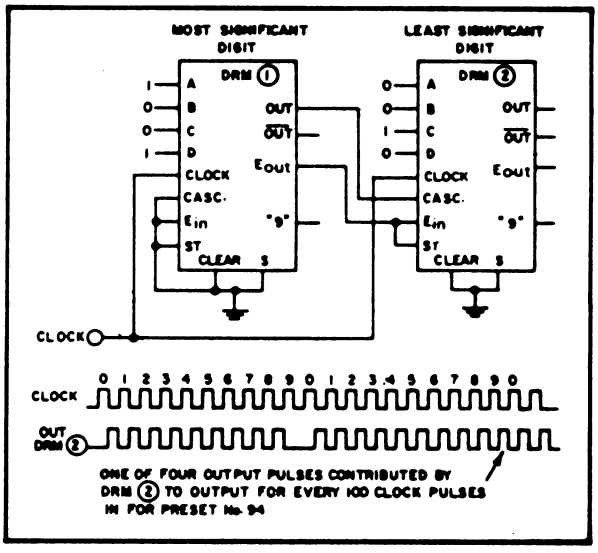


APPLICATIONS INFORMATION

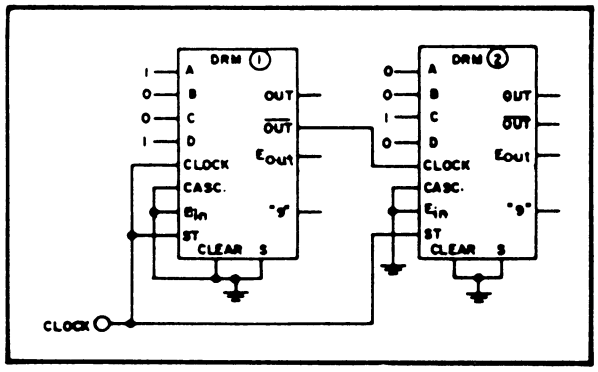
Cascading Connections

For words of more than one digit, 4527B devices may be cascaded in two different modes: an Add mode and a Multiply mode.

In the Add mode, some of the gaps left by the more significant unit at the count of 9 are filled in by the less significant units. Output Rate = Clock Rate X (0.1 BCD_1 + 0.01 BCD_2 + . . .)



Two 4527B's cascaded in the "Add" mode with a preset number of 94.



Two 4527B's cascaded in the "Multiply" mode with a preset number of 36.

In the Multiply mode, the fraction programmed into the first DRM is multiplied by the fraction programmed into the second one.

$$\text{Output Rate} = \text{Clock Rate} \times \frac{BCD_1}{10} \times \frac{BCD_2}{10} \times \ldots$$

APPLICATIONS INFORMATION

Multiplication of Two Variables

$R_1 = f_{CLK} (\frac{A}{10})$

$R_2 = f_{CLK} (\frac{A}{10}) (\frac{B}{10}) = f_{CLK} (\frac{AB}{100})$

$R_3 = f_{CLK} (\frac{N}{10})$

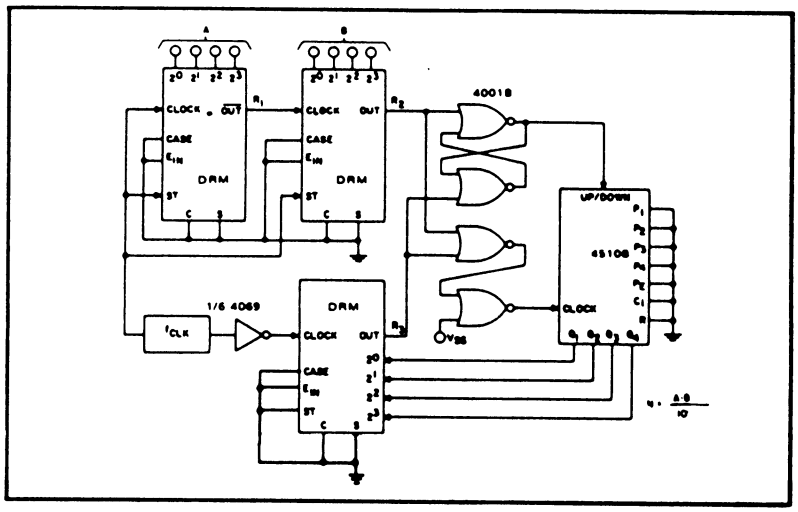
R_2 addresses "up" count, R_3 addresses "down" count. The interface circuit converts to a single clock with mode control. When loop stabilizes,

$R_2 = R_3$

$f_{CLK} (\frac{AB}{100}) = f_{CLK} (\frac{N}{10})$

or $N = \frac{AB}{10}$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Generation of $A^{2/3}$

$R_1 = f_{CLK} (\frac{A^2}{100}) (\frac{1}{10}) = f_{CLK} (\frac{A^2}{1000})$

$R_2 = f_{CLK} (\frac{N^3}{1000})$

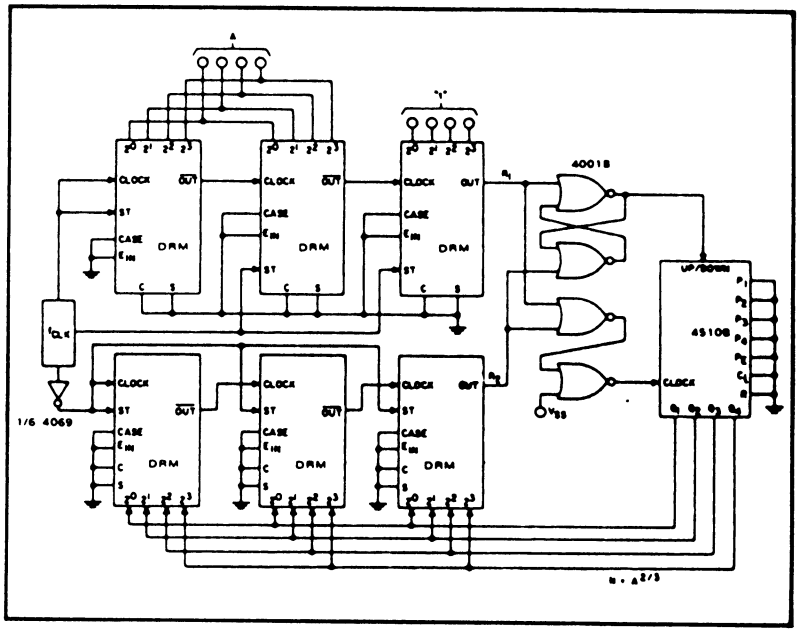
At equilibrium,

$R_1 = R_2$

$N^3 = A^2$

or $N = A^{2/3}$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Frequency Ratios

$R_1 = f_1/10^n$

$R_2 = f_2N/10^n$ where n = number of stages

At equilibrium,

$R_1 = R_2$

$N = f_1/f_2$

Note: To prevent simultaneous commands (overlap), f_1 and f_2 may require preconditioning.