

CMOS 4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- ◆ Function and Pinout Equivalent to 74181
- ◆ Provides 16 Logic Functions and 16 Arithmetic Functions
- ◆ Comparator Function
- ◆ Positive or Negative Logic
- ◆ Full Look-Ahead for High-Speed Operations on Long Words

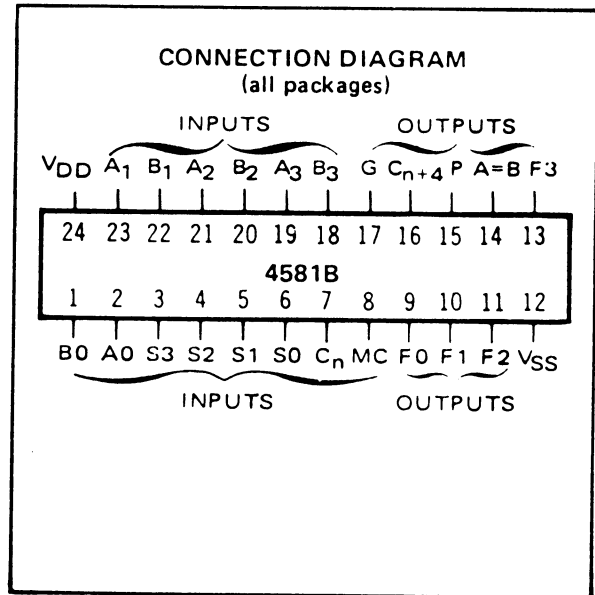
DESCRIPTION

The 4581B is a CMOS 4-Bit Arithmetic Logic Unit (ALU) capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the Mode Control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the Select inputs (S0 thru S3) with the Mode Control input high, while the desired arithmetic operation is selected by applying a low voltage to the Mode Control input, the required level to Carry in, and the appropriate word to the Select inputs. The Word inputs and Function outputs can be operated with either active-high or active-low data.

Carry propagate (P) and Carry generate (G) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the 4582B as a second-order look-ahead block. An inverted Ripple-Carry input (C_n) and a Ripple-Carry output (C_{n+4}) are included for ripple-through operation.

ALU SIGNAL DESIGNATIONS

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
MC	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output

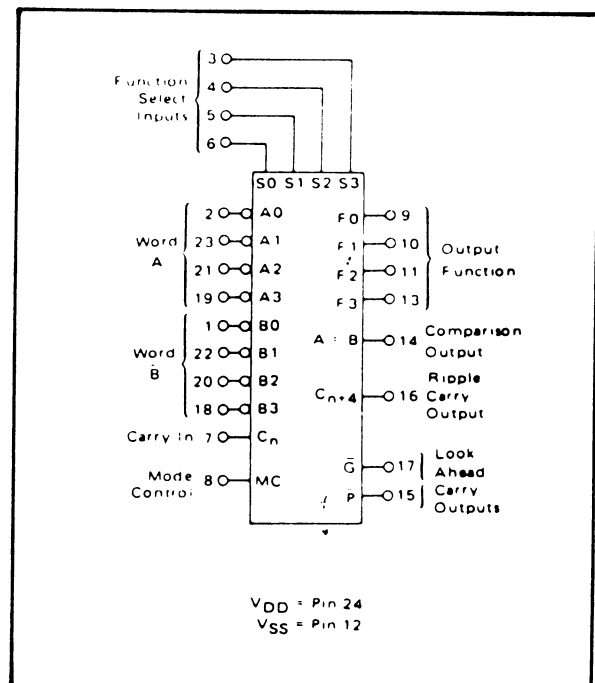


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I _{DD}	5	V _{IN} = V _{SS} or V _{DD} All valid input combinations	-	5	-	0.05	5	-	150	μA _{dc}
	10		-	10	-	0.1	10	-	300	
	15		-	20	-	0.2	20	-	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

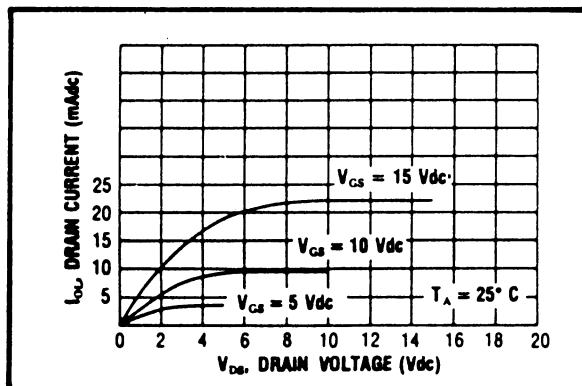
² T_{LOW} = -55°C for C
 = -40°C for E
 T_{HIGH} = +125°C for C
 = +85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units		
PROPAGATION DELAY TIME Sum In to Sum Out	t _{PLH, tPHL}	5	-	400	800	ns		
			10	-	160		320	
			15	-	120		240	
		Sum In to Sum Out (Logic Mode)		5	-	380	760	ns
				10	-	190	380	
				15	-	160	320	
		Sum In to A = B		5	-	450	900	ns
				10	-	275	550	
				15	-	225	450	
		Sum In to P̄ or Ḡ		5	-	300	600	ns
				10	-	150	300	
				15	-	125	250	
		Sum In to C _{n+4}		5	-	300	600	ns
				10	-	150	300	
				15	-	125	250	
		Carry In to Sum Out		5	-	200	400	ns
				10	-	100	50	
				15	-	70	35	
		Carry In to C _{n+4}		5	-	200	400	ns
				10	-	100	50	
				15	-	70	35	
		OUTPUT TRANSITION TIME	t _{TLH, tTHL}	5	-	100	200	ns
				10	-	50	100	
				15	-	40	80	

AC Test Setup Reference Table

TEST	AC PATHS		DC DATA INPUTS		MODE
	INPUTS	OUTPUTS	TO V _{SS}	TO V _{DD}	
Sum _{in} to Sum _{out} Delay Time	A0	Any F̄	Remaining A's C _n	All B's	Add
Sum _{in} to P̄ Delay Time	A0	P	Remaining A's C _n	All B's	Add
Sum _{in} to Ḡ Delay Time	B0	C _{n+4}	All A's C _n	Remaining B's	Add
Sum _{in} to C _{n+4} Delay Time	B0	Ḡ	All A's C _n	Remaining B's	Add
C _n to Sum _{out} Delay Time	C _n	Any F̄	All A's	All B's	Add
C _n to C _{n+4} Delay Time	C _n	C _{n+4}	All A's	All B's	Add
Sum _{in} to A = B Delay Time	A0	A = B	All B's Remaining A's	C _n	Sub
Sum _{in} to Sum _{out} Delay Time (Logic Mode)	All B's	Any F̄	All A's	M	Exclusive OR



Typical N-Channel Sink Current Characteristics

ALU FUNCTION GENERATION

The 4581B can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

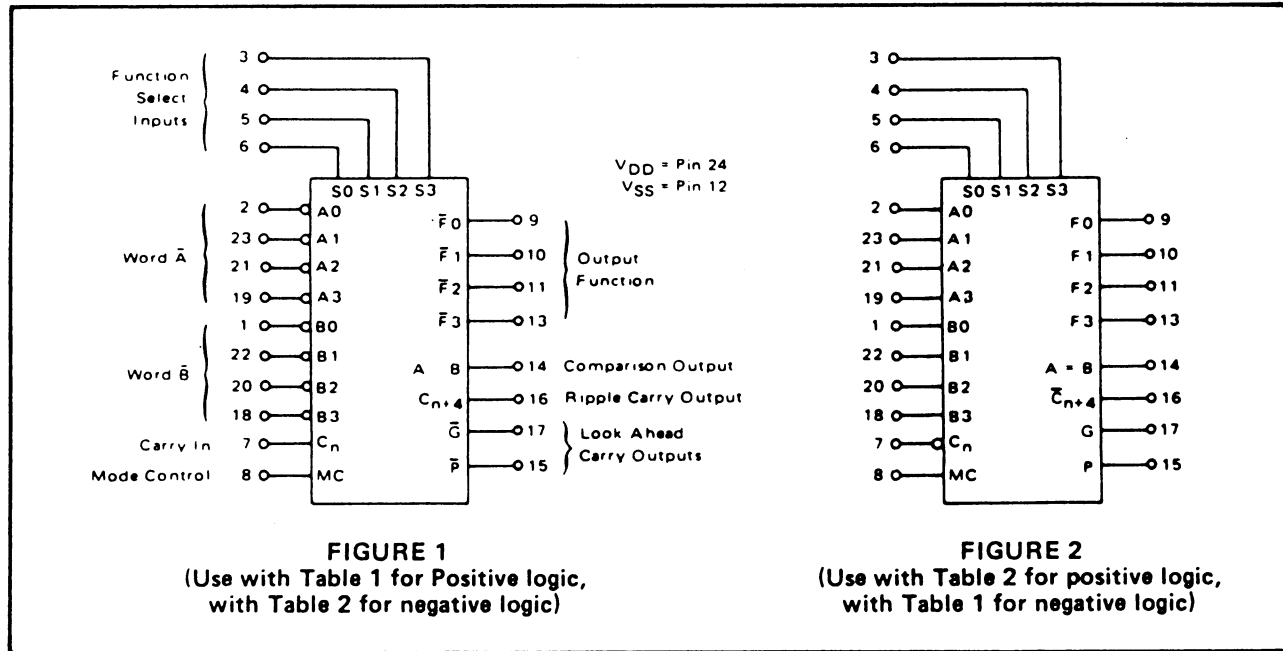


FIGURE 1
(Use with Table 1 for Positive logic,
with Table 2 for negative logic)

FIGURE 2
(Use with Table 2 for positive logic,
with Table 1 for negative logic)

TABLE 1

SELECTION					ACTIVE-LOW DATA		
					MC = H	MC = L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC	C _n = L	C _n = H	
					FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = \bar{A}	F = A MINUS 1	F = A	
L	L	L	H	F = $\bar{A}\bar{B}$	F = AB MINUS 1	F = AB	
L	L	H	L	F = $\bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$	
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO	
L	H	L	L	F = $\bar{A} + \bar{B}$	F = A PLUS (A + \bar{B})	F = A PLUS (A + \bar{B}) PLUS 1	
L	H	L	H	F = \bar{B}	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1	
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B	
L	H	H	H	F = A + \bar{B}	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
H	L	L	L	F = $\bar{A}\bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1	
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1	
H	L	H	L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1	
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1	
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1	
H	H	L	H	F = $\bar{A}\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1	
H	H	H	L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1	
H	H	H	H	F = A	F = A	F = A PLUS 1	

TABLE 2

SELECTION					ACTIVE-HIGH DATA		
					MC = H	MC = L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC	C _n = H	C _n = L	
					FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = \bar{A}	F = A	F = A PLUS 1	
L	L	L	H	F = $\bar{A} + \bar{B}$	F = A + B	F = (A + B) PLUS 1	
L	L	H	L	F = $\bar{A}\bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1	
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO	
L	H	L	L	F = $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1	
L	H	L	H	F = \bar{B}	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1	
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B	
L	H	H	H	F = $\bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$	
H	L	L	L	F = $\bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1	
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1	
H	L	H	L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1	
H	L	H	H	F = AB	F = AB MINUS 1	F = AB	
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1	
H	H	L	H	F = A + \bar{B}	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1	
H	H	H	L	F = A + B	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1	
H	H	H	H	F = A	F = A MINUS 1	F = A	

* Each bit is shifted to the next more significant position.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the A and B inputs is provided using the A=B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	C _n	C _{n+4}	Magnitude
Active High	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active Low	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

APPLICATIONS INFORMATION

ADDITION REQUIREMENTS

Number of Bits	Package Count		Carry Method Between ALU's
	Arithmetic/Logic Units	Look-Ahead Carry Generators	
1 to 4	1		None
5 to 8	2		Ripple
9 to 16	3 or 4	1	Full Look-Ahead
17 to 64	5 to 16	2 to 5	Full Look-Ahead

EXPANSION TECHNIQUES

