

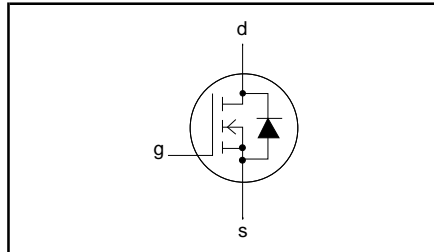
# TrenchMOS™ transistor Logic level FET

PHP45N03LT

## FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

## SYMBOL



## QUICK REFERENCE DATA

$V_{DSS} = 30\text{ V}$
$I_D = 45\text{ A}$
$R_{DS(ON)} \leq 24\text{ m}\Omega (V_{GS} = 5\text{ V})$
$R_{DS(ON)} \leq 21\text{ m}\Omega (V_{GS} = 10\text{ V})$

## GENERAL DESCRIPTION

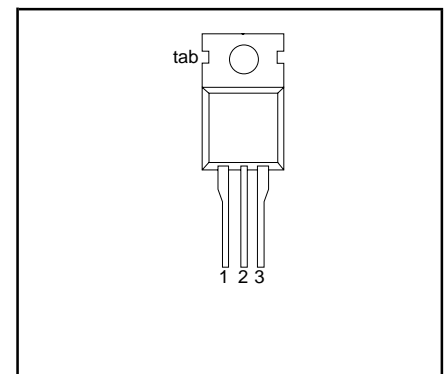
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP45N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.

## PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

## SOT78 (TO220AB)



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	30	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$I_D$	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	45	A
$I_D$	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	36	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	180	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	86	W
$T_{stg}, T_j$	Storage & operating temperature	-	-55	175	$^\circ\text{C}$

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA; T <sub>j</sub> = -55°C	30 27	- -	- -	V V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA T <sub>j</sub> = 175°C T <sub>j</sub> = -55°C	1 0.5 -	1.5 - -	2 - 2.3	V V V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175°C	- -	0.05 -	10 500	μA μA
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±5 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175°C	- - -	20 16 -	24 21 45	mΩ mΩ mΩ

### DYNAMIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 25 A	8	16	-	S
Q <sub>g(tot)</sub>	Total gate charge	I <sub>D</sub> = 40 A; V <sub>DD</sub> = 24 V; V <sub>GS</sub> = 5 V	-	23	-	nC
Q <sub>gs</sub>	Gate-source charge		-	3	-	nC
Q <sub>gd</sub>	Gate-drain (Miller) charge		-	12	-	nC
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	2000	2500	pF
C <sub>oss</sub>	Output capacitance		-	380	450	pF
C <sub>rss</sub>	Feedback capacitance		-	250	300	pF
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 25 A;	-	30	45	ns
t <sub>r</sub>	Turn-on rise time	V <sub>GS</sub> = 5 V; R <sub>G</sub> = 5 Ω	-	80	130	ns
t <sub>d off</sub>	Turn-off delay time	Resistive load	-	95	135	ns
t <sub>f</sub>	Turn-off fall time		-	40	55	ns
L <sub>d</sub>	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L <sub>d</sub>	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>DR</sub>	Continuous reverse drain current		-	-	45	A
I <sub>DRM</sub>	Pulsed reverse drain current		-	-	180	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V I <sub>F</sub> = 40 A; V <sub>GS</sub> = 0 V	- -	0.95 1.0	1.2 -	V V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 40 A; -di <sub>F</sub> /dt = 100 A/μs;	-	52	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = -10 V; V <sub>R</sub> = 25 V	-	0.08	-	μC

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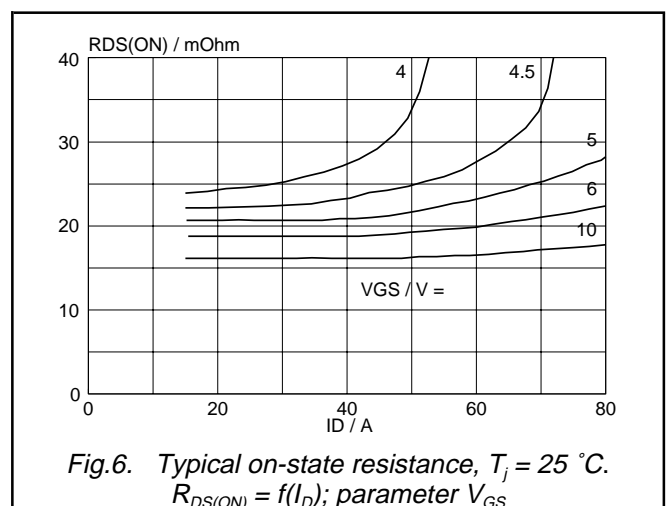
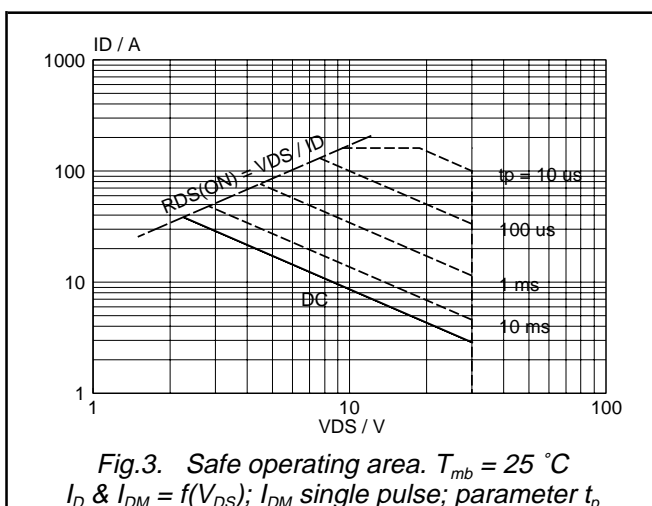
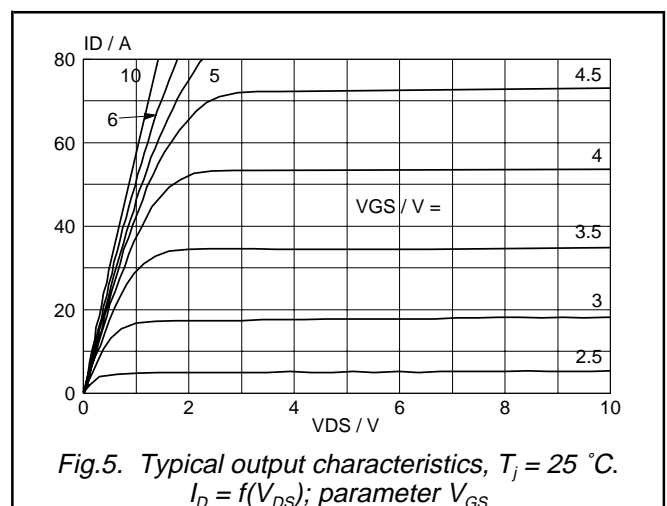
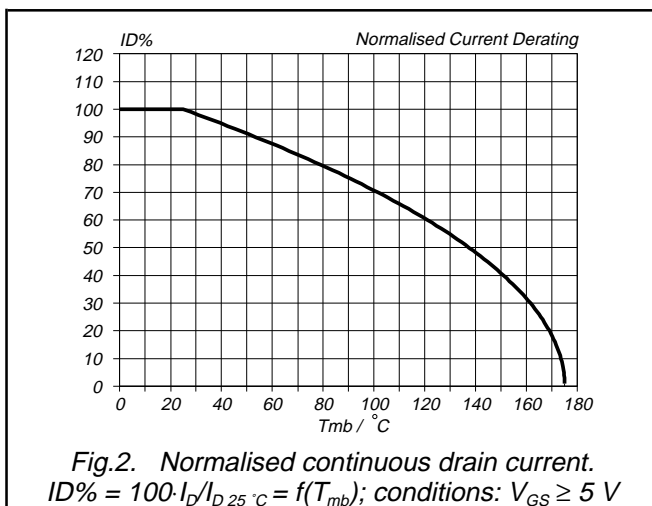
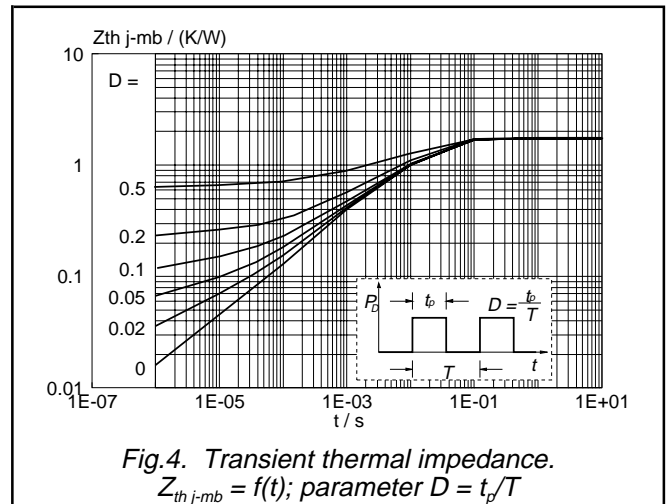
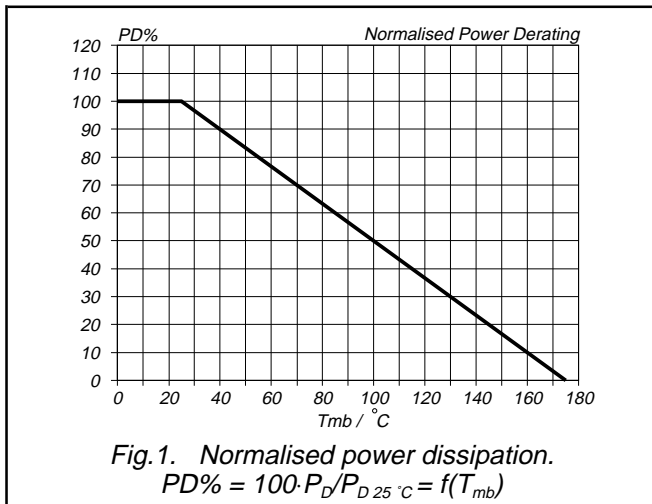
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**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 25 \text{ A}; V_{DD} \leq 25 \text{ V};$ $V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega; T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	60	mJ

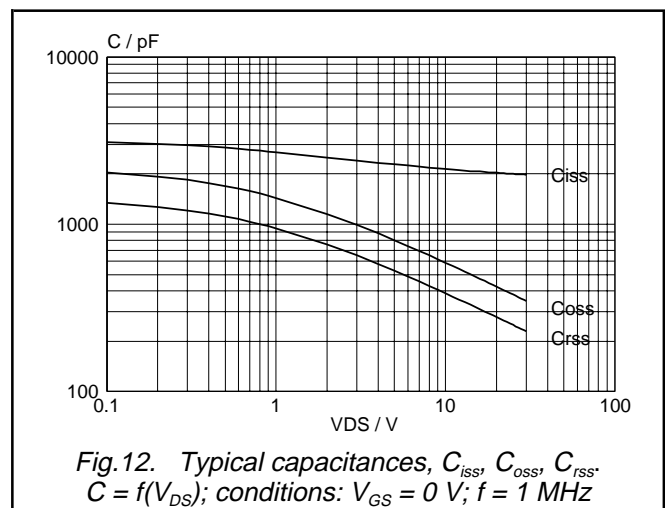
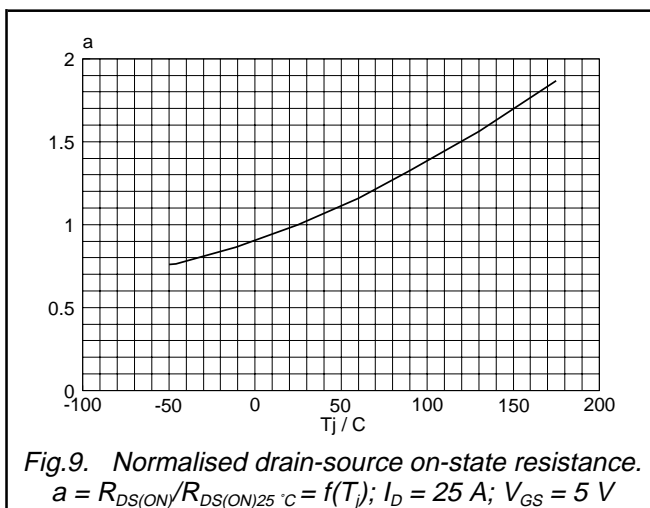
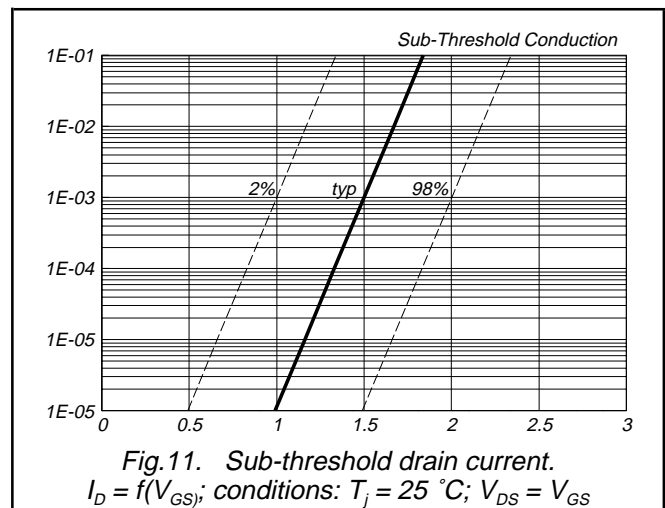
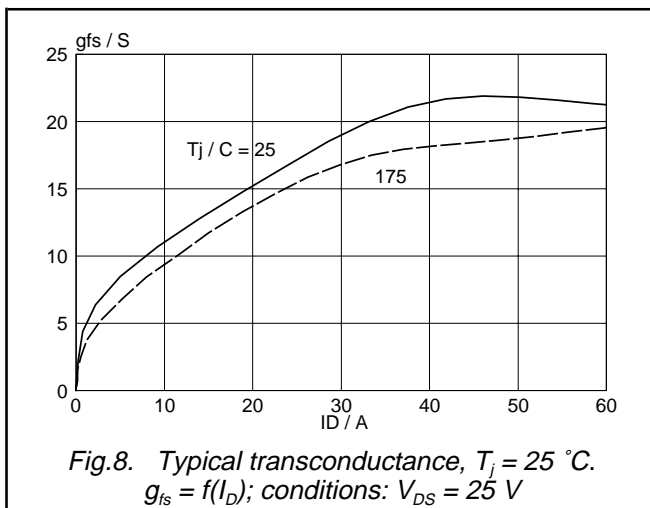
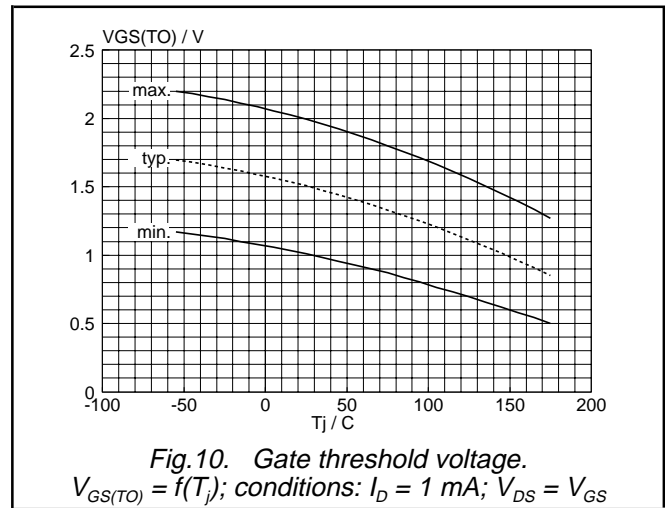
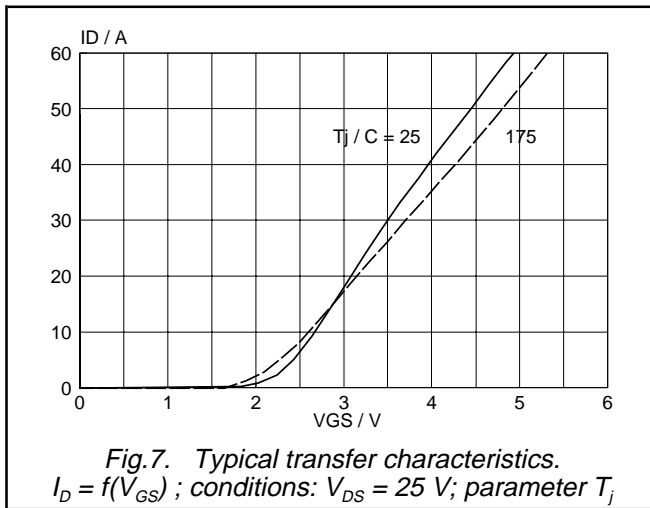
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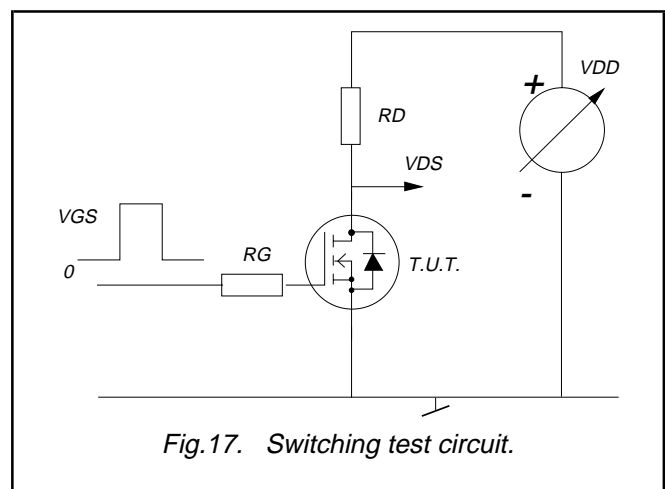
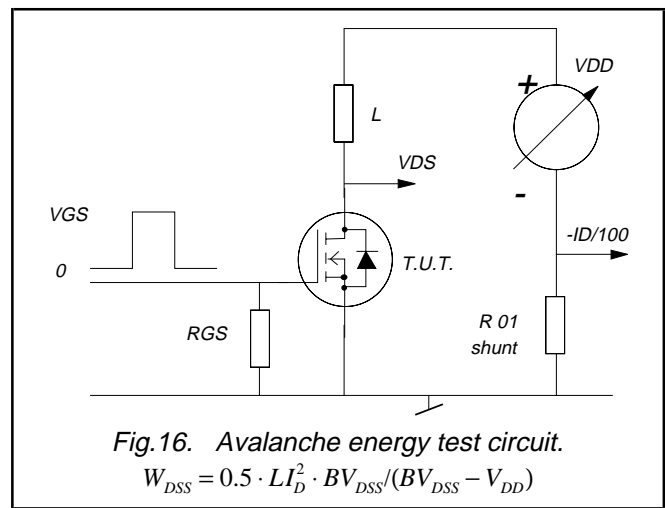
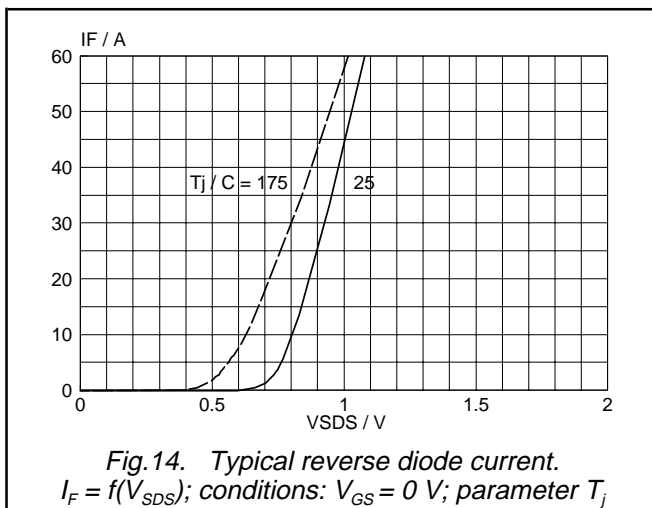
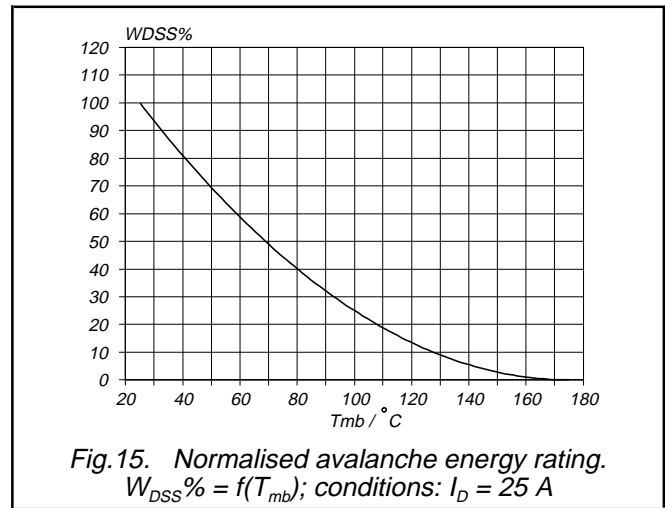
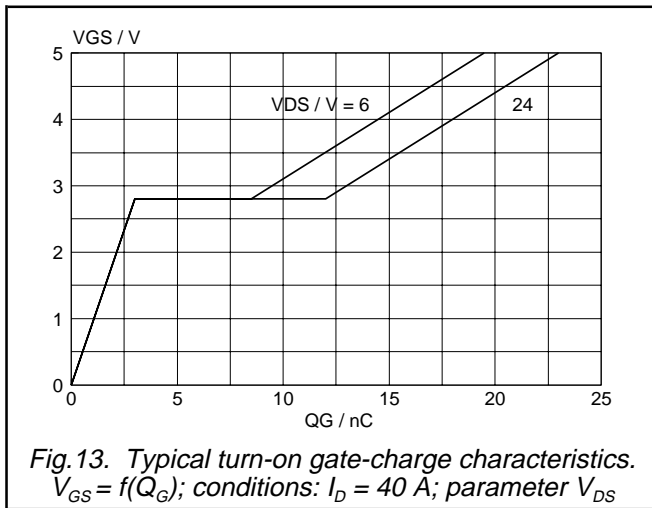
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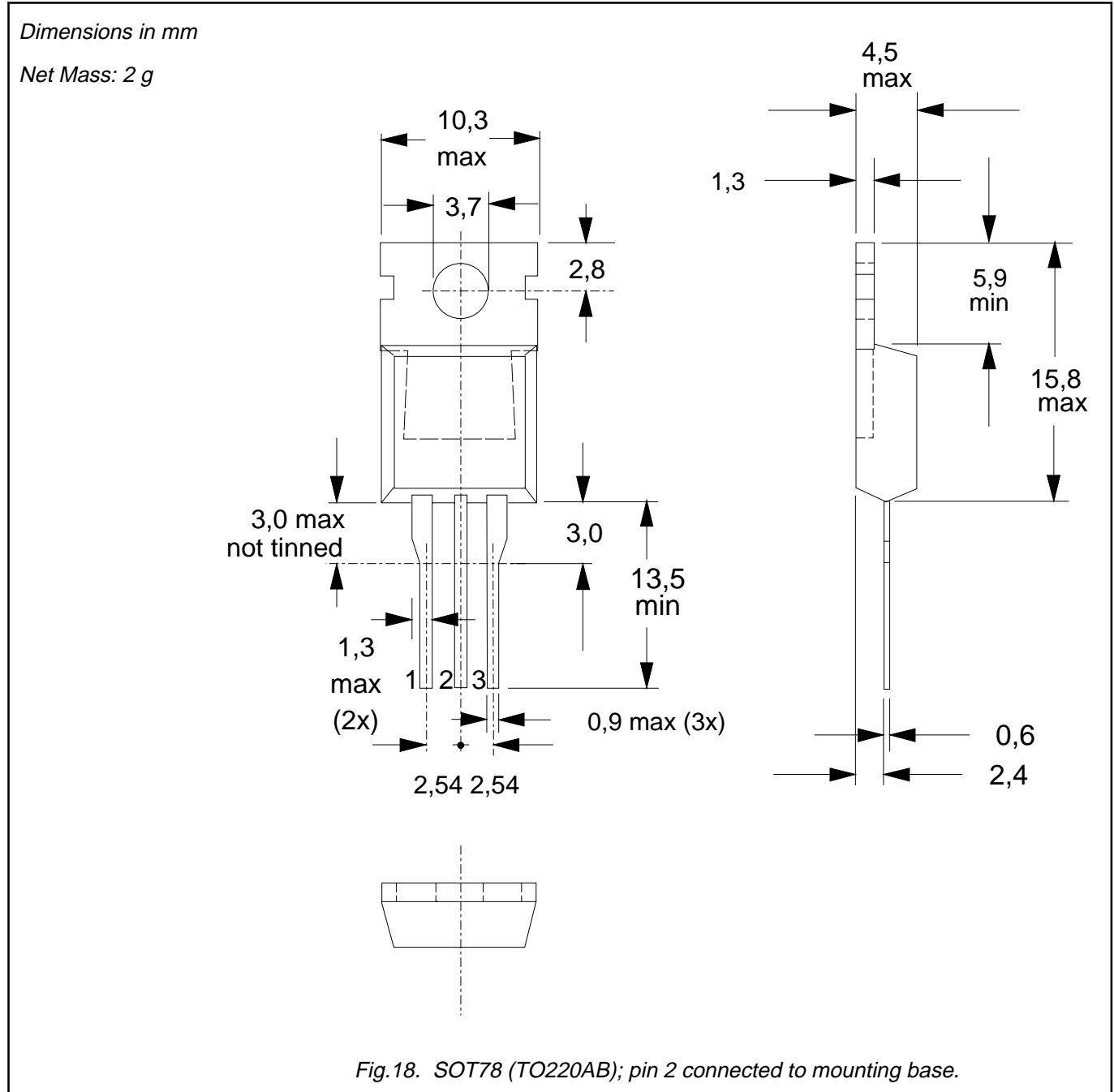
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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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