

4AK26

Silicon N-Channel Power MOS FET Array

HITACHI

Application

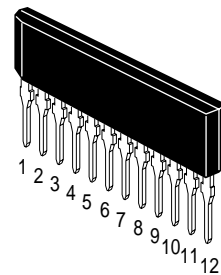
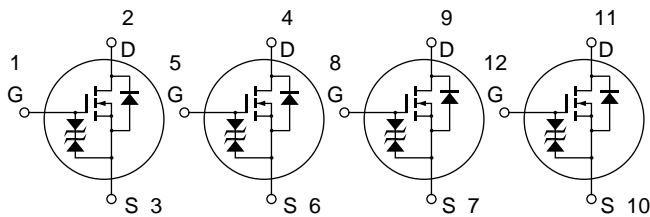
High speed power switching

Features

- Low on-resistance
 $R_{DS(on)} \leq 0.06$, $V_{GS} = 10$ V, $I_D = 5$ A
 $R_{DS(on)} \leq 0.075$, $V_{GS} = 4$ V, $I_D = 5$ A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for motor driver and solenoid driver and lamp driver

Outline

SP-12



1, 5, 8, 12. Gate
2, 4, 9, 11. Drain
3, 6, 7, 10. Source

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_{D}	10	A
Drain peak current	$I_{\text{D(pulse)}}^{*1}$	32	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch ($T_c = 25^\circ\text{C}$)*2	28	W
Channel dissipation	Pch^{*2}	4	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

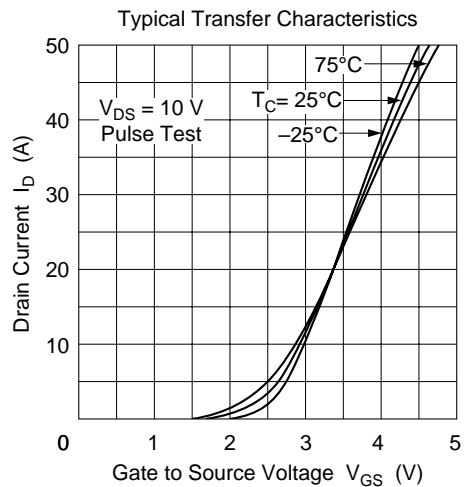
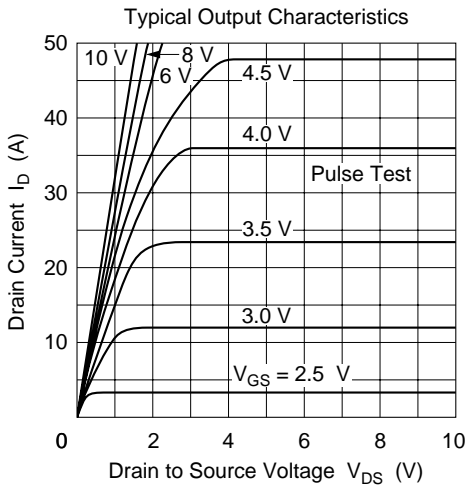
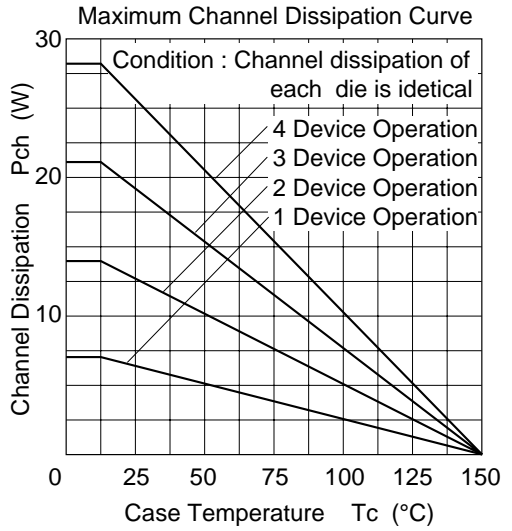
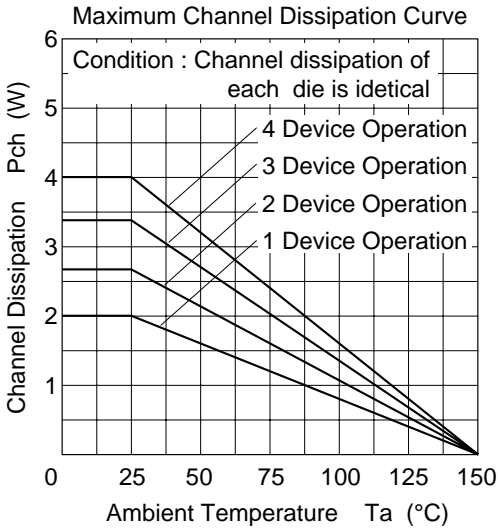
Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. 4 Devices operation

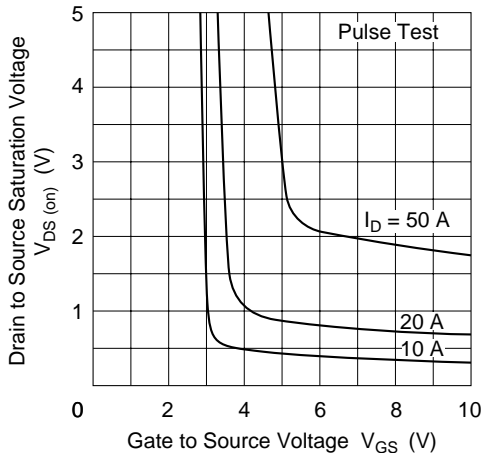
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.045	0.06	Ω	$I_D = 5 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
		—	0.056	0.075	Ω	$I_D = 5 \text{ A}$ $V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	10	12	—	S	$I_D = 5 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	1400	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	720	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	220	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 10 \text{ A}$
Rise time	t_r	—	95	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	300	—	ns	$R_L = 3 \text{ }\Omega$
Fall time	t_f	—	170	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.05	—	V	$I_F = 10 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	110	—	μs	$I_F = 10 \text{ A}$, $V_{GS} = 0$, $dI_F/dt = 50 \text{ A}/\mu\text{s}$

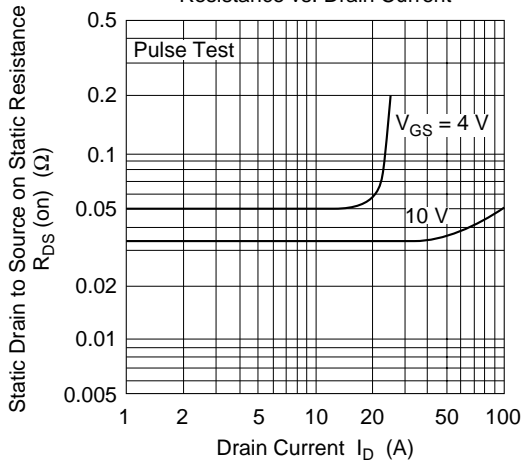
Note: 1. Pulse Test



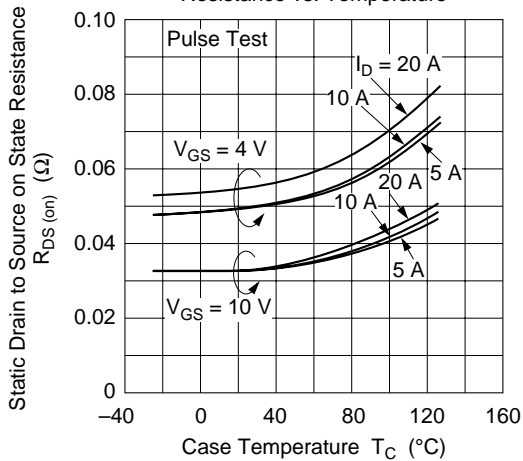
Drain to Source Saturation Voltage vs. Gate to Source Voltage



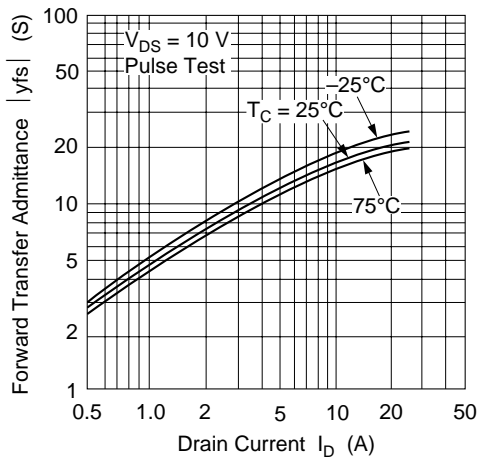
Static Drain to Source on State Resistance vs. Drain Current



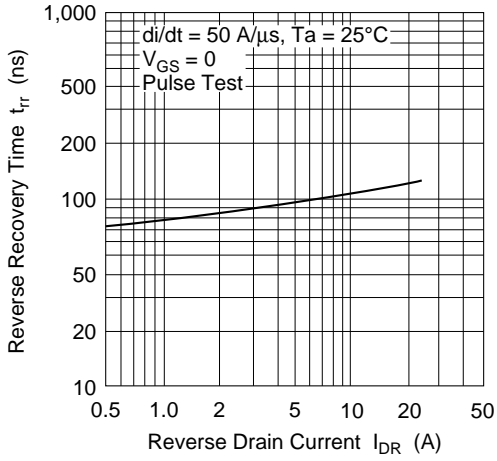
Static Drain to Source on State Resistance vs. Temperature



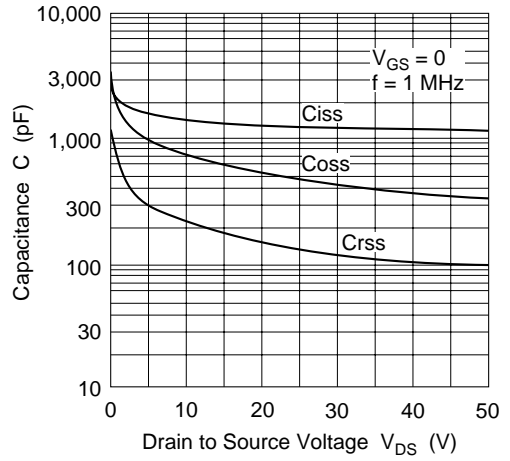
Forward Transfer Admittance vs. Drain Current



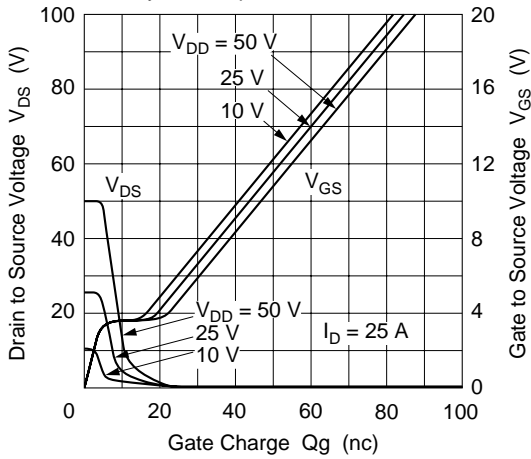
Body to Diode Reverse Recovery Time



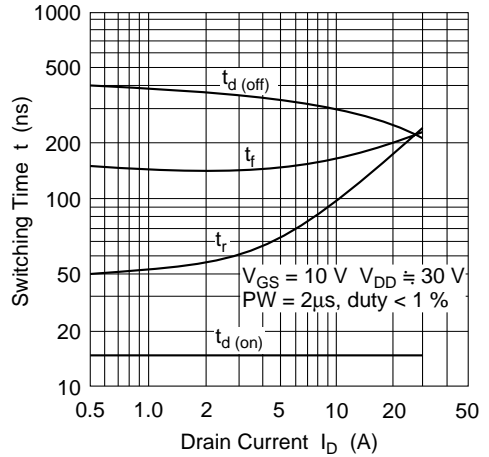
Typical Capacitance vs. Drain to Source Voltage

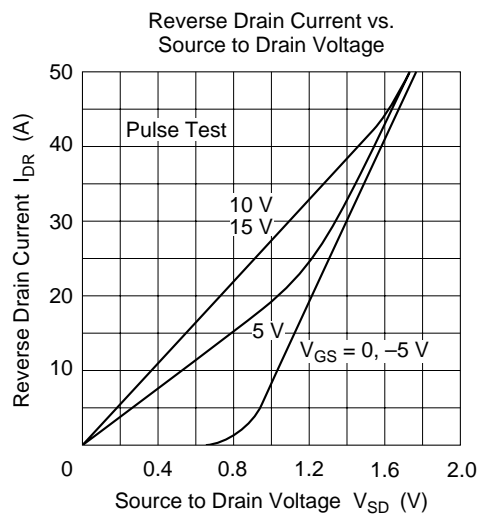


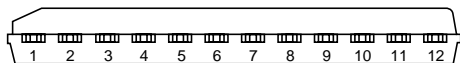
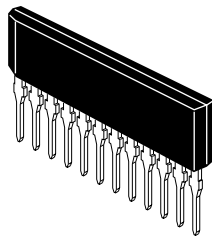
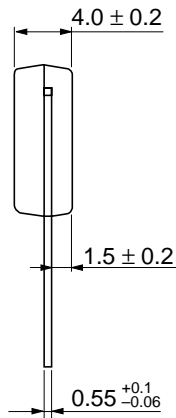
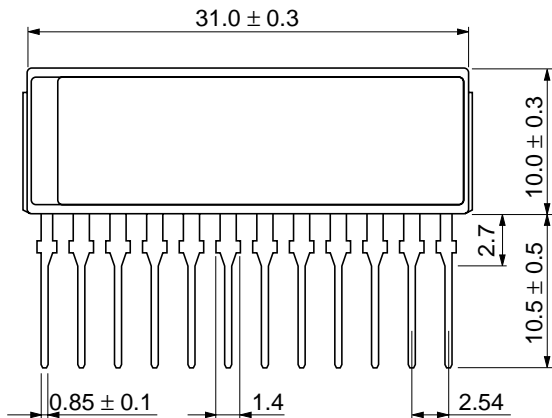
Dynamic Input Characteristics



Switching Characteristics







Hitachi Code	SP-12
JEDEC	—
EIAJ	—
Weight (reference value)	3.6 g

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