NELL SEMICONDUCTOR

Nell High Power Products

N-Channel Power MOSFET
(4A, 800Volts)

DESCRIPTION

The Nell **4N80** is a three-terminal silicon device with current conduction capability of 4A, fast switching speed, low on-state resistance, breakdown voltage rating of 800V ,and max. threshold voltage of 5 volts.
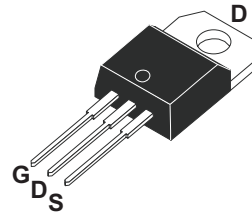
They are designed for use in applications. such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits, and general purpose switching applications .
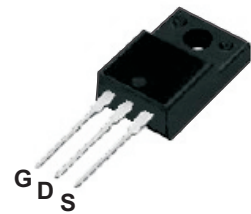
FEATURES

- $R_{DS(ON)}$ = 3.6Ω @ V_{GS} = 10V
- Ultra low gate charge(25nC max.)
- Low reverse transfer capacitance (C_{RSS} = 9pF typical)
- Fast switching capability
- 100% avalanche energy specified
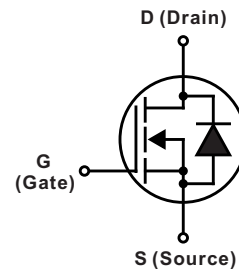- Improved dv/dt capability
- 150°C operation temperature

TO-220AB (4N80A)　　TO-220F (4N80AF)

D (Drain)

G (Gate)

S (Source)

PRODUCT SUMMARY

I_D (A)	4
V_{DSS} (V)	800
$R_{DS(ON)}$ (Ω)	3.6 @ V_{GS} = 10V
Q_G(nC) max.	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

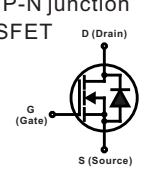| SYMBOL	PARAMETER	TEST CONDITIONS		VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C		800	
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ		800	V
V_{GS}	Gate to Source voltage			±30	
I_D	Continuous Drain Current	T_C=25°C		4	
		T_C=100°C		2.5	
I_{DM}	Pulsed Drain current(Note 1)			15.6	A
I_{AR}	Avalanche current(Note 1)			4	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=4A, R_{GS}=50Ω, V_{GS}=10V		13	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	I_{AS}=4A, L=57mH		460	
dv/dt	Peak diode recovery dv/dt(Note 3)			4.0	V /ns
P_D	Total power dissipation (Derate above 25°C)	T_C=25°C	TO-220AB	106 (0.85)	W(W/°C)
			TO-220F	36 (0.29)	
T_J	Operation junction temperature			-55 to 150	
T_{STG}	Storage temperature			-55 to 150	°C
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case		300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature..

2.I_{AS} = 4A, V_{DD} = 50V, L = 57mH, R_{GS} = 25Ω, starting T_J=25°C.

3.I_{SD} ≤ 4A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J=25°C.

THERMAL RESISTANCE

SYMBOL	PARAMETER		Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-220AB			1.20	°C/W
		TO-220F			3.45	
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-220AB/TO-220F			62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		Min.	Typ.	Max.	UNIT
◎ **OFF CHARACTERISTICS**							
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA ,V_{GS} = 0V		800			V
$\triangle V_{(BR)DSS}/\triangle T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, V_{DS}=V_{GS}			0.95		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=800V, V_{GS}=0V	T_C = 25°C			10	μA
		V_{DS}=640V, V_{GS}=0V	T_C=125°C			100	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 30V, V_{DS} = 0V				100	nA
	Gate to source reverse leakage current	V_{GS} = -30V, V_{DS} = 0V				-100	
◎ **ON CHARACTERISTICS**							
$R_{DS(ON)}$	Static drain to source on-state resistance	I_D =2A, V_{GS} = 10V			2.5	3.6	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA		3		5	V
g_{fs}	Forward transconductance (Note 1)	V_{DS}=50V, I_D=2A			3.8		S
◎ **DYNAMIC CHARACTERISTICS**							
C_{ISS}	Input capacitance	V_{DS} = 25V, V_{GS} = 0V, f =1MHz			680	880	pF
C_{OSS}	Output capacitance				75	100	
C_{RSS}	Reverse transfer capacitance				9	12	
◎ **SWITCHING CHARACTERISTICS**							
$t_{d(ON)}$	Turn-on delay time	V_{DD} = 400V, V_{GS} = 10V, I_D = 4A, R_{GS} = 25Ω (Note 1, 2)			16	40	ns
t_r	Rise time				45	100	
$t_{d(OFF)}$	Turn-off delay time				35	80	
t_f	Fall time				35	80	
Q_G	Total gate charge	V_{DD} = 640V, V_{GS} = 10V, I_D = 4A (Note 1, 2)			19	25	nC
Q_{GS}	Gate to source charge				4		
Q_{GD}	Gate to drain charge (Miller charge)				9		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 4A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			4	A
I_{SM}	Pulsed source current				15.6	
t_{rr}	Reverse recovery time	I_{SD} = 4A, V_{GS} = 0V, dI_F/dt = 100A/μs		580		ns
Q_{rr}	Reverse recovery charge			3.7		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

 2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

4 N 80 A

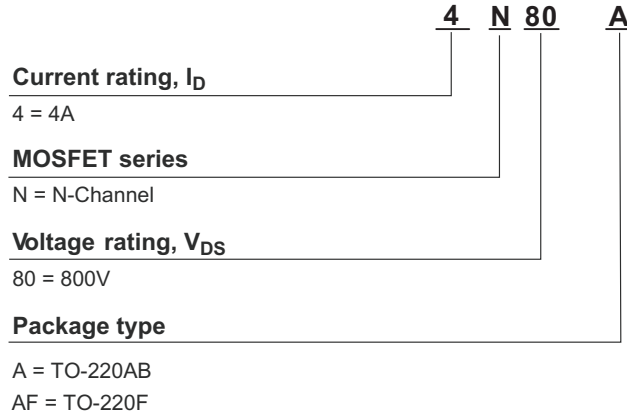**Current rating, I_D**

4 = 4A

MOSFET series

N = N-Channel

Voltage rating, V_{DS}

80 = 800V

Package type

A = TO-220AB
AF = TO-220F

Fig.1 On-region characteristics

V_{GS}
Top: 15 V
10 V
80 V
70 V
60 V
Bottorm: 5.5 V

*Notes:
1.250μs Pulse test
2.T_C=25°C

Drain current, I_D (A)

Drain-to-Source voltage, V_{DS}(V)
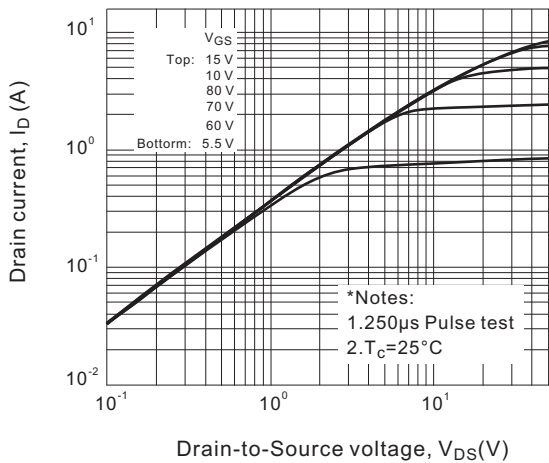
Fig.2 Transfer characteristics

150°C
25°C
-55°C

*Notes:
1.V_{DS}=50V
2.250μs Pulse test

Drain current, I_D (A)

Gate-Source voltage, V_{GS} (V)
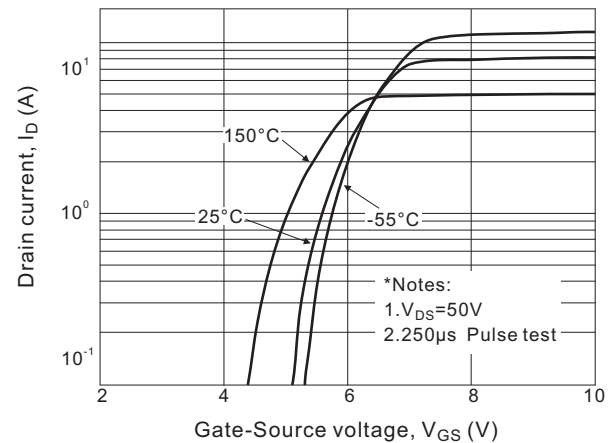
Fig.3 On-resistance variation vs. drain current and gate voltage

V_{GS}=10V
V_{GS}=20V

*Note:T_J=25°C

Drain-source breakdown voltage, BV_{DSS}

Drain current, I_D (A)
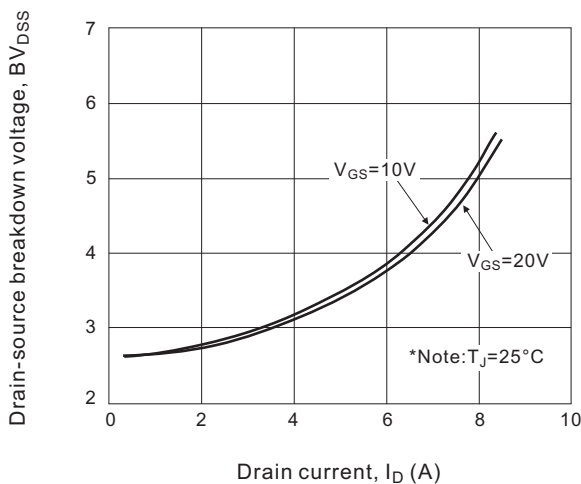
Fig.4 Body diode forward voltage variation vs. Source current and temperature

25°C
150°C

*Notes:
1.V_{GS}=0V
2.250μs Pulse test

Reverse Drain current, I_{DR}(A)

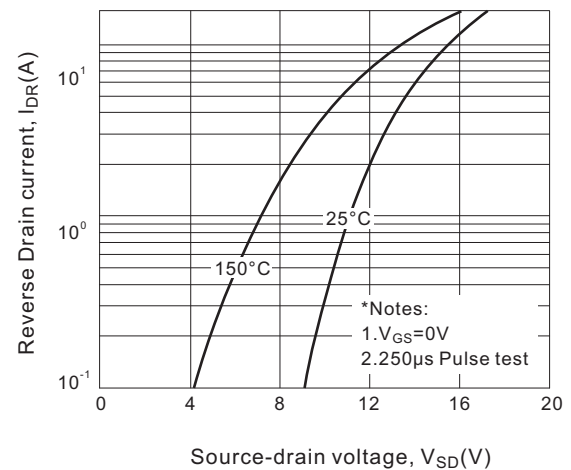Source-drain voltage, V_{SD}(V)
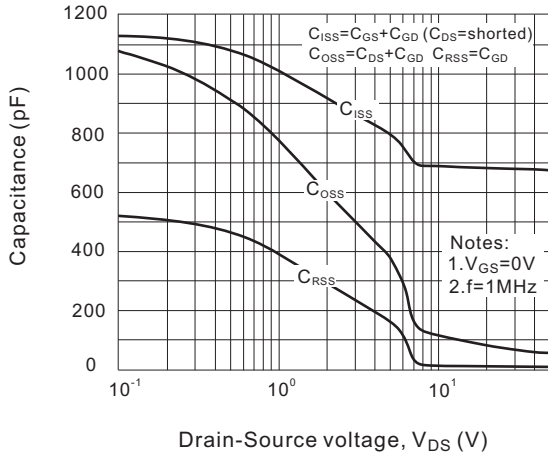
Fig.5 Capacitance characteristics

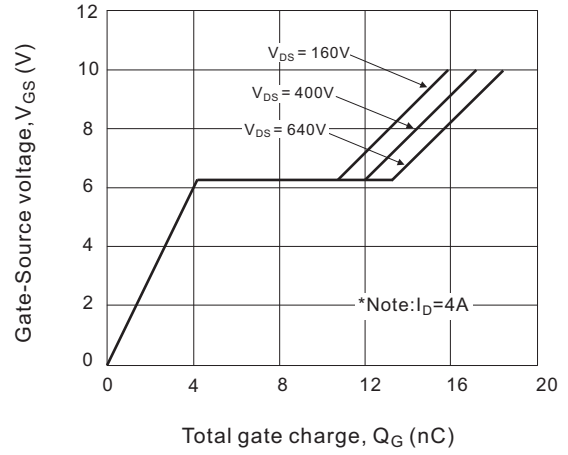**Fig.6 Gate charge characteristics**

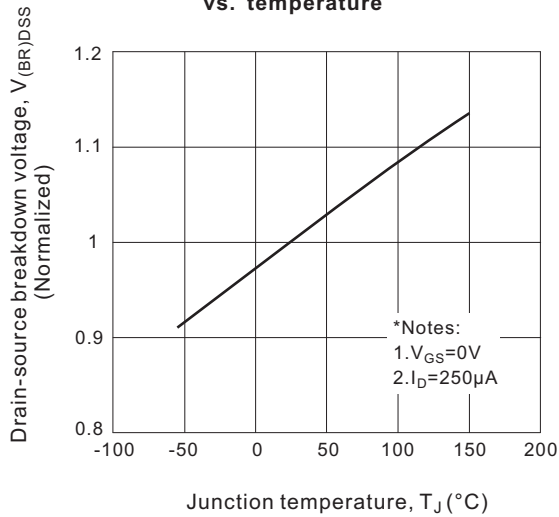**Fig.7 Breakdown voltage variation vs. temperature**
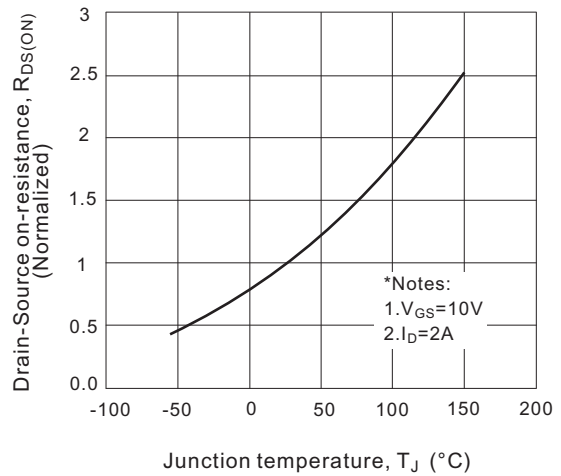

Fig.8 On-resistance vs. temperature

Fig.9-1 Maximum safe operating area for 4N80A

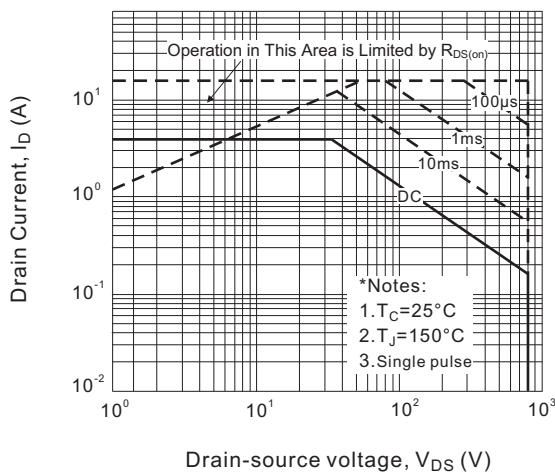**Fig.9-2 Transient thermal response curve for 4N80AF**

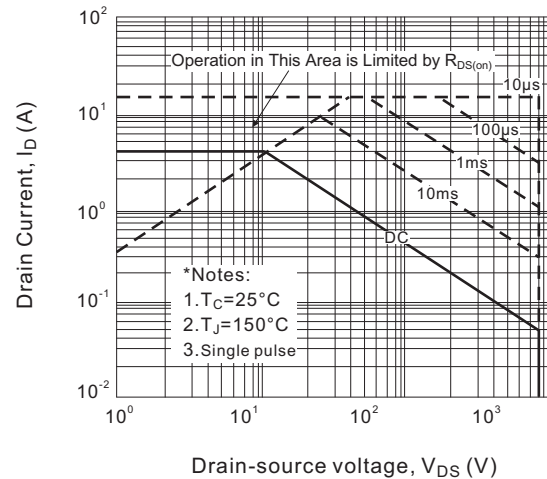## Nell High Power Products

Fig.10 Maximum drain current vs. case temperature

Drain current, I_D (A)

Case temperature, T_C(°C)
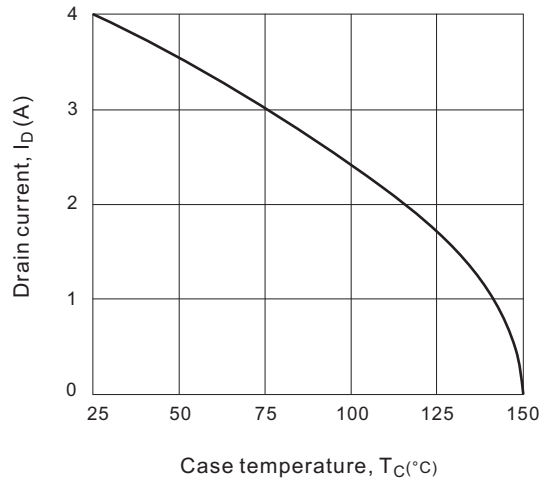
Fig.11-1 Transient Thermal Response Curve for 4N80A

Thermal response, $R_{th(j-c)}$ (t)

D = 0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}
t_1
t_2

Notes:
1. $R_{th(j-c)}(t)$=1.20°C/W Max.
2. Duty factor, D=t1/t2
3. T_{JM}-Tc=P_{DM}×$R_{th(j-c)}(t)$

Square wave pulse duration , t_1(sec.)
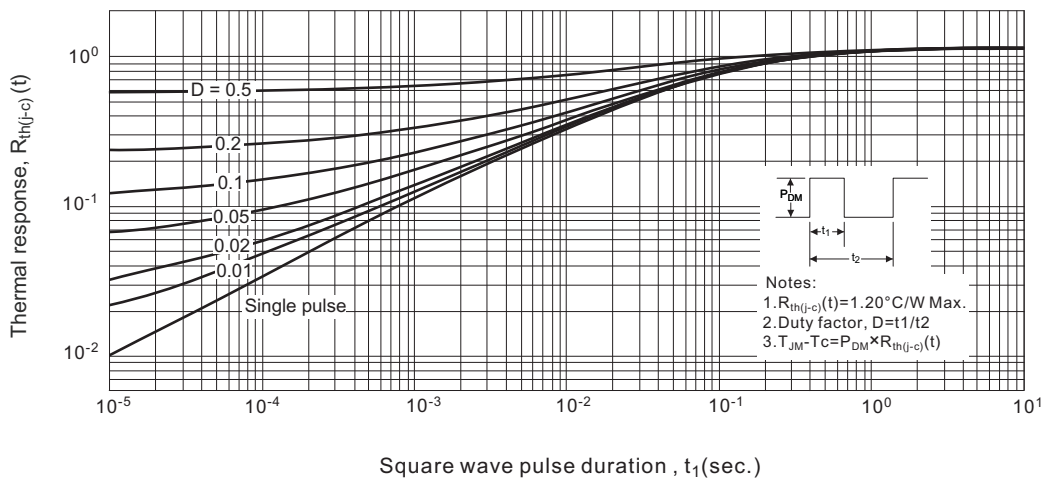
Fig.11-2 Transient Thermal Response Curve for 4N80AF

Thermal response, $R_{th(j-c)}$ (t)

D = 0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}
t_1
t_2

Notes:
1. $R_{th(j-c)}(t)$=3.45°C/W Max.
2. Duty factor, D=t1/t2
3. T_{JM}-Tc=P_{DM}×$R_{th(j-c)}(t)$

Square wave pulse duration , t_1(sec.)
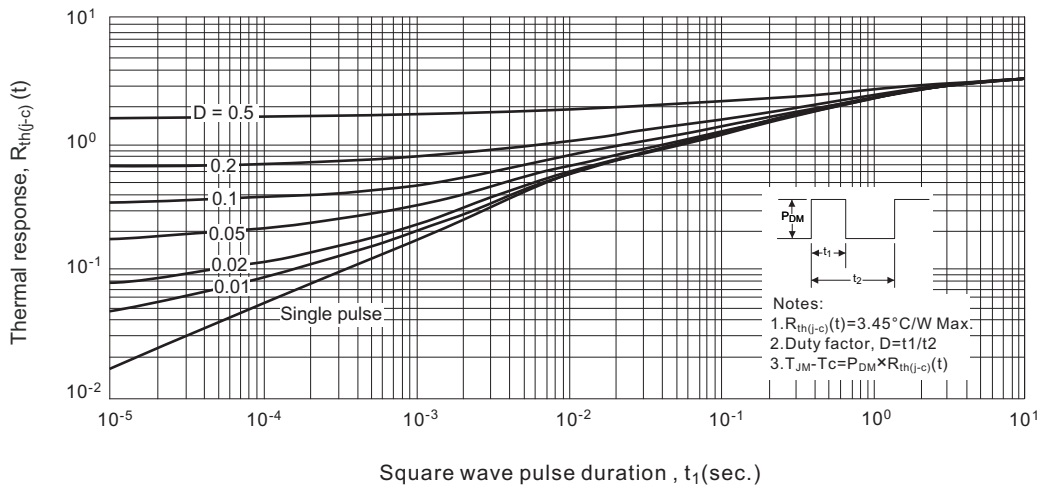
■ **TEST CIRCUITS AND WAVEFORMS**

Fig.1A Peak diode recovery dv/dt test circuit
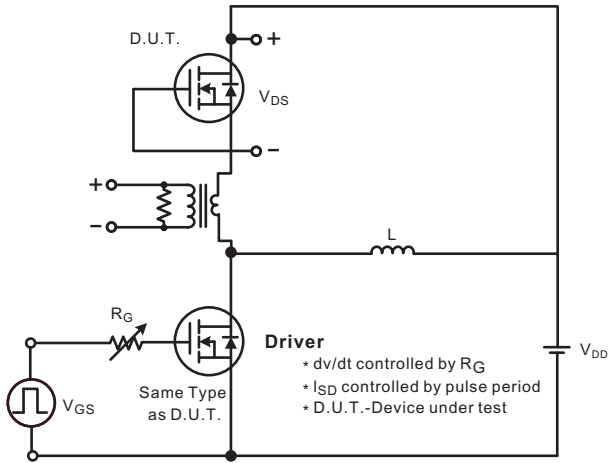
Fig.1B Peak diode recovery dv/dt waverforms

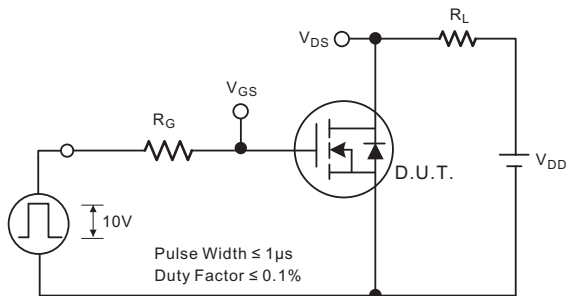Fig.1A circuit:
- D.U.T.
- V_{DS}
- L
- R_G
- Driver
  - Same Type as D.U.T.
  - * dv/dt controlled by R_G
  - * I_{SD} controlled by pulse period
  - * D.U.T.-Device under test
- V_{GS}
- V_{DD}

Fig.1B waveforms:
- V_{GS} (Driver)
- Period
- P.W.
- $D = \dfrac{P.W.}{Period}$
- $V_{GS} = 10V$
- I_{SD} (D.U.T.)
- I_{FM}, Body Diode forward current
- di/dt
- I_{RM}
- Body Diode Reverse Current
- V_{DS} (D.U.T.)
- Body Diode Recovery dv/dt
- V_{DD}
- Body Diode Forward Voltage Drop
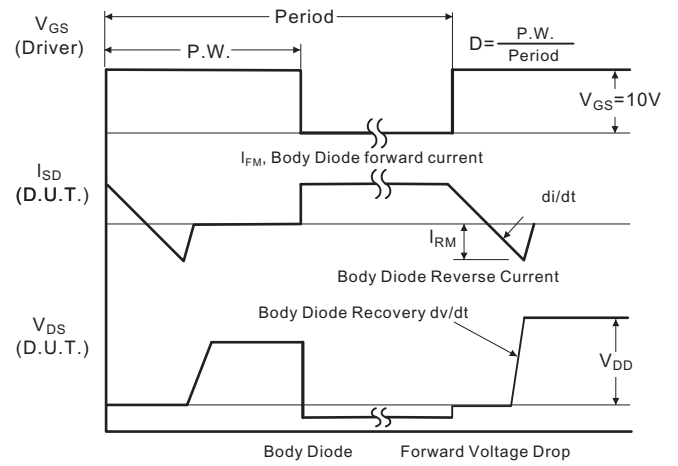
Fig.2A Switching test circuit

Fig.2B Switching Waveforms

Fig.2A circuit:
- R_L
- V_{DS}
- V_{GS}
- R_G
- D.U.T.
- V_{DD}
- 10V
- Pulse Width ≤ 1µs
- Duty Factor ≤ 0.1%

Fig.2B waveforms:
- V_{DS}
- 90%
- V_{GS}
- 10%
- $t_{d(ON)}$
- t_R
- $t_{d(OFF)}$
- t_F
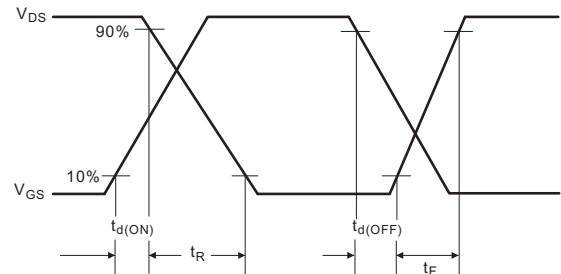
Fig.3A Gate charge test circuit
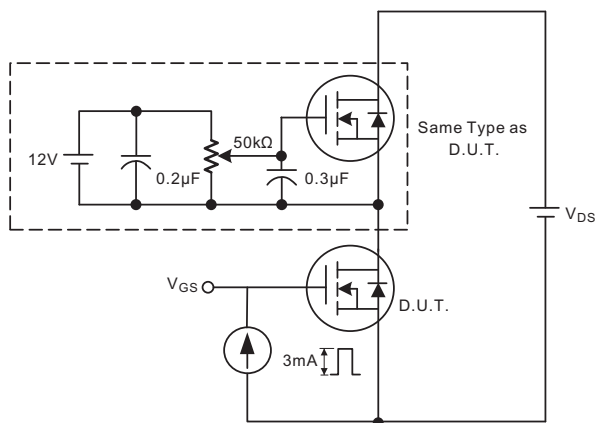
Fig.3B Gate charge waveform

Fig.3A circuit:
- 12V
- 0.2µF
- 50kΩ
- 0.3µF
- Same Type as D.U.T.
- V_{DS}
- V_{GS}
- D.U.T.
- 3mA

Fig.3B waveform:
- V_{GS}
- 10V
- Q_G
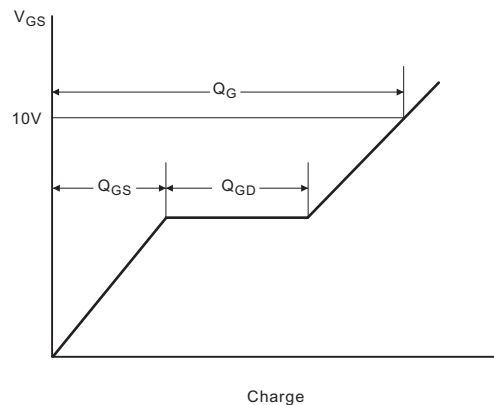- Q_{GS}
- Q_{GD}
- Charge

Fig.4A Unclamped Inductive switching test circuit
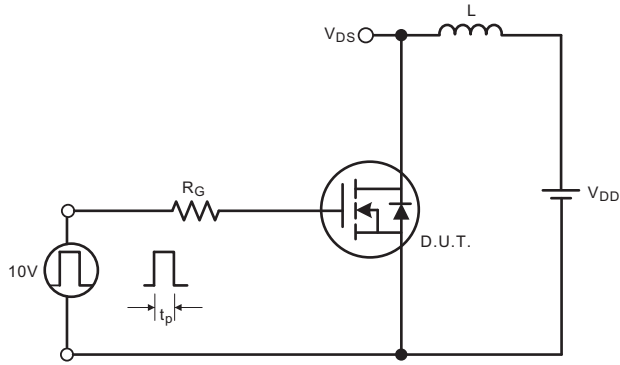
Fig.4B Unclamped Inductive switching waveforms

$$E_{AS} = \frac{1}{2} L \cdot I_{AS}^2 \cdot \frac{V_{BR(DSS)}}{V_{BR(DSS)} - V_{DD}}$$

Case Style

TO-220AB

Case Style

TO-220F

All dimensions in millimeters