

## 1. Description

The KIA50N06 is three-terminal silicon device with current conduction capability of about 50A, fast switching speed. Low on-state resistance, breakdown voltage rating of 60V, and max threshold voltages of 4 volt. It is mainly suitable electronic ballast, and low power switching

## 2. Features

$R_{DS(ON)}=23m\Omega@V_{GS}=10V$ .

Ultra low gate charge (typical 30nC)

Low reverse transfer capacitance

Fast switching capability

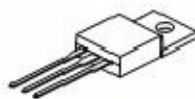
100% avalanche energy specified

Improved dv/dt capability

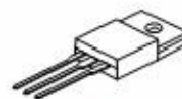
## 3. Pin configuration



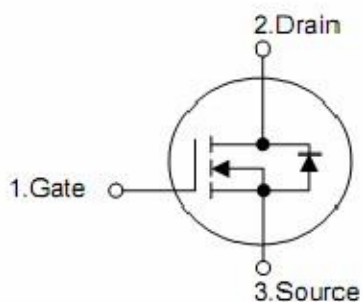
TO-252



TO-220



TO-220F



Pin	Function
1	Gate
2	Drain
3	Source

### 6. Absolute maximum ratings

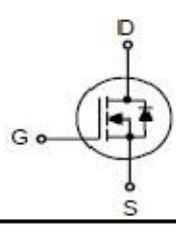
Parameter	Symbol	Value	Unit
Drain to source voltage	$V_{DSS}$	60V	
Gate to source voltage	$V_{GS}$	$\pm 20V$	
Continuous drain current		$T_J = 25^\circ C$ $I_D$	50A
		$T_J = 100^\circ C$ $I_D$	35A
Drain current pulsed (note1)	$I_{DM}$	200A	
Single pulsed avalanche energy (note2)	$E_{AS}$	480mJ	
Repetitive avalanche energy (note1)	$E_{AR}$	13mJ	
Peak diode recovery dv/dt (note3)	dv/dt	7V/ns	
Total power dissipation ( $T_J = 25^\circ C$ )	$P_D$	130W	
Derating factor above 25 °C	$CP_D$	0.9W/°C	
Operating junction temperature	$T_J$	-55 ~ +150°C	
Storage temperature	$T_{STG}$	-55 ~ +150°C	
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.			
Absolute maximum ratings are stress ratings only and functional device operation is not implied.			

### 3. Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal resistance, junction-to-case	$\theta_{JC}$		1.15	°C/W
Thermal resistance, case-to-sink	$\theta_{CS}$			°C/W
Thermal resistance, junction-to-ambient	$\theta_{JA}$	0.5		°C/W
			62.5	

**7. Electrical characteristics**

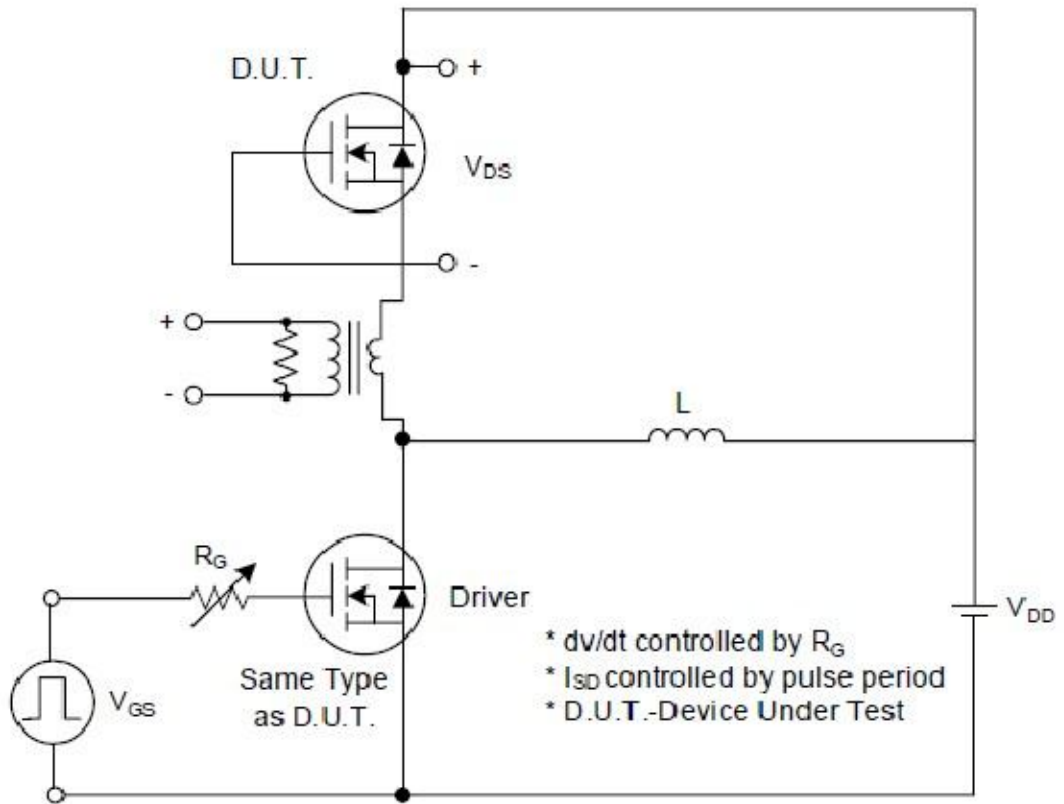
(T<sub>J</sub>=25°C, unless otherwise notes)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
<b>Off characteristics</b>						
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA		60		V
Breakdown voltage temperature coefficient	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	I <sub>D</sub> =250μA, referenced to 25 °C		0.07		V/°C
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =48V, T <sub>c</sub> =125 °C			1	μA
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V			100	nA
		V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
<b>Gate-source leakage Reverse</b>						
<b>On characteristics</b>						
Gate threshold voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA		2.0	4.0	V
Static drain-source on-state resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =25A		18	23	mΩ
<b>Dynamic characteristics</b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		900	1220	pF
Output capacitance	C <sub>OSS</sub>			430	550	pF
Reverse transfer capacitance	C <sub>RSS</sub>			80	100	pF
<b>Switching characteristics</b>						
Turn-on delay time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =25A, R <sub>G</sub> =50Ω (note4,5)		40	60	ns
Rise time	t <sub>r</sub>			100	200	ns
Turn-off delay time	t <sub>D(OFF)</sub>			90	180	ns
Fall time	t <sub>f</sub>			80	160	ns
Total gate charge	Q <sub>G</sub>			30	40	nC
Gate-source charge	Q <sub>GS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =10V, I <sub>D</sub> =50A (note4,5)		9.6		nC
Gate-drain charge (miller charge)	Q <sub>GD</sub>			10		nC
<b>Source-drain diode ratings and characteristics</b>						
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =50A			1.5	V
Continuous source current	I <sub>S</sub>	Integral reverse p-n junction diode in the MOSFET 			50	A
Pulsed source current	I <sub>SM</sub>					200
Reverse recovery time	t <sub>RR</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =50A		54		ns
Reverse recovery charge	Q <sub>RR</sub>			81		μC

diF/dt=100A/μs(note4)Reverse recovery chargeQ<sub>RR</sub>

- Note: 1. repetitive rating: pulse width limited by junction temperature  
 2. L=5.6mH, I<sub>AS</sub>=50A, V<sub>DD</sub>=25V, R<sub>G</sub>=0Ω, starting T<sub>J</sub>=25°C  
 3. I<sub>SD</sub><50A, di/dt<300A/μs, V<sub>DD</sub><BV<sub>DSS</sub>, starting T<sub>J</sub>=25 °C  
 4. Pulse test: pulse width<300μs, duty cycle<2% –  
 5. Essentially independent of operating temperature

8. Test circuits and waveforms



**Fig. 1A Peak Diode Recovery  $dv/dt$  Test Circuit**

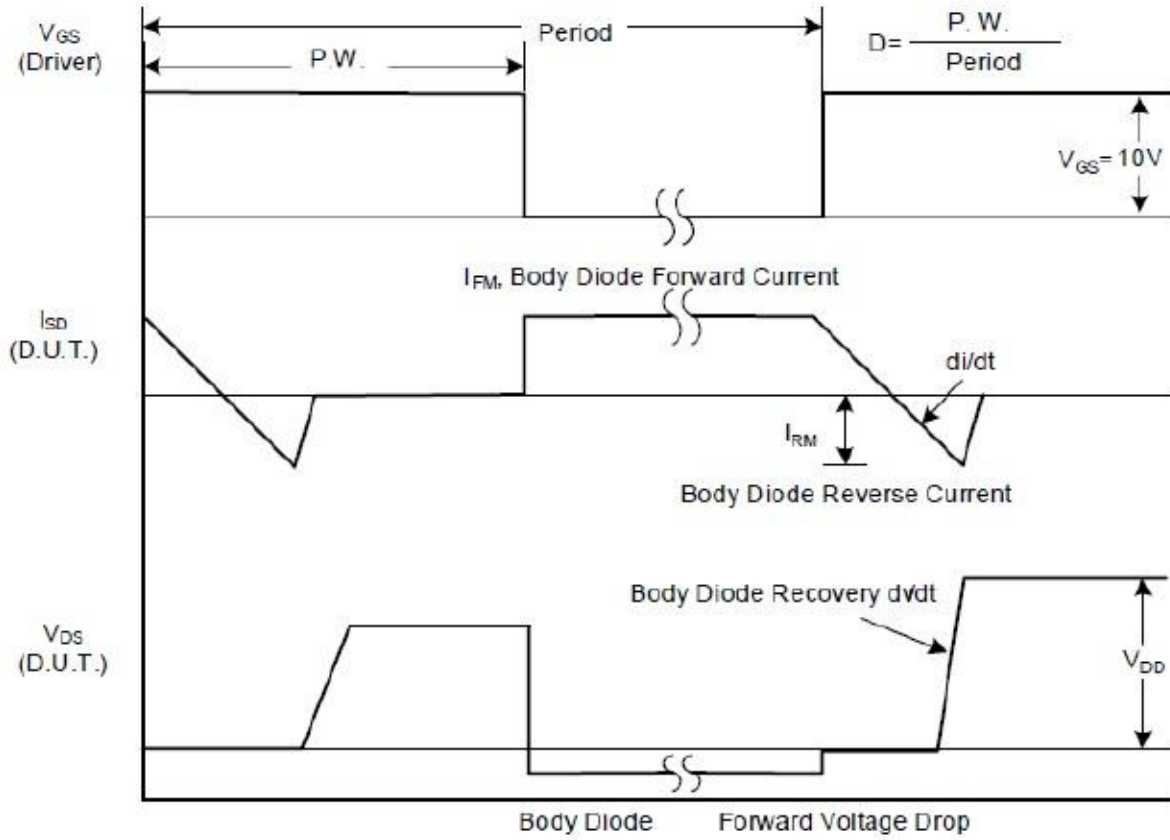
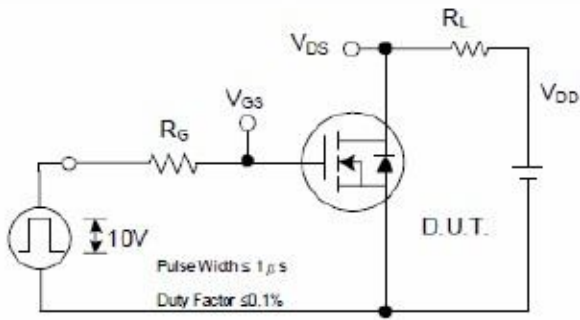
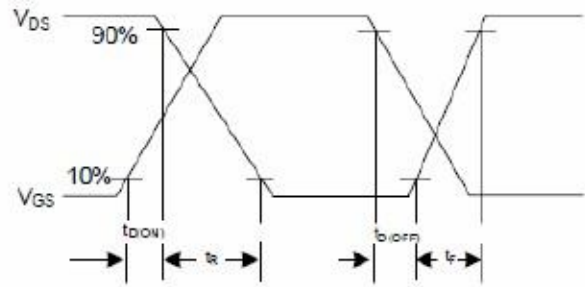


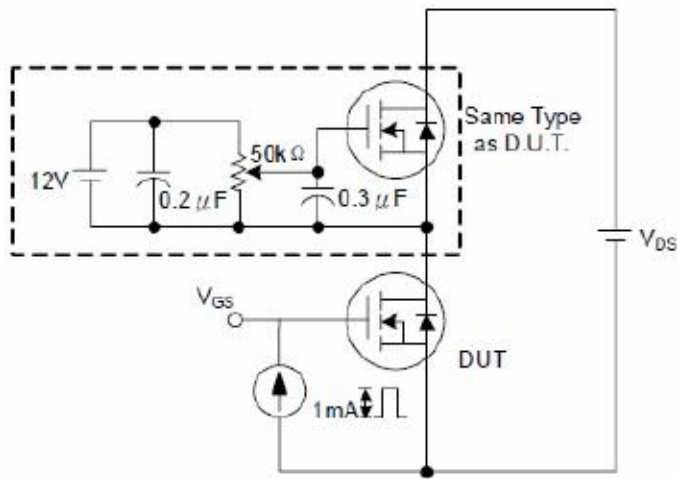
Fig. 1B Peak Diode Recovery  $dv/dt$  Waveforms



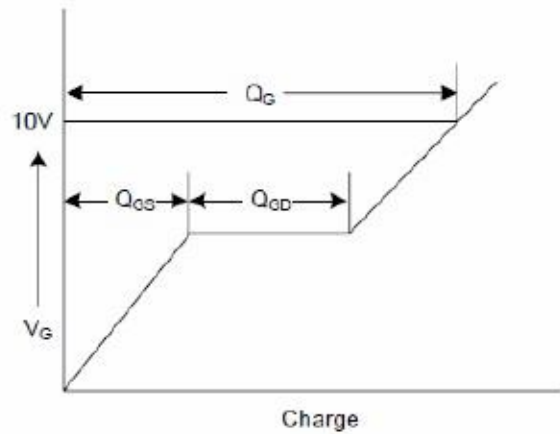
**Fig. 2A Switching Test Circuit**



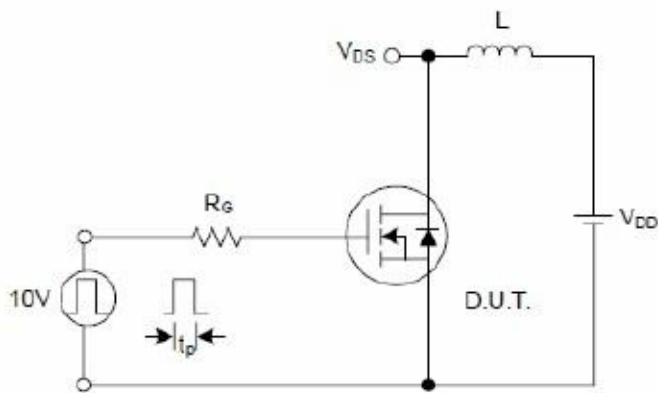
**Fig. 2B Switching Waveforms**



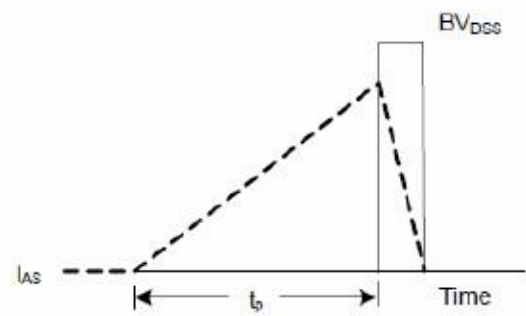
**Fig. 3A Gate Charge Test Circuit**



**Fig. 3B Gate Charge Waveform**



**Fig. 4A Unclamped Inductive Switching Test Circuit**



**Fig. 4B Unclamped Inductive Switching Waveforms**

9. Typical characteristics

