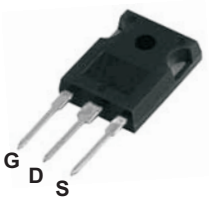
N-Channel Power MOSFET
50A, 300Volts

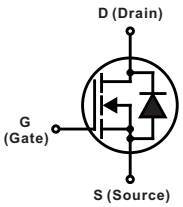
DESCRIPTION

The Nell **50N30** is a three-terminal silicon device with current conduction capability of 50A, fast switching speed, low on-state resistance, breakdown voltage rating of 300V, and max. threshold voltage of 6.5 volts.

They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits, battery chargers, DC choppers, temperature and lighting controls and general purpose switching applications.



TO-247AB
(50N30C)



FEATURES

- $R_{DS(ON)}$ = 0.080Ω @ V_{GS} = 10V
- Ultra low gate charge(65nC typical)
- Low reverse transfer capacitance (C_{RSS} = 60pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	50
V_{DSS} (V)	300
$R_{DS(ON)}$ (Ω)	0.080 @ V_{GS} = 10V
Q_G(nC) typical	65

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C	300	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ	300	
V_{GS}	Gate to Source voltage		±20	
I_D	Continuous Drain Current	T_C=25°C	50	A
		T_C=100°C	35	
I_{DM}	Pulsed Drain current(Note 1)		150	
I_{AR}	Avalanche current(Note 1)		50	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=50A, R_{GS}=50Ω, V_{GS}=10V	50	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	I_{AS}=50A, L=0.1mH	1500	
dv/dt	Peak diode recovery dv/dt(Note 3)		50	V /ns
P_D	Total power dissipation	T_C=25°C	690	W
	Linear derating factor above T_C=25°C		5.8	°C/W
T_J	Operation junction temperature		-55 to 150	°C
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{AS}=50A, L=0.1mH, V_{DD}=50V, R_{GS}=25Ω, starting T_J = 25°C.
3.I_{SD} ≤ 50A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

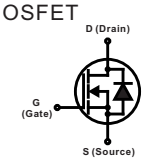
THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			0.18	°C/W
$R_{th(j-a)}$	Thermal resistance, junction to ambient			50	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
◎ OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 1mA, V_{GS} = 0V		300			V
$V_{(BR)DSS}$/ T_J	Breakdown voltage temperature coefficient	I_D = 1mA, V_{DS} =V_{GS}			0.35		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=300V, V_{GS}=0V	T_C=25°C			10	μA
		V_{DS}=240V, V_{GS}=0V	T_C=125°C			100	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 20V, V_{DS}= 0V				100	nA
	Gate to source reverse leakage current	V_{GS} = -20V, V_{DS}= 0V				-100	
◎ ON CHARACTERISTICS							
$R_{DS(ON)}$	Static drain to source on-state resistance	V_{GS}=10V, I_D=25A				0.080	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=4mA		3.5		6.5	V
g_{fs}	Forward transconductance	V_{DS} = 20V, I_D = 25A		19	29		S
◎ DYNAMIC CHARACTERISTICS							
C_{ISS}	Input capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz			3160		pF
C_{OSS}	Output capacitance				600		
C_{RSS}	Reverse transfer capacitance				60		
R_G	Gate input resistance				0.17		Ω
◎ SWITCHING CHARACTERISTICS							
$t_{d(ON)}$	Turn-on delay time	V_{DD}=150V, V_{GS}=10V I_D=25A, R_{GS}=2Ω (Note1,2)			14		ns
t_r	Rise time				15		
$t_{d(OFF)}$	Turn-off delay time				24		
t_f	Fall time				9		
Q_G	Total gate charge	V_{DD}= 150V, V_{GS}=10V I_D=25A, (Note1,2)			65		nC
Q_{GS}	Gate to source charge				22		
Q_{GD}	Gate to drain charge (Miller charge)				32		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 50A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			50	A
I_{SM}	Pulsed source current				200	
t_{rr}	Reverse recovery time	I_{SD} = 25A, V_{GS} = 0V, dI_F/dt = 100A/μs			250	ns
Q_{rr}	Reverse recovery charge			0.95		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

50 N 30 C

Current rating, I_D
50 = 50A

MOSFET series
N = N-Channel

Voltage rating, V_{DS}
30 = 300V

Package type
C = TO-247AB

■ TEST CIRCUITS

Fig.1A Peak diode recovery dv/dt test circuit

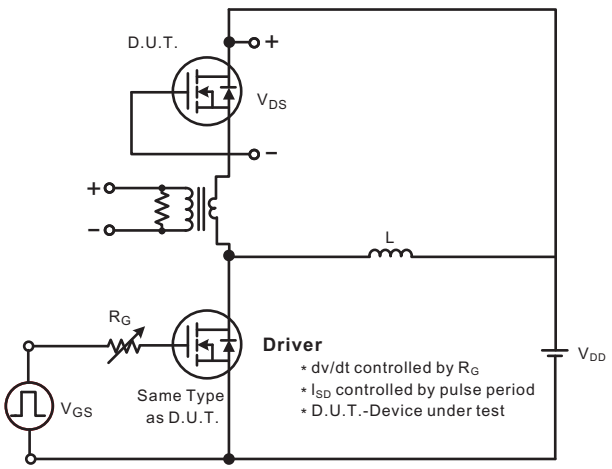
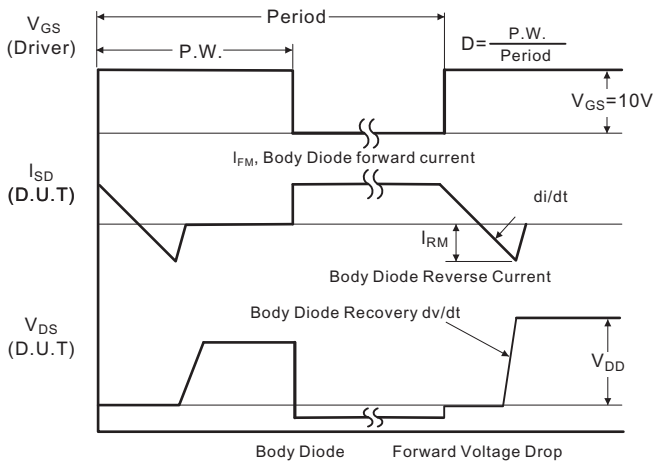


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUIT(Cont.)

Fig.2A Switching test circuit

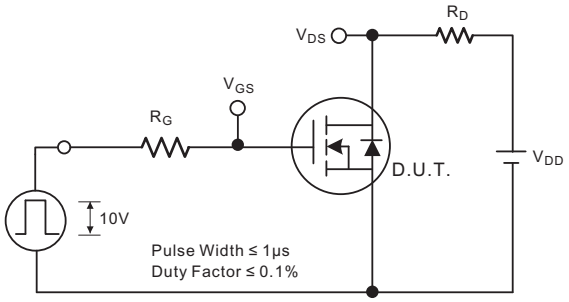


Fig.2B Switching Waveforms

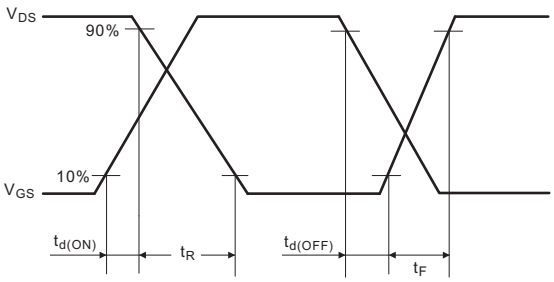


Fig.3A Gate charge test circuit

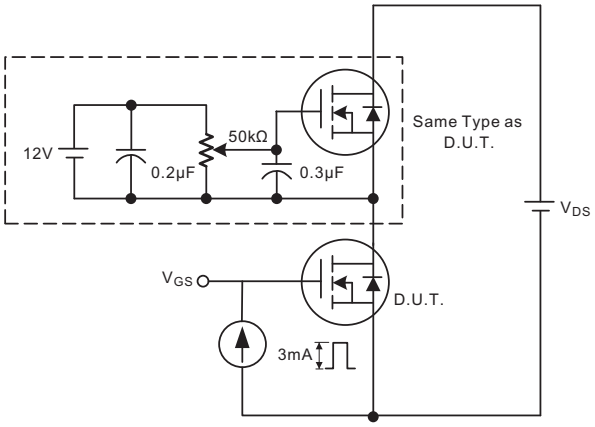


Fig.3B Gate charge waveform

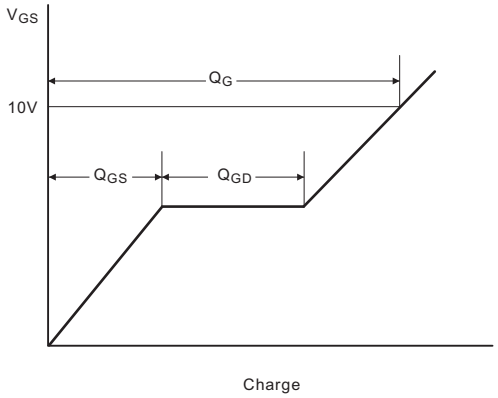


Fig.4A Unclamped Inductive switching test circuit

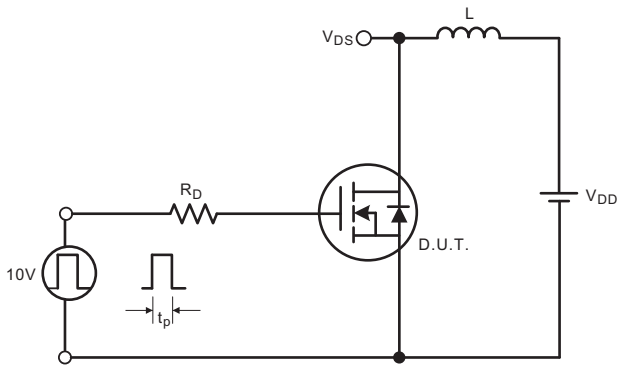


Fig.4B Unclamped Inductive switching waveforms

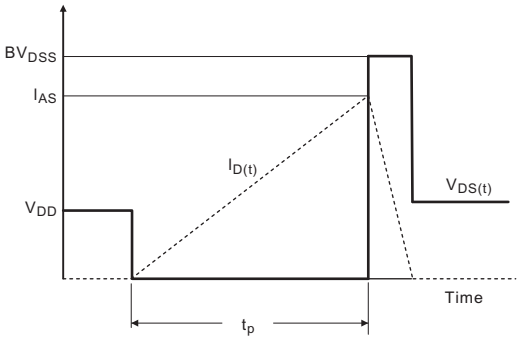


Fig.1 Output characteristics

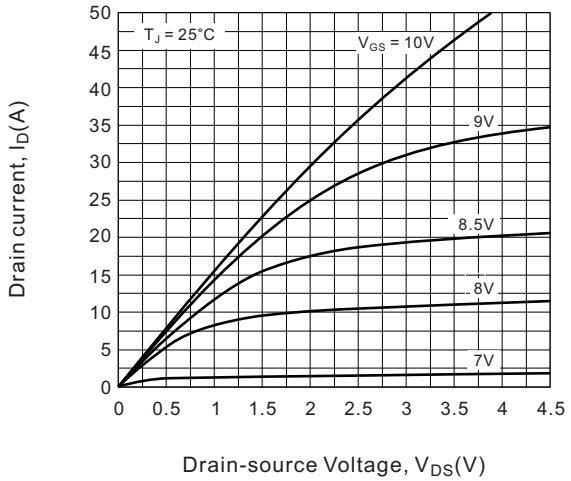


Fig.2 Extended output characteristics

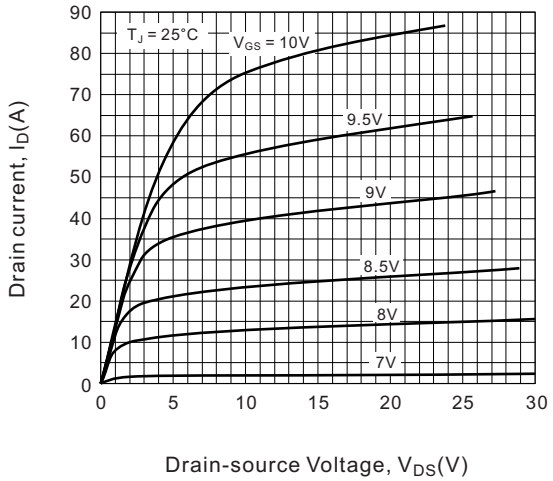


Fig.3 Output characteristics

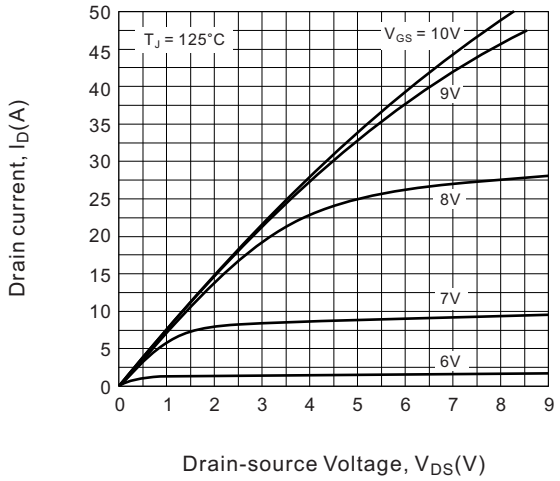


Fig.4 $R_{DS(on)}$ Normalized to I_D =25A value vs. Junction temperature

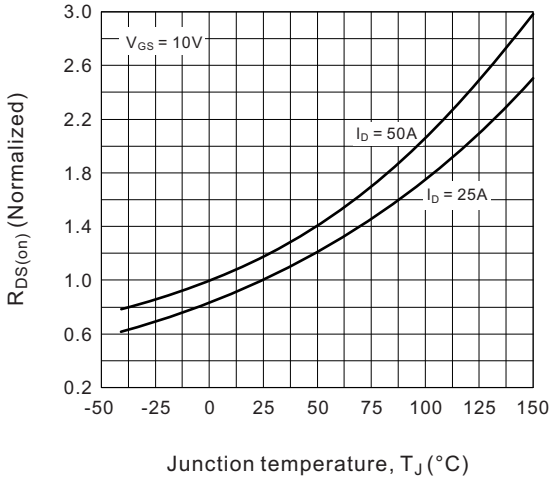


Fig.5 $R_{DS(on)}$ Normalized to I_D =25A value vs. Drain current

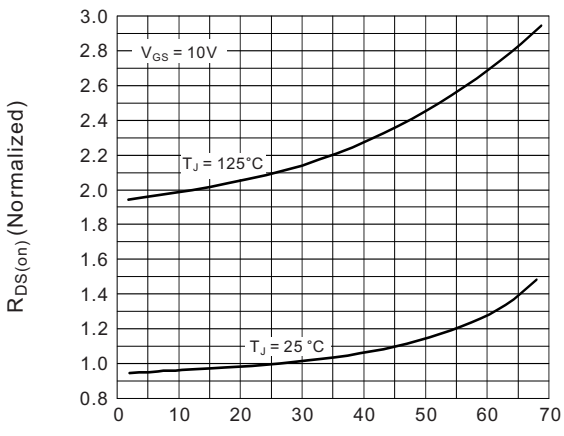


Fig.6 Maximum drain current vs. Case temperature

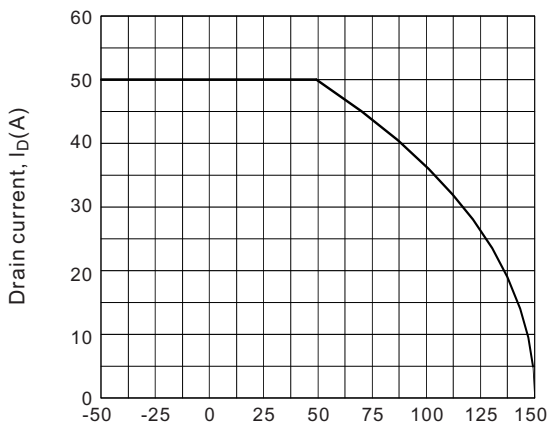


Fig.7 Transfer characteristics

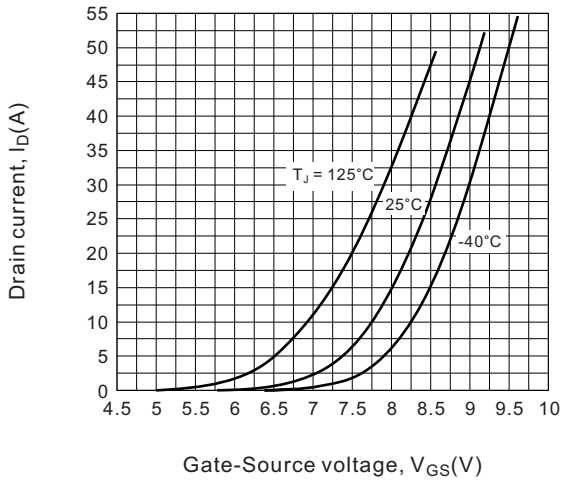


Fig.8 Transconductance

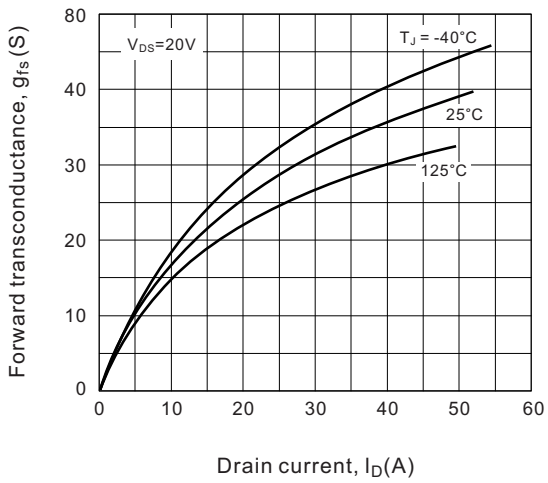


Fig.9 Forward voltage drop of Intrinsic diode

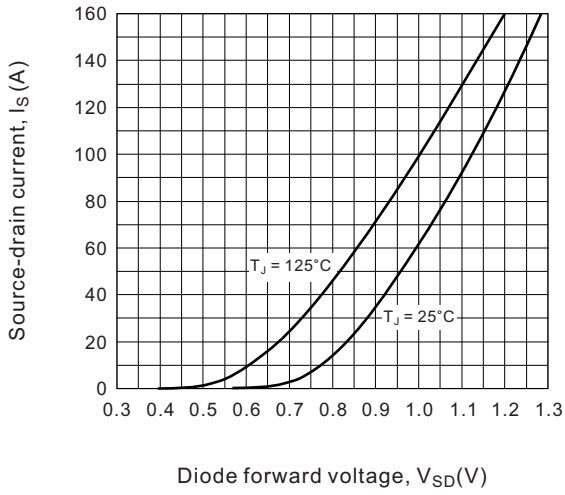


Fig.10 Gate charge characteristics

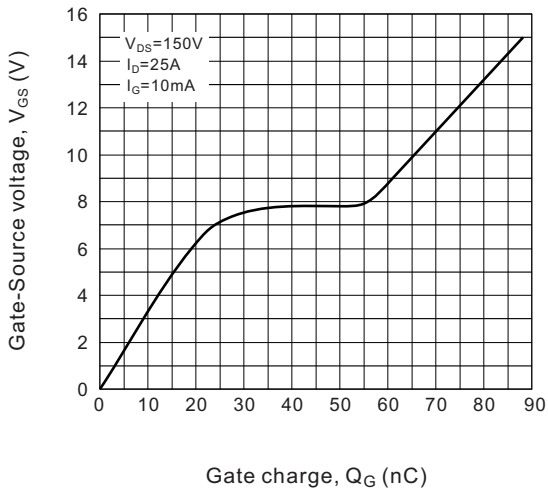


Fig.11 Capacitance characteristics

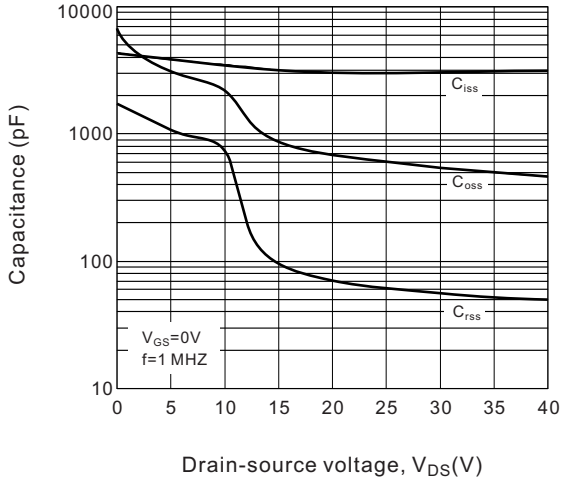


Fig.12 Forward-Bias safe opeerating area

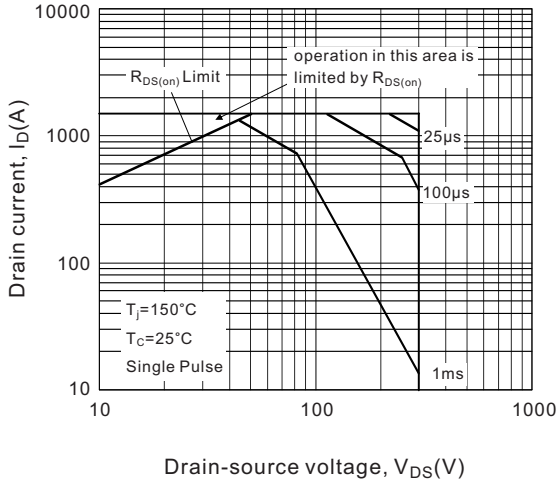
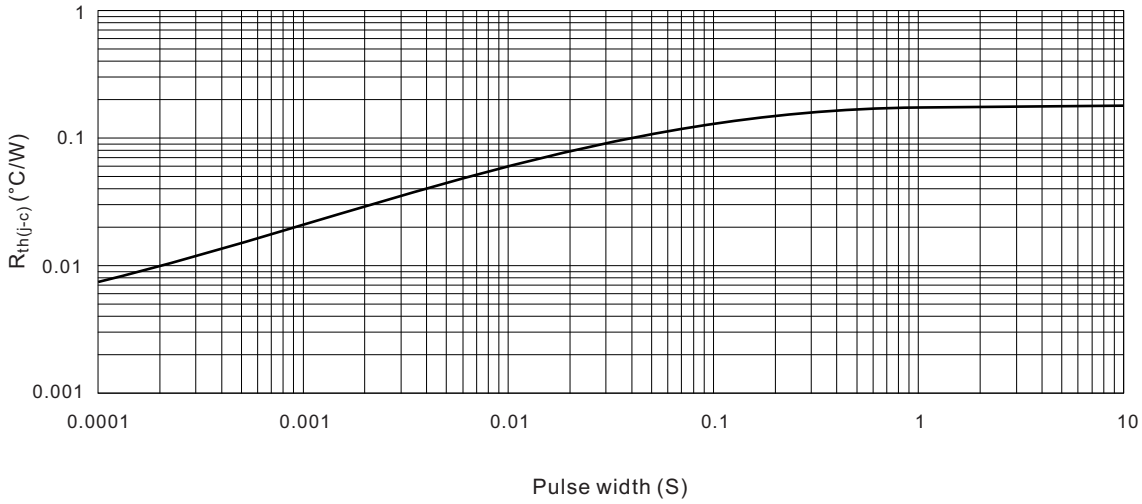
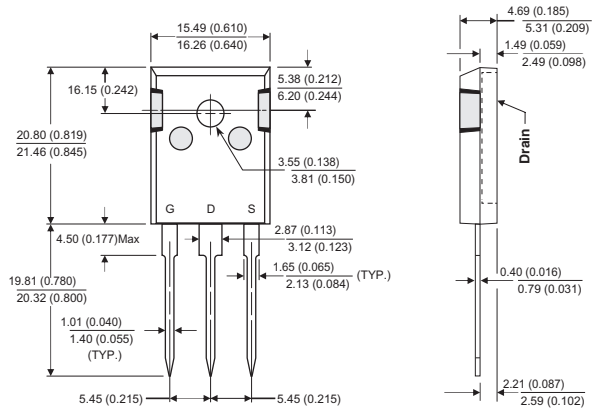


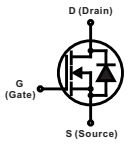
Fig.13 Maximum transient thermal Impedance



Case Style

TO-247AB





All dimensions in millimeters(inches)