Dual-Bridge Sensor Signal Processor with SENT Interface 520.47

PRODUCT PREVIEW – May 18, 2018

RoHS compliant

Features and Benefits

- Supply voltage: 4.75 V to 5.25 V
- Supply and output protection: -18/+35 V
- Simultaneous signal processing for two sensors
- Fully digital calibration; no external trim components
- Tool set provided for application support
- Optimized for resistive sensor bridges
- Sensitivity range: 3 - 112 mV/V
- 10-step coarse gain trimming
- 31-step coarse offset trimming to ±4* input span
- Low noise input with 15-bit ADC
- Configurable digital low-pass: 13Hz ... 1.1kHz
- Additional NTC channel with on-chip linearization
- 12-bit output via configurable SENT interface
- Configurable SENT output; same pin providing single-wire programming interface
- I²C interface for fast access to sensor/configuration/calibration data
- Developed acc. to ISO26262 with safety requirements rated up to ASIL C

Applications

- Automotive sensor applications
- Safety applications, e.g. braking systems
- General MEMS p-sensor applications
- Conditioning of resistive bridge sensors

General Description

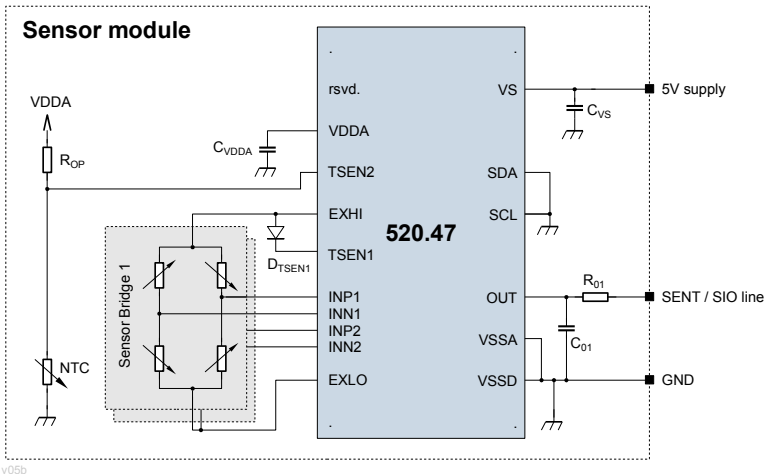
This IC provides low-noise sensor signal conditioning with two individual 15-bit Delta-Sigma ADCs for two resistive bridge sensors, including compensation and linearization. Two additional temperature channels with a 14-bit Delta-Sigma ADC allow for precise acquisition and linearization of divers temperature sensors.
Internal sensor- and self-diagnosis, particular safety requirements and the development compliant to ISO26262 enable the integration of this IC into safety applications.
All compensated and linearized sensor data are available at the digital SENT interface output. The dual function SENT pin permits a serial I/O communication to enable real 3-wire end-of-line configuration and calibration.
Alternatively an additional I²C interface allows faster access to sensor, diagnosis, calibration and configuration data.
A calibration tool set including a bench top evaluation software is provided to facilitate sensor mass production.

Ordering Information

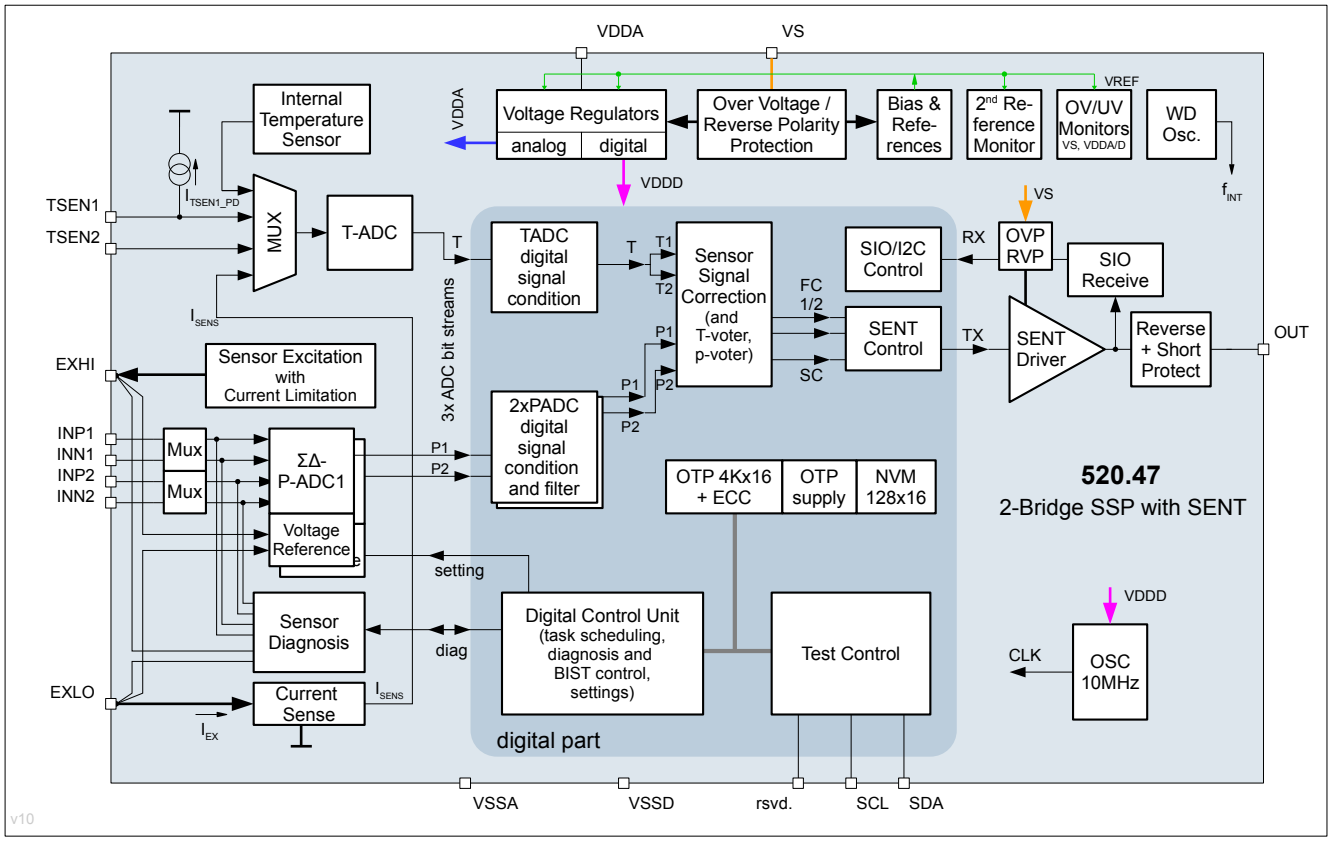
Order Code	Temperature Range	Package
E52047A52C	-40°C to +140°C	QFN20L4
E52047A24Y	-40°C to +150°C	Die *

* Contact factory for bare die specifications

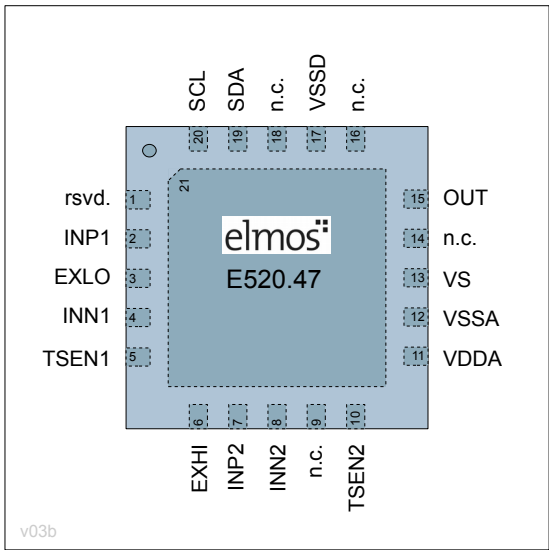
Typical Operating Circuit



Functional Diagram



Pin Configuration



Pin Description

No	Name	Type	Description
1	reserved		Internally connected. Reserved for factory use, connect to VSSD.
2	INP1	A_I	sensor voltage input 1, positive
3	EXLO	A_O	sensor excitation voltage output, negative
4	INN1	A_I	sensor voltage input 1, negative
5	TSEN1	A_I	external diode type temperature sensor input 1, connect to EXHI if not used
6	EXHI	A_O	sensor excitation voltage output, positive
7	INP2	A_I	sensor voltage input 2, positive
8	INN2	A_I	sensor voltage input 2, negative
9	n.c.		Not connected. Leave open.
10	TSEN2	A_I	external RTD type temperature sensor input 2, leave pin open if not used
11	VDDA	A_O	internal analogue voltage supply output, external connections only acc. to recommended operating conditions
12	VSSA	S	supply ground, analogue
13	VS	HV_S	main supply input
14	n.c.		Not connected. Leave open.
15	OUT	HV_D_IO	SENT data output / Serial IO programming interface
16	n.c.		Not connected. Leave open.
17	VSSD	S	supply ground, digital
18	n.c.		Not connected. Leave open.
19	SDA	D_IO	I2C data I/O, connect to VSSD if not used
20	SCL	D_I	I2C clock input, connect to VSSD if not used
21	EP	S	exposed die pad; connect to VSSA on PCB

Note: A = Analogue, D = Digital, S = Supply, I = Input, O = Output, IO = Bidirectional, HV = High Voltage

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to VSSA. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Table 1-1: Maximum Ratings

No.	Description	Condition	Symbol	Min	Max	Unit
1	supply voltage at pin VS		V_{VS}	-18	+35	V
2	voltage at data output pin OUT		V_{OUT}	-18	+35	V
3	voltage at output pin VDDA		V_{VDDA}	-0.3	+5.5	V
4	voltage at sensor inputs pins INP1, INN1, INP2 and INN2[1)]		V_{AIN}	-0.3	+5.5	V
5	voltage at sensor excitation pin EXHI[1)]		V_{EXHI}	-0.3	+5.5	V
6	voltage at sensor ground pin EXLO		V_{EXLO}	-0.3	+0.6	V
7	voltage at pin VSSD		V_{VSSD}	-0.3	+0.3	V
8	voltage at temperature sensor inputs pins TSEN1 and TSEN2[1)]		$V_{TSEN1,2}$	-0.3	+5.5	V
9	voltage at digital input SCL, SDA		V_{DIG_IO}	-0.3	+5.5	V
10	current at output pin OUT		I_{OUT}	-10	+10	mA
11	current at pin VDDA		I_{VDDA}	-20	+5	mA
12	current at sensor inputs pins INP1, INN1, INP2 and INN2		I_{AIN}	-5	+5	mA
13	current at pin EXHI		I_{EXHI}	-10	+5	mA
14	current at pin EXLO		I_{EXLO}	-5	+10	mA
15	current at pins TSEN1, TSEN2		$I_{TSEN1,2}$	-5	+5	mA
16	current at digital IOs SCL, SDA		I_{DIG_IO}	-10	+5	mA
17	storage temperature[2)]		T_{ST}	-40	150	°C
18	junction temperature[3)]		T_J	-40	150	°C

[1)] Maximum limit: Whatever voltage is lower: 5.5V or V_{VDDA}+0.3V.
[2)] See 4.7-1 for a permissible temperature profile to ensure NVM data retention.
For moisture sensitive devices refer to JEDEC standard J-STD-033 for details of handling and usage. Storage at temperatures > 90°C for more than 96 h may affect the solderability of the devices. Storage is not considering any packing materials such as tapes, reels, dry packs, foils etc.
[3)] See 4.7-1 for a permissible temperature profile to ensure NVM data retention.

2 ESD

Table 2-1: ESD Level Definition

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM protection at system level pins only: OUT, VS, VSSD, VSSA	[1]	$V_{ESD(HBM)SYS}$	-4	4	kV
ESD HBM protection at all pins	[2]	$V_{ESD(HBM)}$	-2	2	kV
ESD CDM protection at all pins	[3]	$V_{ESD(CDM)}$	-500	500	V
ESD CDM protection at edge pins	[3]	$V_{ESD(CDM)C}$	-750	750	V

[1] According to AEC-Q100-002 (HBM) chip level test; system level pins are OUT, VS, VSSD, VSSA
[2] According to AEC-Q100-002 (HBM) chip level test; all other pins
[3] According to AEC-Q100-011 (CDM) chip level test

3 Recommended Operating Conditions

Table 3-1: Recommended Operating Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	supply voltage at pin VS		V_{VS}	4.75	5.00	5.25	V
2	input voltage range for pins EXHI, INN1, INP1, INN2, INP2, TSEN1, TSEN2[1)]		V_{SEN}	0	-	1	V_{VDDA}
3	input voltage range for pin EXLO		V_{EXLO}	0	-	0.11	V_{EXHI}
4	ambient temperature	in QFN20L4	T_A	-40	-	140	°C
5	external load at regulator at pin VDDA[2)]	at pin VDDA	$I_{VDDA\_EXT\_LD}$	-1.5	-	0	mA
6	DC current at pin OUT	DC	I_{OUT}	-1.2	-	+1.2	mA
7	buffer capacitor at VS	close to pin	C_{VS}	80	100	250	nF
8	bypass capacitor at VDDA	close to pin	C_{VDDA}	80	100	120	nF
9	**diode sensor parameters**		.				
10	forward voltage of external temperature sensing diode at TSEN1(2)	I_F=20µA	V_{F_DIO}	0.2	-	1.1	V
11	linear TC of forward voltage of external diode at TSEN1	I_F=20µA	TC_{VF}	-2.3	-2.0	-1.7	mV/K
12	**NTC sensor parameters**		.				
13	optional filter capacitor at TSEN2[3)]	close to pin	C_{TSEN2}	-	10	13	nF
14	load resistor for NTC resistor divider[4)]		R_{OP}	0.8	-	1.2	R_{NTC_25}
15	NTC resistance at room temperature	R_{NTC}(T=25°C)	R_{NTC_25}	2	-	10	kΩ
16	usable input range for NTC divider at pin TSEN2[5)]		V_{IN_NTC}	2.5	-	97.5	% VDDA
17	**sensor bridge parameters**		.				
18	capacitance from pins INP1, INN1, INP2 or INN2 to GND[6)]		C_{IN_GND}	-	-	130	pF
19	common mode input voltage at sensor inputs INP1/INN1 and INP2/INN2[7)]	0.5*(V_{INP}+V_{INN})-V_{EXLO}	V_{IN_CM}	0.40	0.50	0.60	V_{EX}
20	single ended input voltage at sensor inputs INP1/INN1 and INP2/INN2 to avoid diagnosis errors[8)]		V_{IN_BR}	0.35	-	0.65	V_{EX}
21	sensor bridge resistance (EXHI to EXLO)[9)]	bridges parallel	R_{BR}	0.9	-	12	kΩ
22	sensor bridge resistance of each of one or two bridges to avoid diagnosis errors[10)]	(each) single bridge	R_{BR_single}	0.9	-	12	kΩ
23	linear TC of bridge resistance in case of temperature sensing via bridge current		TCR_{BR}	1600	-	5000	^{ppM}/K
24	2nd order TC of bridge resistance in case of temperature sensing via bridge current		TCR_{BR_2nd}	0	-	1/300	TCR_{BR}/K
25	sensitivity of sensor bridge (including TC)[11)]	(full scale span)	S_{IN}	3	-	84	mV_{pp}/V
26	sensor bridge offset		OFF	-3.75	-	+4.00	S_{IN}

[1)] This condition includes already error conditions at listed pins. For proper sensor operation narrower ranges are necessary, see further operating conditions.

[2)] Higher current at VDDA pin possible, as long as sum $|I_{VDDA\_EXT\_LD}| + |I_{EXHI\_pin}| < 5.5mA$.

[3)] C_{TSEN2} for filtering and EMC reasons. Suited value has to be chosen depending on specific application conditions. In very disturbed environments more sophisticated EMC filter circuitry may be necessary.

Note: If a capacitor is used, the ADC input charging is incomplete and average input current at pin TSEN2 produces following voltage drop $I_{TSEN2} \cdot R_{NTC}||R_{OP}$ as input voltage error. This may cause at very low temperatures additional errors in temperature reading, especially with high NTC impedance values.

[4)] Selection of R_{OP} so that NTC resistor divider is at about 50% in the middle of temperature range is optimal for ADC resolution (for example R_{OP}= R_{NTC}(55°C)). Self-heating of NTC and current consumption should be considered too, so that higher R_{OP} can be the better choice.
[5)] Range limited due to limits of "out of range" diagnosis and necessary precision for NTC formula linerization.
[6)] For EMC reasons a capacitance from input pins to ground may be necessary. For that case this limit should be fulfilled. It is necessary to ensure function of sensor open test. Care about symmetric capacitive load at corresponding input pins.
If larger EMC capacitors at these pins needed the sensor pin open test has to be disabled.
[7)] V_{EX}=V_{EXHI}-V_{EXLO} and V_{IN_CM} or V_{IN_BR} shall be related here not to VSS, but to V_{EXLO}, which can be some 100mV higher then VSS.
[8)] Every bridge sensor output signal (without any load) shall be in this range under consideration of offset and any possible pressure signal. This demand together with bridge impedance range is necessary to avoid diagnostic errors.
(Definition of unit V_{EX} see footnote above.)
[9)] Resistivity of parallel circuit of both bridges (or one, if single bridge setup used). Each single bridge shall not exceed given resistance **maximum** limit because of noise performance and necessary timing for bridge open diagnostic.
[10)] There are two bridge operating conditions R_{BR} and R_{BR_single} because of different demands to the bridges. For both bridges in parallel it is to consider the maximal current capability of EXHI and, if used, the TADC range for bridge current sensing. For each single bridge the resistivity is defined by limits to ensure correct open bridge detection.
Example: Two bridges with 3kΩ and 11kΩ are possible, but not with 1.5kΩ together with 2kΩ or 3kΩ together with 15kΩ.
[11)] Nominal the maximum adjustable input range is up to 112mV_{pp}/V. But due to discrete offset setting in worst case only up to 84mV_{pp}/V sensor signals can be adjusted. Range could be extended by additional resistors in EXHI and EXLO bridge supply lines. See 4.2.2-1 for selection of an appropriate GAIN matching the input range.

4 Electrical Characteristics

(V_{VS} = V_{VS_LOW} to V_{VS_HIGH}, T_A=-40°C to + 140°C, unless otherwise noted.
Typical values are at V_{VS}= 5.0V and T_A = +25°C. Positive currents flow into the device pins.)

4.1 SUPPLY - Power Supply and Reverse Polarity Protection

Table 4.1-1: Electrical Parameter Table SUPPLY

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	supply current	V_{VS}=5V; I_{EXHI}=I_{OUT}=0; I_{VDDA}=0;	I_{VS}		3.0	5.0	mA
2	analogue regulator output voltage, normal operation	I_{VDDA}=0..-1mA ext. load; 4.75<V_{VS}<5.25V	V_{VDDA}	3.8	4.0	4.2	V
3	analogue regulator output voltage in case of over-voltage	5.25<V_{VS}<35V	V_{VDDA_HV}	3.8	4.0	4.2	V
4	current limit at VDDA	V_{VDDA}=3V; I_{EXHI}=0	I_{VDDA_LIM}	-28	-	-15	mA
5	threshold for V_{VS} too low	V_{VS} falling	V_{VS_LOW}	4.3	4.5	4.7	V
6	threshold for V_{VS} too high	V_{VS} rising	V_{VS_HIGH}	5.4	5.7	6.0	V

4.2 PSEN_AFE / PADC_DIG - Sensor Analogue Front-End

4.2.1 Sensor Bridge Excitation and Current Sense

Table 4.2.1-1: Electrical Parameter Table PSEN_AFE: Sensor Excitation

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	excitation voltage drop from VDDA pin to EXHI pin	I_{EXHI}= -4mA; V_{VS}=5V	ΔV_{EXHI}	0.00	-	0.18	V
2	resistance from pin EXLO to VSSA, Mode 1[1)]	I_{EXLO}= +4mA; RSENSE=1	R_{EXLO_1}	72	87	102	Ω
3	resistance from pin EXLO to VSSA, Mode 2[2)]	I_{EXLO}= +2mA; RSENSE=2	R_{EXLO_2}	144	174	204	Ω
4	resistance from pin EXLO to VSSA, Mode 3[3)]	I_{EXLO}= +1mA; RSENSE=3	R_{EXLO_3}	250	300	350	Ω
5	short circuit current limit at pin EXHI	V_{EXHI} = 3.3V	I_{EXHI_LIM}	-10	-	-5.5	mA

[1)] Setting RSENSE=1 is recommended if bridge current sensing is not used (TCHANx<3), **or** for bridge resistances in range 0.9..4kΩ (when using bridge current sensing and PHALF1=PHALF2=0).
[2)] Setting RSENSE=2 is recommended if bridge current sensing is used **and** bridge resistances in range 1.9..8kΩ (if PHALF1=PHALF2=0).
[3)] Setting RSENSE=3 is recommended if bridge current sensing is used **and** bridge resistances in range 3.6..12kΩ (if PHALF1=PHALF2=0).

4.2.2 Sensor Signal Acquisition and Pressure ADC

Table 4.2.2-1: Electrical Parameter Table PSEN_AFE: Sensor Signal Acquisition

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	resolution for sensor bridge ADC[*)]		RES_{PADC}	-	15	-	bit
2	PADC update rate of 14 bit result[1)]		f_{PADC_UPDT}	-	3.91	-	kHz
3	3dB signal bandwidth of PADC[*)]	LPFC=1	BW_{PADC}	-	1	-	kHz

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
4	input range V_{INP}-V_{INN} for PGAIN=12[2)]	PGAIN = 0xC	$V_{S\_IN,12}$		7		mV_{pp}/V
5	input range V_{INP}-V_{INN} for PGAIN=11[2)]	PGAIN = 0xB	$V_{S\_IN,11}$		10		mV_{pp}/V
6	input range V_{INP}-V_{INN} for PGAIN=10[2)]	PGAIN = 0xA	$V_{S\_IN,10}$		14		mV_{pp}/V
7	input range V_{INP}-V_{INN} for PGAIN=9[2)]	PGAIN = 0x9	$V_{S\_IN,9}$		20		mV_{pp}/V
8	input range V_{INP}-V_{INN} for PGAIN=8[2)]	PGAIN = 0x8	$V_{S\_IN,8}$		28		mV_{pp}/V
9	input range V_{INP}-V_{INN} for PGAIN=4[2)]	PGAIN = 0x4	$V_{S\_IN,4}$		28		mV_{pp}/V
10	input range V_{INP}-V_{INN} for PGAIN=3[2)]	PGAIN = 0x3	$V_{S\_IN,3}$		40		mV_{pp}/V
11	input range V_{INP}-V_{INN} for PGAIN=2[2)]	PGAIN = 0x2	$V_{S\_IN,2}$		56		mV_{pp}/V
12	input range V_{INP}-V_{INN} for PGAIN=1[2)]	PGAIN = 0x1	$V_{S\_IN,1}$		80		mV_{pp}/V
13	input range V_{INP}-V_{INN} for PGAIN=0[2)]	PGAIN = 0x0	$V_{S\_IN,0}$		112		mV_{pp}/V
14	minimum offset of PADCx input range[3)]	POFFS = 0x10 (-16)	V_{POFFS_min}		-4.00		$V_{S\_IN,n}$
15	maximum offset of PADCx input range[3)]	POFFS = 0x0f (+15)	V_{POFFS_max}		+3.75		$V_{S\_IN,n}$
16	offset adjustment average step size of PADCx input range[4)]	(V_{POFFS_max} - V_{POFFS_min})/31	V_{POFFS_step}		0.25		$V_{S\_IN,n}$
17	ratio of internal half bridge resistor divider[5)]	PHALFx=1, POLx=0 meas. of V_{INNx}	Rat_{PHALF}	48	50	52	$\%V_{EX}$
18	signal-to-noise ratio for maximum band width (LPFC=1)[*) 6)]	PGAIN=0xA; 40mV span; noise BW=1kHz	SNR_{PADC}	-	65	-	dB
19	signal-to-noise ratio with medium band width (LPFC=3)[*) 6)]	PGAIN=0xA ; 40mV span; noise BW=210Hz	SNR_{PADC_250Hz}	-	70	-	dB
20	input equivalent noise in base band[*)]	PGAIN=0xA; 40mV span; nois. BW=1kHz	e_{IN}	-	7	-	μV_{rms}

[*)] Not tested in production
[1)] Derived from system clock oscillator. For timing tolerances see 4.8-1.
[2)] Usable input difference voltage range at pins INP and INN depending on programmed GAIN value in application. This includes voltage range for span **and** bridge offset combined. Indirect production test by measurement of PADC gain.
[3)] This means shift of center of input range related to this input range $V_{S\_IN,n}$ (see 6.3.2-2).
For lower gain settings not all offset settings are possible, see operating condition V_{IN_BR}.
[4)] This means shift of center of input range related to this input range $V_{S\_IN,n}$ (see 6.3.2-2).
[5)] Ratio calculated from: (V_{INNx}-V_{EXLO})/(V_{EXHI}-V_{EXLO})*100%
[6)] with:

$$SNR = 20 \cdot log_{10}\left(\frac{V_{span}}{2 \cdot \sqrt{2} \cdot e_{IN}}\right)$$

4.3 TSEN_AFE / TADC_DIG - Temperature Sensor Analogue Front-End

Table 4.3-1: Electrical Parameter Table TSEN_AFE: Temperature Signal ADC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	resolution for temperature ADC[*)]	TRES_LO=0	RES_{TADC}	-	14	-	bit
2	TADC update rate of 14 bit results for each T1 and T2[1)]	TRES_LO=0	f_{TADC_UPDT}	-	60	-	Hz

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
3	TADC input range low limit[2)]	TCHAN=2; TGAIN=2; calibrated; code=0x0000->0x0001	V_{T_REFL}	-0.2	-	+0.2	% V_{VDDA}
4	TADC input range high limit[2)]	TCHAN=2; TGAIN=2; calibrated; code=0x3FFE->0x3FFF	V_{T_REFH}	99.8	-	100.2	% V_{VDDA}
5	pull-down operating current at pin TSEN1		I_{TSEN1_PD}	15	20	25	µA
6	average input current at pin TSEN2 with TADC running[*)]	T_{SENS2}=2V; TCHAN=2; TGAIN=2; average	I_{TSEN2_IN}	-2.0	-1.4	-0.5	µA
7	TADC conversion time for 14 bit result[3)]	TRES_LO=0	t_{TADC_CONV}	-	6.55	-	ms

*) Not tested in production
1) Derived from system clock oscillator. For timing tolerances see 4.8-1.
Defined by the scheduler cycle rate. In this frequency ADC conversion of 2 channels are possible.
2) Indirect measurement. Parameters V_{T_REFL} and V_{T_REFH} define together offset and gain of TADC for the specified channels.
3) Derived from system clock oscillator. For timing tolerances see 4.8-1.

4.4 CORRECT - Digital Sensor Signal Processing

4.4.1 Pressure Sensor Signal Correction

Table 4.4.1-1: Electrical Parameter Table CORRECT: Bridge Sensor

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	update rate of bridge sensor acquisition[1)]		f_{PSEN_UPDT}	-	3.91	-	kHz

1) Derived from system clock oscillator. For timing tolerances see 4.8-1.

4.4.2 Sensor Temperature Signal Correction

Table 4.4.2-1: Electrical Parameter Table CORRECT: Temperature Sensor

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	error of temperature using internal diode[*) 1)]	TCHAN=0	$E_{T,INT}$	-2	-	+2	K
2	error of temperature using external diode[*)]	TCHAN=1	$E_{T,EXT}$	-2	-	+2	K
3	error of temperature using bridge resistance as temperature sensor[*) 2)]	TCHAN=3 TCR_{BR_2nd}= TCR_{BR}/1000	E_{T,I_EX}		1		K

*) Not tested in production
1) Calibration at customer side together and during sensor calibration process.
At delivery not calibrated.
2) For temperature sensing using the bridge resistance of the sensor attached, only sensor as specified in the recommended operating conditions (ch. 3) are suitable. For the given conditions and R_{BR} behavior according $R_{BR}(T) = R_{BR}(25°C) \cdot (1 + TCR_{BR} \cdot (T-25°C) + TCR_{BR\_2nd} \cdot (T-25°C)^2)$ the given tolerance can be achieved.

4.4.3 NTC Temperature Processing

Table 4.4.3-1: Electrical Parameter Table CORRECT: NTC Sensor

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	error of corrected NTC temperature[*) 1)]	T=0...100°C	$E_{T,NTC}$	-1.5	-	+1.5	K

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
2	error of corrected NTC temperature in extended temperature range*) 2)	T=125°C	$E_{T,NTC,125C}$	-2.5	-	+2.5	K
3	error of corrected NTC temperature in extended temperature range*) 2)	T=-40°C	$E_{T,NTC,-40C}$	-2.5	-	+2.5	K
4	update rate of NTC sensor evaluation3)		f_{NTC_UPDT}	-	60	-	Hz
5	NTC characteristic model parameter A*) 1)		1/A	-	300	-	K
6	NTC characteristic model parameter B*) 1)		1/B	-	3400	-	K
7	NTC characteristic model parameter C*) 1)		1/C	-	250e3	-	K

*) Not tested in production
1) It is assumed, the NTC characteristic fits the following formula:

$$T_{NTC}(R) = \frac{1}{A + B \cdot \ln\left(\frac{R}{R_0}\right) + C \cdot \ln^2\left(\frac{R}{R_0}\right) + D \cdot \ln^3\left(\frac{R}{R_0}\right)} \quad \text{with:} \quad R_0 = R(T_0) \quad \text{and} \quad T_0 = \frac{1}{A}$$

Operating point resistor set to $R_{OP} = 0.8 \cdot R_{NTC\_25}$.
2) Error limit line shows a linear behavior between -40°C and 0°C and between 100°C and 150°C (see 6.5.4-3). Assumed: Ideal NTC characteristic.
3) Derived from system clock oscillator. For timing tolerances see 4.8-1.

4.5 SENT_DIG / SENT_IF - SENT and Programming Interface

4.5.1 SENT Mode

Table 4.5.1-1: Electrical Parameter Table SENT_IF: SENT Mode

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	low state output voltage	I_{OUT} = 0.52 mA, measured at SENT-wire	$V_{OUT,OL}$	-	-	0.5	V
2	high state output voltage	I_{OUT} = -0.1 mA, measured at SENT-wire	$V_{OUT,OH}$	4.1	-	-	V
3	signal fall time (see 6.6.1.1-2) 1)	clock tick=3µs; from 3.8V->1.1V	t_{FALL}	-	-	6.5	µs
4	signal rise time (see 6.6.1.1-2) 1)	clock tick=3µs; from 1.1V->3.8V	t_{RISE}	-	-	18	µs
5	edge to edge jitter with static environment for any pulse period*)		Δt_{FALL}	-	-	0.1	µs
6	low state duration (see 6.6.1.1-2)*) 1)	clock tick=3µs, pulse low for 5 clock ticks	$t_{STABLE,LOW}$	6	-	-	µs
7	high state duration (see 6.6.1.1-2)*) 1)	clock tick=3µs, pulse high for 7 clock ticks	$t_{STABLE,HIGH}$	6	-	-	µs
8	tick time for SENT per LSB in TICKSEL[4:0] value2)	TICKSEL[4:0]=n $t_{TICK,LSB}=t_{TICK}/n$	$t_{TICK,LSB}$	0.94	1.00	1.06	µs/ LSB

*) Not tested in production
1) Measured at SENT-wire, receiver connected.
2) Derived from and checked with oscillator frequency.

4.5.2 SIO Mode (Serial Input Output)

Table 4.5.2-1: Electrical Parameter Table SENT_IF: SIO Mode

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	data baud rate[1)]		BR_{SIO}	-	14400	-	bit/s
2	SIO bit cycle time, transmitting		$t_{C,TX,SIO}$	61.0	68.0	76.0	µs
3	SIO bit low time, transmitting thresholds 40% V_{VS} falling to 60% V_{VS} rising	C_{OUT}=2.2nF	$t_{W,TX,L,SIO}$	0.45	0.50	0.55	$t_{C,TX.SIO}$
4	SIO bit cycle time, receiving		$t_{C,RX,SIO}$	58.0	69.4	79.0	µs
5	SIO bit low time, receiving		$t_{W,RX,L,SIO}$	0.45	0.5	0.55	$t_{C,RX,SIO}$
6	SIO input threshold at pin OUT (falling)	falling edge	$V_{THf,SIO}$	0.30	-	0.60	V_{VS}
7	SIO input threshold at pin OUT (rising)	rising edge	$V_{THr,SIO}$	0.40	-	0.70	V_{VS}
8	SIO input hysteresis at pin OUT[*)]		$V_{HYS,SIO}$	0.05	0.20	0.35	V_{VS}
9	SIO output low level at pin OUT	$I_{OL,SIO} \leq 0.5$ mA	$V_{OL,SIO}$	0.10	-	0.65	V
10	SIO output high level at pin OUT	$I_{OL,SIO} \geq -0.3$ mA	$V_{OH,SIO}$	3.9	-	5.5	V
11	Time window to enter configuration or diagnostic mode[1)]		t_{Window}	5.0	5.6	6.0	ms
12	SIO command timeout[1)]	max. duration of **one** command	$t_{timeout,SIO}$	9	10	11	ms

[*)] Not tested in production
[1)] Derived from and checked with system clock oscillator.

4.6 CONTROL - Digital Control, I2C Interface and Test Mode Logic

4.6.1 Inter IC Interface (I2C)

Table 4.6.1-1: I2C Interface: Electrical Parameter Table

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	SCL clock frequency (Fast mode I^2C bus)[1)]		f_{SCL}	-	-	400	kHz
2	logic input threshold for pins SDA, SCL (rising)	rising	V_{I2C_THr}	50	-	70	%VS
3	logic input threshold for pins SDA, SCL (falling)	falling	V_{I2C_THf}	30	-	50	%VS
4	hysteresis at inputs SDA, SCL[*)]		V_{I2C_HYS}	10	-	30	%VS
5	low level output voltage at SDA, SCL	I_{pin} = 3 mA	V_{I2C_OL}	0	-	0.4	V
6	input leakage current at pins SDA, SCL	$0 < V_{PIN} < V_{VS}$ (SDA tristate)	I_{I2C_LK}	-1	-	1	µA
7	input capacitance for pins SDA, SCL[*)]		C_{I2C_IN}	-	-	10	pF
8	output fall time of SDA signal[*)]	C_{LOAD}< 400pF s. 6.7.1-1	t_{I2C_FALL}	20	-	120	ns

[*)] Not tested in production
[1)] checked with worst case pattern

4.7 NVM - Non-Volatile Memory

Table 4.7-1: Electrical Parameter Table Memory

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	NVM array size x 16 bit*)	for info only	N_{NVM}	-	128	-	Word
2	endurance (write cycles)*)		N_{PROG}	1000	-	-	1
3	data retention time*) 1)		t_{NVM_ret}	15		-	year

*) Not tested in production
1) Permissible temperature profile as follows, e.g.
Operating (12000h total), with:
$T_{j,op}$ = -40°C, t < 720h
-40 °C < $T_{j,op}$ ≤ 25 °C, t < 2400h
25 °C < $T_{j,op}$ ≤ 100°C, t < 7800h
100 °C < $T_{j,op}$ ≤ 150°C, t < 1080h
add 13.6 years non-operating within -40 < Tj ≤ 85°C

4.8 OSC - Oscillator

Table 4.8-1: Electrical Parameter Table OSC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	core frequency of internal oscillator		f_{CLK}	9.5	10.0	10.5	MHz

4.9 Functional Safety

4.9.1 Safety Measures and Diagnosis

Table 4.9.1-1: Electrical Parameter Table: Safety Measures and Diagnosis

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	period of BIST and diagnosis cycle including BISTs according 6.10.1.2-1*) 1)		t_{BIST_CYC}	-	4.2	-	ms
2	period of temperature related BISTs, see 6.10.1.2-1 (all BISTs enabled)*) 2)		t_{T_BIST}	-	17	-	ms
3	period of ROM (OTP) BIST*) 2)		t_{ROM_BIST}	-	4.5	-	ms

*) Not tested in production
1) Cycle time of most diagnostic and cyclical BIST checks. Details see in chapter 6.10. Derived from system clock oscillator. For timing tolerances see 4.8-1.
2) Derived from system clock oscillator. For timing tolerances see 4.8-1.

4.9.2 Bridge Sensor Diagnosis - SM21

Table 4.9.2-1: Electrical Parameter Table: Bridge Diagnostics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	diagnostic threshold "too low" at INP1/2, INN1/2 1)	DIAG=0x4/6/C/E	$V_{IN\_DIAG\_L}$	0.17	0.20	0.23	V_{EX}
2	diagnostic threshold "too high" at INP1/2, INN1/2 1)	DIAG=0x5/7/D/F	$V_{IN\_DIAG\_H}$	0.77	0.80	0.83	V_{EX}
3	threshold "short to higher voltage" at EXLO	DIAG=0x3/B	V_{EXLO_DIAG}	0.17	0.20	0.23	V_{VDDA}
4	threshold "short to lower voltage" at EXHI	DIAG=0x2/A	V_{EXHI_DIAG}	0.77	0.80	0.83	V_{VDDA}
5	switchable pull-up resistor at pins INN1/2, INP1/2 to VDDA	PU_PSEN1/2=1	R_{IN_PU}	20	25	30	kΩ

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
6	switchable pull-down resistor at pins INN1/2 to VSSA	PD_PSEN1/2=1	R_{INN_PD}	30	60	100	Ω

[1] $V_{EX} = V_{EXHI}-V_{EXLO}$ are related to V_{EXLO} (not VSSA). V_{EXLO} can be several 100mV above VSSA.

4.9.3 NTC Sensor Diagnosis - SM22, SM23

Table 4.9.3-1: Electrical Parameter Table: NTC Sensor Diagnosis

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	switchable pull-up resistor at pin TSEN2 to VDDA	PUD_TSEN=1; DIAG[0]=0	R_{TSEN2_PU}	15	20	25	kΩ
2	switchable pull-down resistor at pin TSEN2 to VSSA	PUD_TSEN=1; DIAG[0]=1;	R_{TSEN2_PD}	15	20	25	kΩ
3	out-of-range indication of NTC input, recommended lower limit[*] [1]	RTx_LIM[7:0]= 0x06	V_{NTC_MIN}	-	2.3	-	%FS TADC
4	out-of-range indication of NTC input, recommended upper limit[*]	RTx_LIM[15:8]= 0xFA	V_{NTC_MAX}	-	97.7	-	%FS TADC

[*] Not tested in production
[1] For NTC sensors a divider of R_{NTC} and R_{OP} between VSSA and VDDA is connected to TSEN2 (Parameter TGAIN2 = 2).
Example: If VDDA=4V and NTC-voltage out of range enabled (RT2_ERR=1), input voltages below about 2.3% * 4V = 92mV at TSEN2 are detected as range error (for instance due to short TSEN2 to VSS or divider open at VDDA).

4.9.4 Diode Sensor Diagnosis - SM24

Table 4.9.4-1: Electrical Parameter Table: Diode Sensor Diagnosis

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	threshold for temperature diode forward voltage for "diode shorted"; recommended limit[*] [1]	RTx_LIM[7:0]= 0x13 TGAINx=0 or 1	V_{DIO_SHORT}	-	0.1	-	V
2	threshold for temperature diode forward voltage for "diode open" indication; recommended limit[*] [1]	RTx_LIM[15:8]= 0xE6 TGAINx=0 or 1	V_{DIO_OPEN}	-	1.2	-	V
3	threshold for overtemperature error[*] [2]		T_{OT_ERR}	150	158	166	°C

[*] Not tested in production
[1] Applied TADC limits depending on NVM setting of RT1_LIM or RT2_LIM and selected TGAIN range.
Only for information: Checked indirectly by TADC measurement.
[2] Indirect measurement at lower temperature.

5 Register Overview Table

Addr	Name	Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x70	DIAG_RES1	0x00	OPINP1	OPINN1	SHBRL	SHBRH	INP1EXHI	INP1EXLO	INN1EXHI	INN1EXLO
0x71	DIAG_RES2	0x00	OPINP2	OPINN2	-	-	INP2EXHI	INP2EXLO	INN2EXHI	INN2EXLO
0x72	ERRC1	0x00	PV_ERR	TV_ERR	V5H_ERR	V5L_ERR	-	TSP_ERR	PSP2_ERR	PSP1_ERR
0x73	ERRC2	0x00	S42_ERR	S32_ERR	S22_ERR	S02_ERR	S41_ERR	S31_ERR	S21_ERR	S01_ERR
0x74	ERRC3	0x00	-	NOP_ERR	RT2_ERR	RT1_ERR	T2_SAT	T1_SAT	P2_SAT	P1_SAT
0x75	ERRC4	0x00	OT_ERR	VSM_ERR	-	-	S1_ERR	TC1_ERR	PC2_ERR	PC1_ERR
0x76	ERRC5	0x00	-	NV3_ERR	NV2_ERR	NV1_ERR	-	-	-	-
0x77	I2C_CTRL SFR and NVM	0x60	-	SCL_OUT	SDA_OUT	CCP_LCK	I2C_ADR[1:0]		I2C_ENA	I2C_MODE
0x78	PGAIN1 SFR and NVM	0x00	POL1	PHALF1	RSENSE[1:0]		PGAIN1[3:0]			
0x79	POFFS1 SFR and NVM	0x20	LPFC[2:0]			POFFS1[4:0]				
0x7A	PGAIN2 SFR and NVM	0x00	POL2	PHALF2	-	P2OFF	PGAIN2[3:0]			
0x7B	POFFS2 SFR and NVM	0x00	-	-	-	POFFS2[4:0]				
0x7C	SENTCONF1 SFR and NVM	0x00	FC_MODE[2:0]			TICKSEL[4:0]				
0x7D	SENTCONF2 SFR and NVM	0x00	SC_MODE	SC_CONF	NPP	-	-	-	-	-
0x7E	SENTCONF3 SFR and NVM	0x00	PP_LEN[7:0]							
-	T1_MODE NVM	0x00	IDIO_OFF	-	-	-	TCHAN1[1:0]		TGAIN1[1:0]	
-	T2_MODE NVM	0x00	-	-	-	CORR2	TCHAN2[1:0]		TGAIN2[1:0]	
-	SENTCONF4 NVM	0x00	-	-	FC2_SRC[2:0]			FC1_SRC[2:0]		
-	ERR_EN1 NVM	0x00	PV_EN	TV_EN	V5H_EN	V5L_EN	CAP_EN	TSP_EN	PSP2_EN	PSP1_EN
-	ERR_EN2 NVM	0x00	S42_EN	S32_EN	S22_EN	S02_EN	S41_EN	S31_EN	S21_EN	S01_EN
-	ERR_EN3 NVM	0x00	-	NOP_EN	RT2_EN	RT1_EN	T2SAT_EN	T1SAT_EN	P2SAT_EN	P1SAT_EN
-	ERR_EN4 NVM	0x00	OT_EN	VSM_EN	-	-	S1_EN	TC1_EN	PC2_EN	PC1_EN

6 Functional Description

6.1 Overview

The sensor signal processor (SSP) 520.47 as shown in 6.1-1 contains an analogue front-end for the inputs of two differential resistive bridges and one or two out of 4 different temperature sensors, a digital compensation unit and a SENT data interface block. Supporting circuits are voltage regulators, overvoltage and reverse voltage protection and monitor hardware units and a non-volatile memory block (NVM) for storage of individual device settings (configuration and sensor calibration data, ID-code).
Primary inputs are the differential signals from two resistive pressure sensor bridges which are fed to two parallel high resolution AD-converter, called PADC1 and PADC2 (pressure ADC). These PADC input ranges are separately programmable in offset and gain (or input span). The excitation of the resistive sensor bridge is provided by a stabilized voltage output.
Temperature signals from an internal T-sensor, external diode, external NTC resistor divider or bridge current are fed via a multiplexer to a further AD-channel TADC (temperature ADC), which can convert one or two of these 4 temperature input sources to allow thermal calibration of the bridge sensor including optional 2nd redundant temperature value (for later comparison with the first one).
The one or two selected temperature sensors are processed by the same TADC in time multiplex.
The subsequent compensation calculator engine applies a thermal correction and linearization algorithm to the acquired both bridge signals providing two temperature independent, highly linear outputs p_1 and p_2. Sensor specific parameters of the correction algorithm from device or batch specific measurements are transferred to the embedded NVM of the IC via a serial data-I/O (SIO) sharing its pin with the SENT data output at pin OUT. Access to internal data registers and programming of configuration or calibration data is also possible through an I2C compatible interface at pins SDA and SCL.
Output of the SSP is provided via SENT data interface according to the **standard SAE J2716**, APR2016. Here, different SENT sensor classes can be configured to provide output of pressure and temperature data in the fast message channel and supplementary data in the enhanced serial message channel.

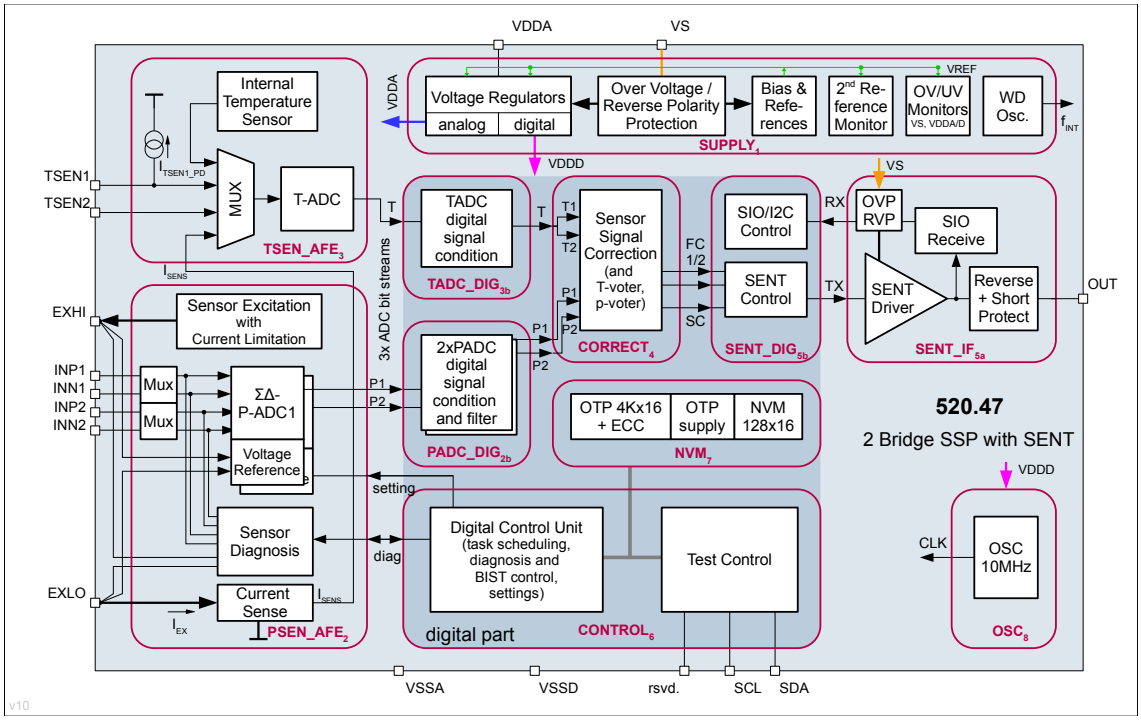


Figure 6.1-1: SSP Simplified Block Schematic

6.2 SUPPLY - Power Supply and Reverse Polarity Protection

The IC operates from a 5V-supply with internal over voltage protection (OVP) and reverse voltage protection (RVP). The protection circuitry prevents damage to the device in case of overvoltage at the supply input VS. Also a low-drop reverse protection circuit is integrated which blocks negative voltages from the internal circuitry.

An integrated linear voltage regulator with output at pin VDDA generates a 4V stabilized voltage to supply the analogue precision circuitry including the sensor excitation unit. A current limitation with threshold I_{VDDA_LIM} at the regulator output pin prevents destruction in case of short circuit to ground. This regulator requires an external bypass capacitor to ground for HF-rejection. The pin VDDA is intended to connect this capacitor C_{VDDA} and optionally a resistor divider with NTC temperature sensor. In sum maximal load current $I_{VDDA\_EXT\_LD}$ can be drawn from VDDA pin.

An additional on-chip regulator for the digital circuit blocks is integrated (VDDD) but with internal connections only.

The external capacitor C_{VS} at the main supply input VS is recommended to block fast transients from the IC and for EMC requirements.

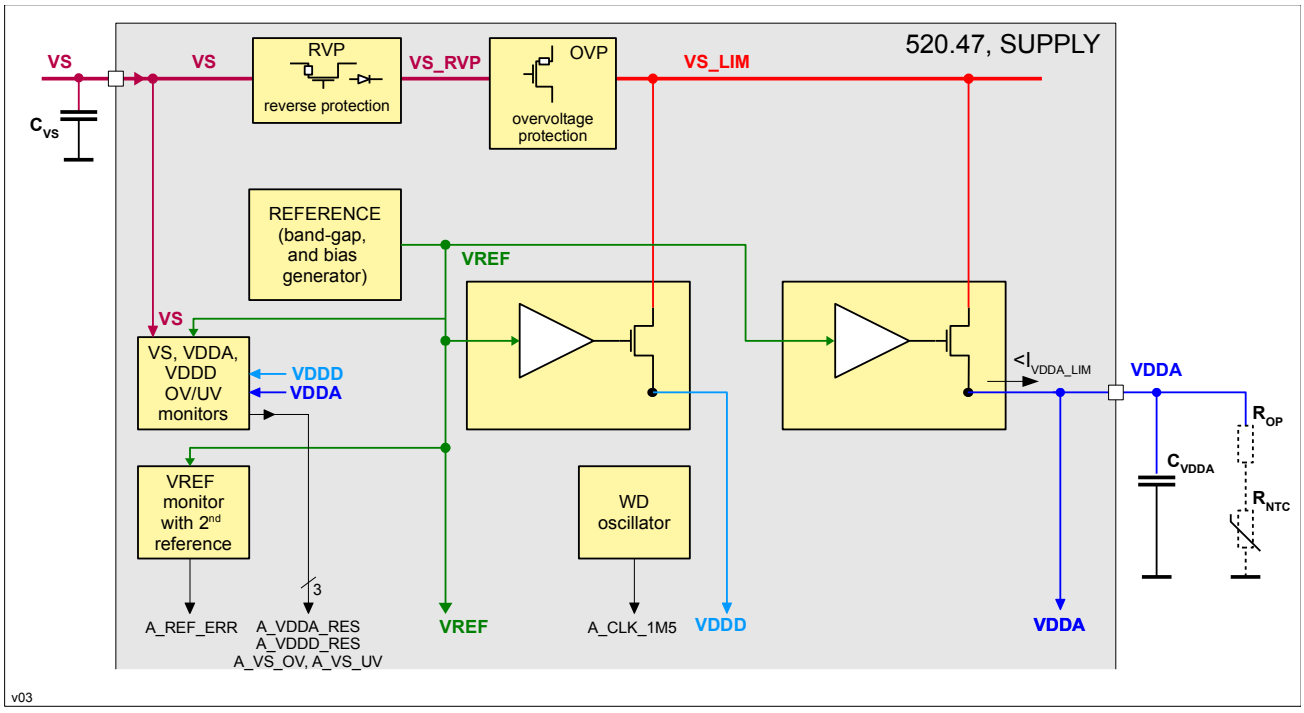


Figure 6.2-1: Simplified Schematic of SUPPLY Block

The SUPPLY block provides beside overvoltage (OVP) and reverse polarity protection (RVP):

- an internal reference and bias generation
- a 4.0V regulators for analogue VDD
- a 1.8V regulator for digital VDD
- overvoltage and undervoltage monitor circuits for V_{DDA} and V_{DDD} regulator outputs
- supply monitor for VS over- and undervoltage
- a monitor for the primary reference VREF against another 2nd reference regarding overvoltage and undervoltage
- an additional oscillator working as clock for watchdog for control logic

Supply Monitors

Next figure shows, how reset thresholds for rising and falling V_{VDDA} resp. V_{VDDD} and monitor thresholds for V_{VS} are defined.

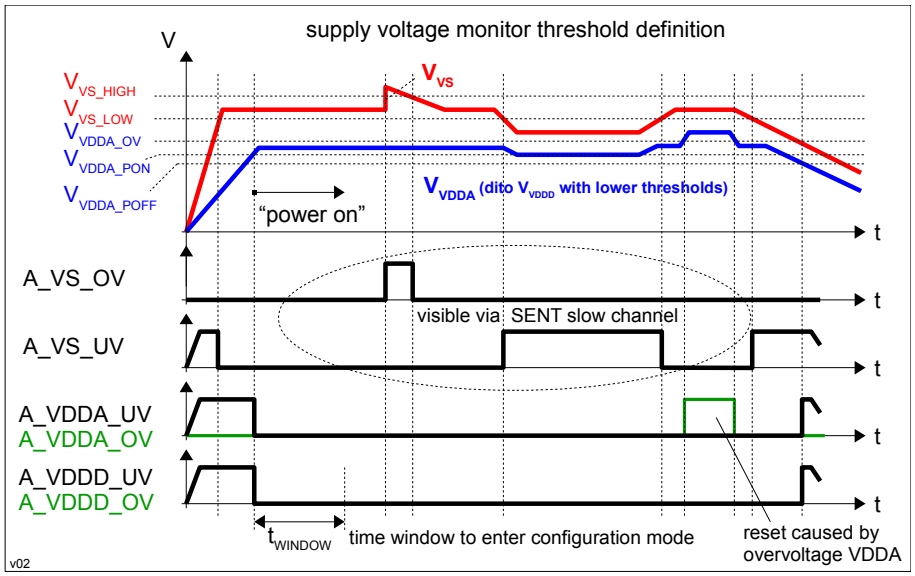


Figure 6.2-2: Supply Monitor Threshold Definitions

The overvoltage or undervoltage case at the supply VS is copied to the bits **V5H_ERR** and **V5L_ERR** of register ERRC1, if the corresponding enable bits **V5H_EN** and **V5L_EN** are set in NVM register ERR_EN1. In the slow channel SENT message this information will be sent as diagnostic error code (VS overvoltage or undervoltage), see 6.6.1.4-1.

Undervoltage or overvoltage at the 4V-regulated V_{VDDA} or internal 1.8V-regulated V_{VDDD} will trigger a reset of the IC.

Beside the asynchronous monitor signals above there are further synchronous generated reset pulses caused by safety measures. For details see chapter 6.10.1.2.

Reset State:

The reset state is considered as safe state. The SENT output at pin OUT is tri-state (high-ohmic) during reset state.

6.3 PSEN_AFE / PADC_DIG - Sensor Analogue Front-End

This chapter describes the pressure sensor analogue front-end named PSEN_AFE.
The main structure of the block is shown in following figure:

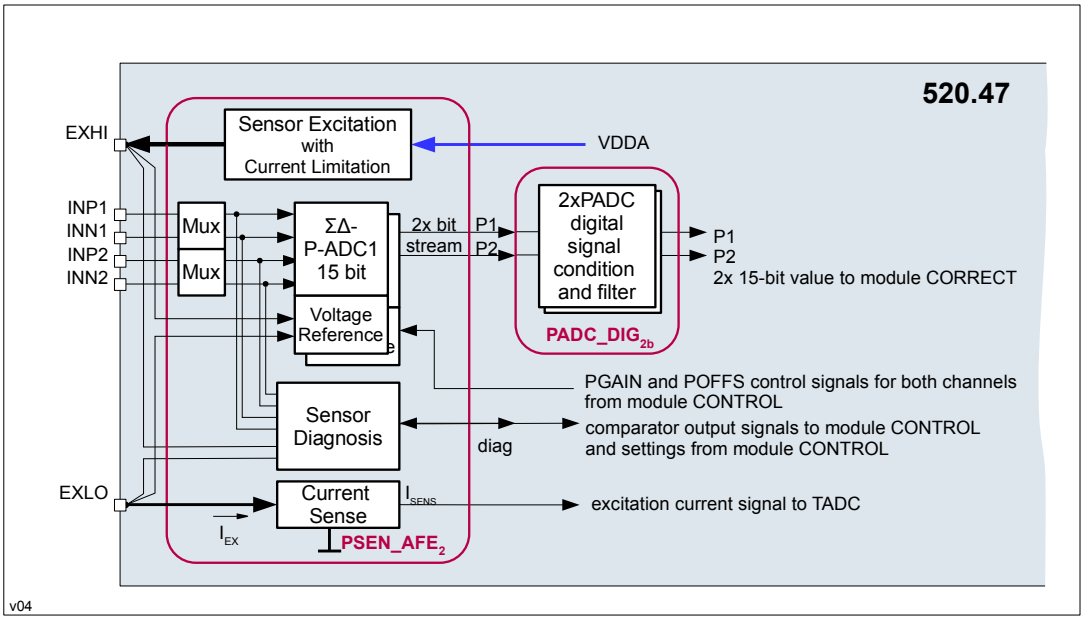


Figure 6.3-1: Overview Block PSEN_AFE

The functions of the blocks are:

- supply of sensor bridge with current limitation
- 2x bridge differential signal pre-conditioning for ADC
- 2x 15-bit pressure signal ADC with adjustable input range and offset (PADC1 and PADC2)
- bridge and block function diagnostics

Details are described in following sub-chapters.

6.3.1 Sensor Bridge Excitation and Current Sense

The sensor bridge is supplied with constant voltage between positive excitation EXHI and ground pin EXLO.

The voltage source at pin EXHI is derived from internal analogue regulator output voltage V_{VDDA}. The bridge supply block EXHI_SW basically forms a switch to VDDA with a low voltage drop ΔV_{EXHI} and a current limitation at I_{EXHI_LIM}.

Voltage difference between pins EXHI and EXLO is used by both subsequent pressure signal ADCs (PADC1 and PADC2) as reference potentials as shown in 6.3.1-1. In case of temperature measurement selected by measuring the excitation current I_{EX} the same potentials are used as reference by the temperature signal ADC (TADC).

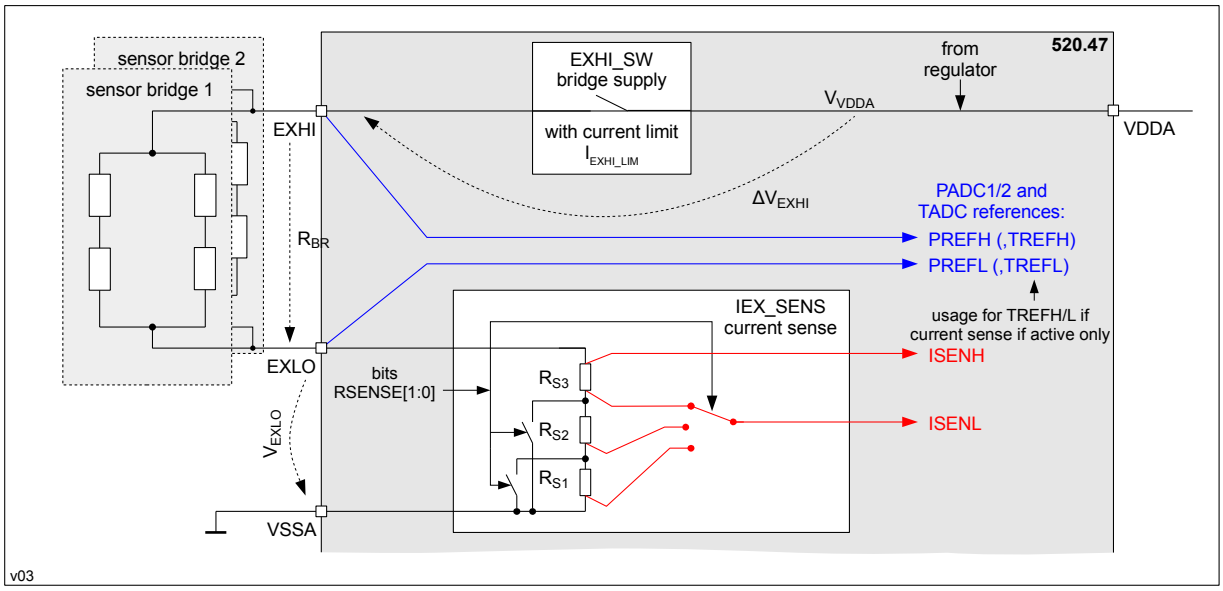


Figure 6.3.1-1: Overview Sensor Bridge Excitation

On the lower side of the bridge low ohmic shunt resistors R_{S1}, R_{S2} and R_{S3} to ground pin VSSA are placed. These are used to sense the excitation current, if used for TADC. To cover the wide range of possible effective bridge resistances (both bridges in parallel), there are two control bits **RSENSE[1:0]** to switch between three different shunt resistances R_{EXLO_1}, R_{EXLO_2} and R_{EXLO_3}.

The bits **RSENSE[1:0]** has to be set to 0b01 (in NVM memory) at these conditions:
- for low bridge resistances
- if excitation current I_{EX} is NOT used for temperature sensing (to minimize the drop at pin EXLO).

The voltage drop at the shunt is fed to the temperature converter TADC, if excitation current sensing is selected as temperature measurement channel.

If temperature measurement via sensing of bridge current at EXLO shall be used, the setting of suited sense resistance depends on minimum reached bridge resistance over temperature range and if optional internal half bridges are used, which would create additional EXLO current.
A recommendation for the proper setting of one out of three different sense resistors by RSENSE[1:0] is shown in the table below.

Table 6.3.1-1: Detailed Recommendations for RSENSE Setting

RSENSE[1:0]	***typ. R_S***	***$R_{BR,min}$ for PHALF1=0 PHALF2=0***	***$R_{BR,min}$ for PHALF1=0(1) PHALF2=1(0)***	***$R_{BR,min}$ for PHALF1=1 PHALF2=1***
0,1	87 Ω	> 0.9 kΩ	> 0.95 kΩ	> 1.0 kΩ
2	174 Ω	> 1.9 kΩ	> 2.2 kΩ	> 2.5 kΩ
3	300 Ω	> 3.6 kΩ	> 4.6 kΩ	> 6.3 kΩ

For the case PHALF1=PHALF2=0 (internal half bridges are not activated) see also recommendations in 4.2.1-1. There are recommended maximum bridge resistances too for the different ranges. This is because the largest sense resistor should be used to optimize the temperature measurement resolution.

6.3.2 Sensor Signal Acquisition and Pressure ADC

The data acquisition for pressure sensor bridge and signal flow for both PADCs is shown below.

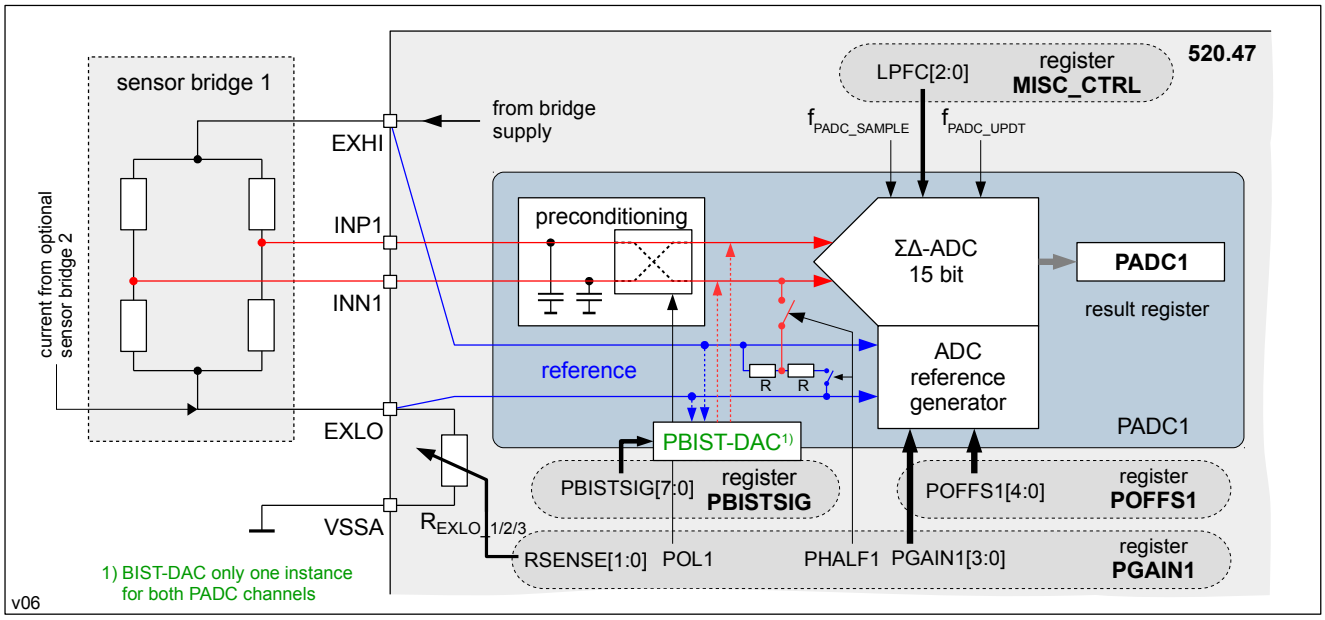


Figure 6.3.2-1: Overview Pressure Sensor Signal Acquisition and PADC

PADC2 has the same structure as PADC1. Elements drawn with suffix "1" in name, identically exist with suffix "2".

The voltages at pins EXHI and EXLO are used to derive proportional references for Sigma-Delta ADC full scale. For flexibility the polarity of INN1/P1 and INN2/P2 inputs can be inverted by setting bit **POL1/2** in registers PGAIN1 or PGAIN2.

As depicted in the figure above, with the control bit **PHALF1/2** for each channel a "half bridge" operation mode can be selected. If enabled the single input INP1 and/or INP2 will be evaluated against internal provided 50% resistive divider between EXHI and EXLO. The corresponding negative input INN1 and/or INN2 shows the internal generated half bridge reference voltage and has to stay high ohmic in that mode.

The input range regarding span and offset can be adjusted by setting bits **PGAIN1/2[3:0**] and **POFFS1/2[4:0**] from registers **PGAINx** and **POFFSx** defined in subsequent tables:

Table 6.3.2-1: Gain and offset setup registers SFR and NVM

Register Name	*Address*	*Description*
PGAIN1 SFR and NVM	0x78	gain control register for P1 sensor front-end (copied from **NVM**)
POFFS1 SFR and NVM	0x79	offset control register for P1 sensor front-end (copied from **NVM**)
PGAIN2 SFR and NVM	0x7A	gain control register for P2 sensor front-end (copied from **NVM**)
POFFS2 SFR and NVM	0x7B	offset control register for P2 sensor front-end (copied from **NVM**)

Table 6.3.2-2: Register **PGAIN1** SFR and NVM (0x78) gain control register for P1 sensor front-end (copied from **NVM**)

	MSB							***LSB***
Content	POL1	PHALF1	RSENSE[1:0]		PGAIN1[3:0]			
Reset value	0	0	00		0000			
Access	R/W	R/W	R/W		R/W			
Bit Description	**POL1** : swaps polarity of inputs INP and INN: 1: INP to "-" and INN to "+" **PHALF1** : switches negative input of PADC1 to internal 50% divider between EXHI and EXLO 1: ADC-input to 50% 0: ADC-input to INN1 (or INP1 if POL1=1) **RSENSE[1:0]** : selection of current sensing resistance (details see in 4.2.1-1) **0** or **1**: R_{EXLO_1} ca. 87Ω (selection for low ohmic bridges or if no current sensing is used) **2**: R_{EXLO_2} ca. 174Ω (for medium ohmic bridges) **3**: R_{EXLO_3} ca. 300Ω (for high ohmic bridges) **PGAIN1[3:0]** : sensor ADC gain adjust for channel 1; 10 valid settings: 0,1,2,3,4,8,9,10,11,12; (details see in 4.2.2-1) => **PGAIN1[3]**: coarse 4:1 gain switch => **PGAIN1[2:0]**: fine stepping from 0...4 in about sqrt(2) relative steps ==> here invalid settings 5,6,7 are mapped to setting 4 **Note**: Setting 4 and 8 cause approximately same gain. Here setting 8 provides higher differential input resistance at INP1 to INN1, and might show overall slightly lower signal noise.							

Table 6.3.2-3: Register **PGAIN2** SFR and NVM (0x7A) gain control register for P2 sensor front-end (copied from **NVM**)

	MSB							***LSB***
Content	POL2	PHALF2	-	P2OFF	PGAIN2[3:0]			
Reset value	0	0	0	0	0000			
Access	R/W	R/W	R	R/W	R/W			
Bit Description	**POL2** : swaps polarity of inputs INP and INN: 1: INP to "-" and INN to "+" **PHALF2** : switches negative input of PADC2 to internal 50% divider between EXHI and EXLO 1: ADC-input to 50% 0: ADC-input to INN2 (or INP2 if POL2=1) **P2OFF** : disables PADC2 channel to save current consumption 1: disable **PGAIN2[3:0]** : sensor ADC gain adjust for channel 2; 10 valid settings: 0,1,2,3,4,8,9,10,11,12; => **PGAIN2[3]**: coarse 4:1 gain switch => **PGAIN2[2:0]**: fine stepping from 0...4 in about sqrt(2) relative steps ==> here invalid settings 5,6,7 are mapped to setting 4 **Note**: Setting 4 and 8 cause approximately same gain. Here setting 8 provides higher differential input resistance at INP2 to INN2, and might show overall slightly lower signal noise.							

Table 6.3.2-4: Register **POFFS1** SFR and NVM (0x79) offset control register for P1 sensor front-end (copied from **NVM**)

	MSB							***LSB***
Content	LPFC[2:0]			POFFS1[4:0]				
Reset value	001			00000				
Access	R			R/W				
Bit Description	**LPFC[2:0]** : 2nd order low-pass filter coefficient k (for both ADC channels) **POFFS1[4:0]** : sensor ADC offset adjust for channel 1, 32 settings with steps of about 25%FS of input span (depending on gain setting)							

Table 6.3.2-5: Register **POFFS2** SFR and NVM (0x7B) offset control register for P2 sensor front-end (copied from **NVM**)

	MSB							***LSB***
Content	-	-	-	POFFS2[4:0]				
Reset value	0	0	0	00000				
Access	R	R	R	R/W				
Bit Description	**POFFS2[4:0]** : sensor ADC offset adjust for channel 2, 32 settings with steps of about 25%FS of input span (depending on gain setting)							

By use of control bits **POFFS1/2[4:0]** and **PGAIN1/2[3:0]** the bridge voltage input range for $\Delta V_{IN} = (V_{INP} - V_{INN})$ can be adjusted optimally in 1 out of 320(=10*32) different ranges independent for both channels PADC1 and PADC2. The following two figures depict the definition of different input ranges for

- all possible gains (with fix offset setting) and for
- all possible offsets (with fix gain setting)

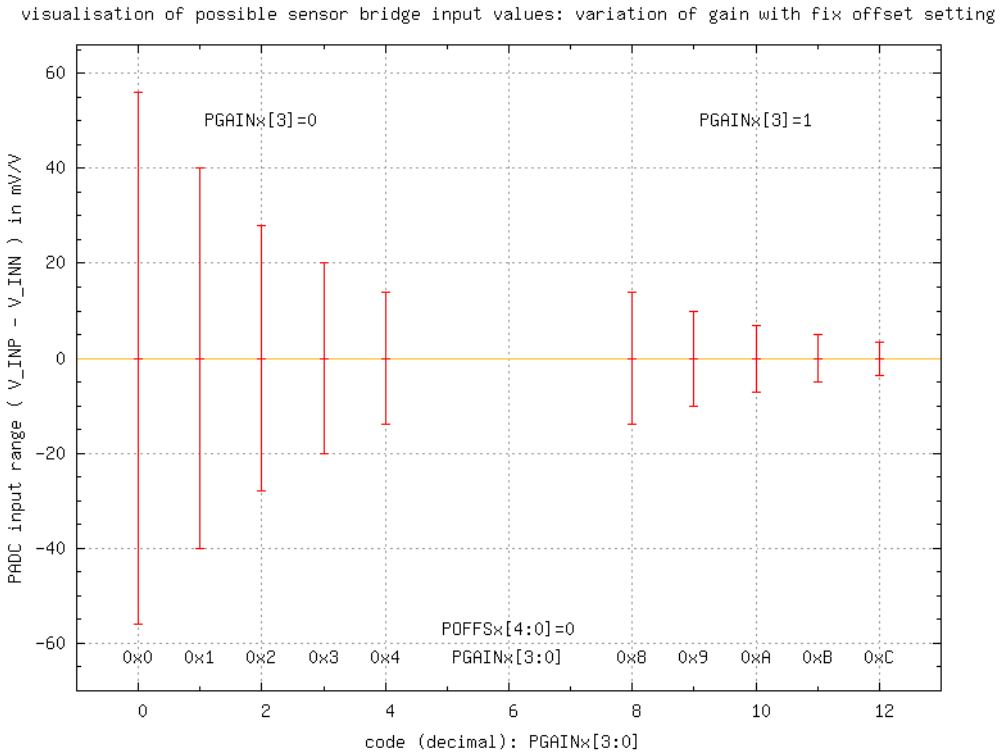


Figure 6.3.2-2: Plot of Selectable Differential Input Ranges (Gains), see also 4.2.1-1

Note:
PGAINx=4 and PGAINx=8 have same gain respectively input range. Here PGAINx=8 is recommended because of higher input impedance of PADC and slightly better noise performance for this setting PGAINx=8.

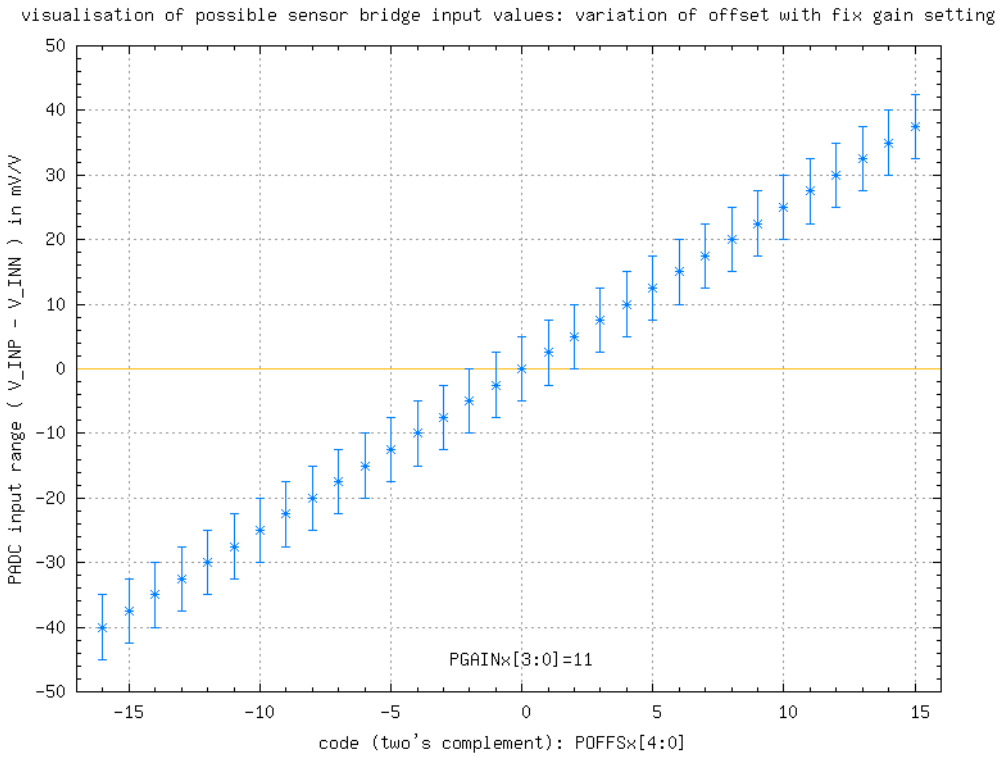


Figure 6.3.2-3: Plot of Selectable Differential Input Ranges (Offsets), see also 4.2.1-1

The figures above show input ranges under typical conditions. The vertical lines represent the permissible input voltages on y-axis, which are mapped onto the ADC output range from 0 LSB (lower end) to 2^{15}-1 LSB (upper end of line), with the polarity bit **POLx** set to 0. With **POLx=1** the mapping of input difference voltage to PADC results is inverse.

The step size of gain and offset is chosen in a way to have a **wide range of input differential voltages** mapped optimally to the ADC range. With the optimal setting the span should always cover about 60...100% of ADC range to have the best possible resolution.

6.3.3 Digital Low-pass Filter

After the decimation filter-stage, the sensor signal is low-pass filtered in a 2nd order digital filter for each pressure signal channel. This filter can be configured by the bits **LPFC[2:0]** of the register POFFS1.

The data in **LPFC[2:0]** herein defines the -3dB-corner frequency f_c as listed below.

Table 6.3.3-1: Digital Low-pass Filter: -3dB corner frequency

Setting LPFC[2:0]	*3-dB Frequency f_C (nominal)*	*Settling Time 10% to 90% (typ.)* [1)]
0b000 = 0	disable LP filtering (not recommended)	-
0b001 = 1	1092 Hz	<1 ms
0b010 = 2	459 Hz	1.0 ms
0b011 = 3	213 Hz	1.9 ms
0b100 = 4	104 Hz	3.4 ms
0b101 = 5	51 Hz	6.7 ms
0b110 = 6	26 Hz	13 ms
0b111 = 7	13 Hz	27 ms

[1)] The settling time includes the analog front-end and digital filter, only. For the complete data transmission to a host processor an additional delay of 100 us in the signal correction engine plus the duration of max. 2 fast channel SENT messages needs to be added (latency time).

The tolerance of the -3dB-corner frequency equals the tolerance of the master clock frequency f_{CLK}.
A slower filter setting improves the signal to noise ratio (SNR) of the PADC results.
Setting the register content **LPFC=0** completely bypasses the low-pass filter, which is not recommended.

The simulated step response for the fastest 4 filter settings is shown in the following figure.
There it is to consider, that even the fastest SENT protocol timing gives a limited data update rate of about 1/850µs (with 3µs and pause pulse setting).

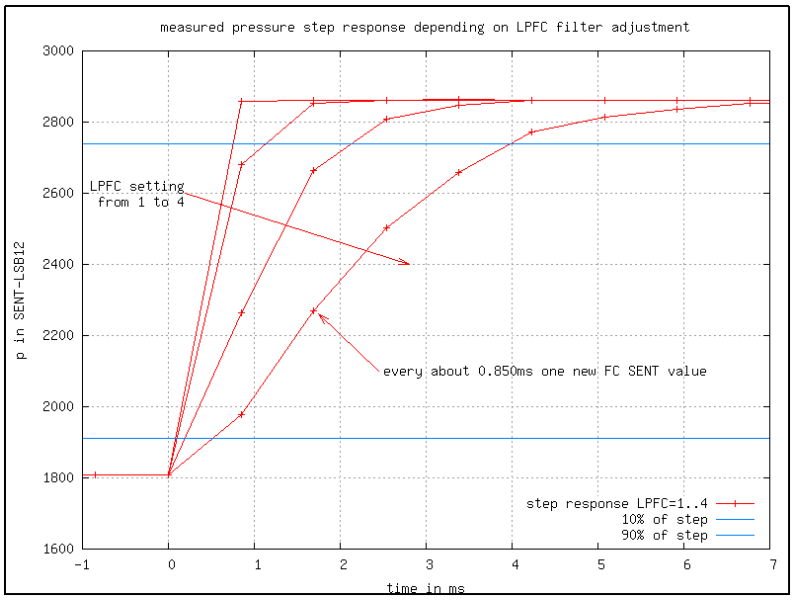


Figure 6.3.3-1: Pressure Step Response Behaviour

6.4 TSEN_AFE / TADC_DIG - Temperature Sensor Analogue Front-End

The temperature sensor analogue front-end TSEN_AFE acquires and pre-processes different temperature signals and has the following general tasks:

- bridge temperature measurement suited for bridge sensor TC calibration
- 2nd redundant bridge temperature measurement for functional safety application (to compare with the 1st value with means of a temperature voter)
- alternatively a precise absolute media temperature measurement or other temperature value

The next figure depicts the implemented simplified block schematic of this block. This also shows the input and reference potentials used for different channels selected:

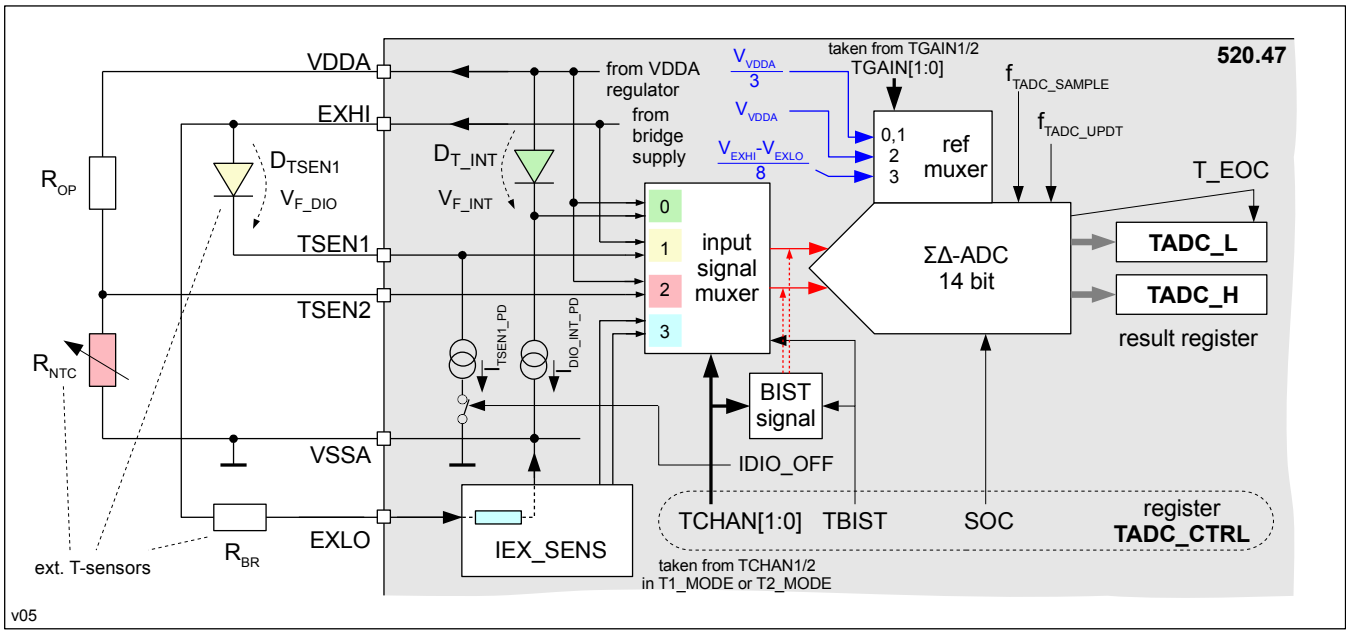


Figure 6.4-1: Overview Temperature Sensor Analogue Front-end TSEN_AFE

For the optional external diode D_TSEN1 an operating pull-down current I_{TSEN1_PD} will be provided by the IC. The possible range of diode forward voltages for given operating current defines V_{F_DIO}.

The NTC element at pin TSEN2 is defined by $R_{NTC\_25} = R_{NTC}(25°C)$, characteristic model parameters A,B,C,D and a constant resistor R_{OP} to form an appropriate voltage divider (details see chapter 3 and chapter 6.5.4).

Bridge current sensing is done via a configurable shunt resistor $R_{EXLO\_1}/R_{EXLO\_2}/R_{EXLO\_3}$ controlled by bits **RSENSE[1:0]** (see chapter 6.3.1). See definition of R_{BR} range in chapter 3 for hints for suited setting of range switching bits **RSENSE**.

Logical Temperature Channels T1 and T2:

We have two **logical** temperature channels T1 and T2 which are measured sequentially within one temperature measurement and temperature BIST cycle T_{T_BIST}.

Logical channel T1 is used for pressure sensor temperature compensation. In safety applications channel T2 shall be used as second, different temperature sensor for the sensor temperature to compare with (see temperature voter in chapter 6.10.16). Otherwise another temperature (for example media temperature) can be measured with channel T2.

With the NVM setting bits **TCHAN1[1:0]** and **TCHAN2[1:0]** each logical temperature channel can be mapped onto a **physical** channel. The channel at pin TSEN2 is suited for different external connected temperature sensors, like diodes or resistor dividers with NTC or PTC. The pin TSEN1 is mainly specialized for external diode sensors connected to EXHI voltage.

The following table gives an overview for the different possible set-ups:

Table 6.4-1: Temperature Sensor Overview

physical channel =>	***internal diode***	***diode at TSEN1***	***diode at TSEN2***	***PTC/... at TSEN2***	***NTC at TSEN2***	***I_EX: bridge current***
logical channel:						
[1)] T1	x	x	x	x	-	x
T2	x	x	(x)	x	x	x
necessary settings:						
TCHAN1 or **TCHAN2**	0	1	2	2	2	3
TGAIN1 or **TGAIN2**	0..1	0..1	0..1	0..3	2	3
[2)] **CORR2**	0	0	0	0	1	0

1) Logical channel T1 always primary bridge sensor linearization temperature. Here NTC not possible.
2) CORR2 enables logarithmic linearization formula according Steinhart/Hart for NTCs and for channel T2 only, otherwise linearization with polynomial 3rd order in T for all other sensor types.

As to be seen in 6.4-1 and in 6.4-1, the sensor inputs TSEN1 and TSEN2 are not identical:
- input pin TSEN1 is preferred suited for external diode sensor (with internal pull-down current)
- input pin TSEN2 is preferred for NTC or PTC sensors (no pull current and special diagnosis features)

Use case with only one T channel

This use case is not recommended for functional safety applications because of missing redundancy for the temperature measurement, with temperature may have significant impact on primary pressure input correction.
If no second channel (T2) is needed it is recommended to select the internal diode for T2. The reason is, that T2 measurement is performed anyway and so no additional TADC input current at pins TSEN1 or TSEN2 is generated. Additionally the temperature voter has to be disabled if only one temperature channel is used, see chapter 6.10.16.

TADC Setting Registers:

The mentioned setting bits for TADC are stored in NVM in the T1_MODE and the T2_MODE register, which are defined in detail in the following tables:

Table 6.4-2: Register **T1_MODE** [NVM] temperature channel mapping and offset selection (in NVM)

	MSB							***LSB***
Content	IDIO_OFF	-	-	-	TCHAN1[1:0]		TGAIN1[1:0]	
Reset value	0	0	0	0	0		0	
Access	R	R	R	R	R		R	
Bit Description	**IDIO_OFF** : 1: switch off diode pull down current at TSEN1 **TCHAN1[1:0]** : selects input for T1 (used for bridge sensor temperature correction) 0 = internal diode 1 = TSEN1 (measured against EXHI) 2 = TSEN2 (measured against VDDA) 3 = sensor current **TGAIN1[1:0]** : selects gain for T1 0 = full scale is V_{VDDA}/3 (from 2..3x V_{VDDA}/3) 1 = full scale is V_{VDDA}/3 (from 2..3x V_{VDDA}/3) 2 = full scale is V_{VDDA} (from 0..V_{VDDA}/1) 3 = full scale is V_{VDDA}/8 (from 0..V_{VDDA}/8)							

Table 6.4-3: Register **T2_MODE** [NVM] temperature channel mapping and offset selection (in NVM)

	MSB							***LSB***
Content	-	-	-	CORR2	TCHAN2[1:0]		TGAIN2[1:0]	
Reset value	0	0	0	0	0		0	
Access	R	R	R	R	R		R	
Bit Description	**CORR2** : selects T2 correction algorithm 0 = normal (polynomial) 1 = NTC (Steinhart-Hart approach) **TCHAN2[1:0]** : selects input for T2 (used for media temperature or redundant sensor temperature) 0 = internal diode (or if T2 is not used) 1 = TSEN1 (measured against EXHI) 2 = TSEN2 (measured against VDDA) 3 = sensor current **TGAIN2[1:0]** : selects gain for T2 0 = full scale is V_{VDDA}/3 (from 2..3x V_{VDDA}/3) 1 = full scale is V_{VDDA}/3 (from 2..3x V_{VDDA}/3) 2 = full scale is V_{VDDA} (from 0..V_{VDDA}/1) 3 = full scale is V_{VDDA}/8 (from 0..V_{VDDA}/8)							

6.5 CORRECT - Digital Sensor Signal Processing

6.5.1 Pressure Sensor Signal Correction

The digital compensation engine shall calculate from the acquired signals of sensor bridge and (bridge) temperature a temperature independent and linearized digital output signal, which is normalized to a given output range and offset free (or with defined offset).

Generally a polynomial up to 2nd order in p and 3rd order in T as follows is implemented:

$$P_{SENT}(p_{ADC}, T_{SENT}) = \sum_{i=0}^{2}\sum_{j=0}^{3} c_{ij} \cdot {p_{ADC}}^{i} \cdot {T_{SENT}}^{j}$$

The coefficients c_{00} ... c_{23} of the correction formula will be determined in the final calibration process of SSP mated to a sensor bridge by measuring the sensor at different pressure and temperature corners and calculating the coefficients from a best fit algorithm. For that task a calibration library is provided.
After calculation of intermediate coefficients Q_x from current sensor temperature (always $T1_{SENT}$) we get a 2nd order pressure linearization formula, which has to be calculated for every pressure channel with different coefficients:

$$P_{SENT}(p_{ADC}) = Q_2(T_{SENT}) \cdot {p_{ADC}}^2 + Q_1(T_{SENT}) \cdot p_{ADC} + Q_0(T_{SENT})$$

where:

p_{ADC} = input signal from the sensor bridge PADC
P_{SENT} = corrected output signal in SENT output format

See 6.5.1-1 for the transfer characteristic for pressure according SENT definition for comparison in pressure voter and later on for transmission in fast or slow channel. The points PX1/2 and PY1/2 are defined during calibration process with support from our calibration library and can be transmitted via SENT slow channel.

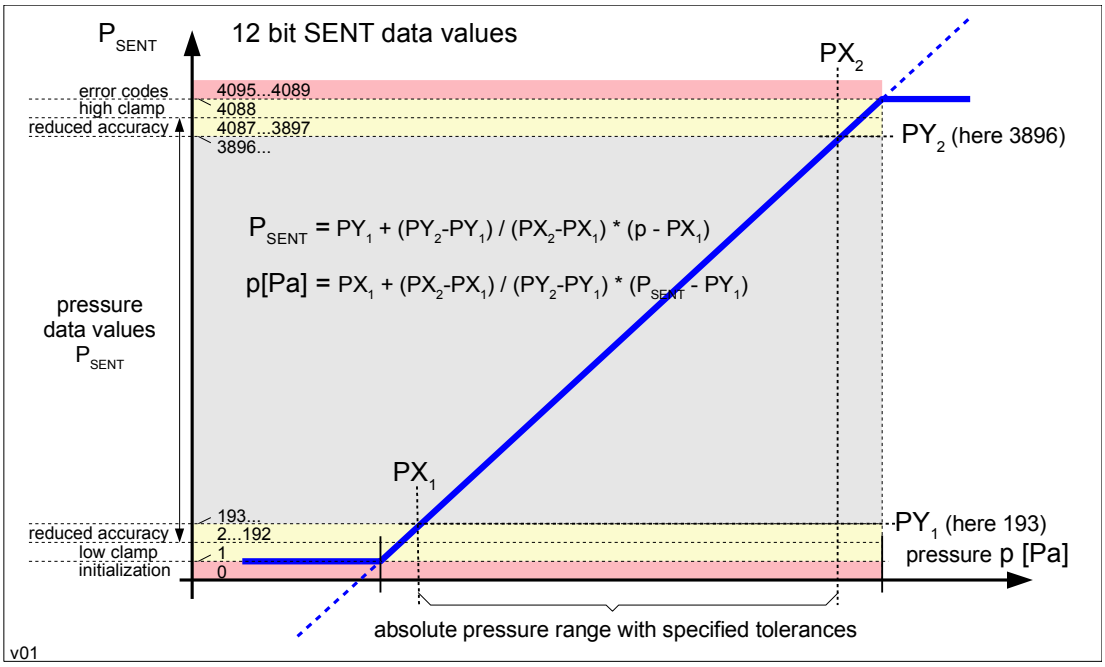


Figure 6.5.1-1: SENT Pressure Characteristic Function

6.5.2 Pressure Sensor Post Correction

There is an easy way in correction algorithm to implement a so called *post correction* of both pressure channels. This allows to correct SENT pressure value characteristic with an additional linear function with individual gain and offset value for each channel.
So potential effects on characteristic by subsequent manufacturing processes like higher level packaging can be corrected.
The correction range is intended small and defined by parameters in NVM block 2 according following table:

Table 6.5.2-1: Post Correction Parameters

Name	*Meaning*	*Correction Effect*
DGAIN1 DGAIN2	delta gain for p1/p2	8 bit value interpreted as two's complement; correction factor formula: GainFactor = 1 + DGAINx[7:0]/8192 Range: 100% +/-1.55%
DOFFS1 DOFFS2	delta offset for p1/p2	8 bit value interpreted as two's complement; correction offset formula: Offset = DOFFSx[7:0] Range: -128...+127 LSB_{SENT} (approx. +/-3.1% FS)

Post correction formula is implemented as follows for each channel P1 and P2:

$$P_{SENT,CORR}(P_{SENT},DGAINx,DOFFSx) = GainFactor(DGAINx) * P_{SENT} + Offset(DOFFSx)$$

The coefficients DGAINx and DOFFSx are set to 0x00 if no correction is necessary or to suited values calculated by a 2nd post calibration process if wanted.

The following figure shows an example, how post correction acts on SENT characteristic.

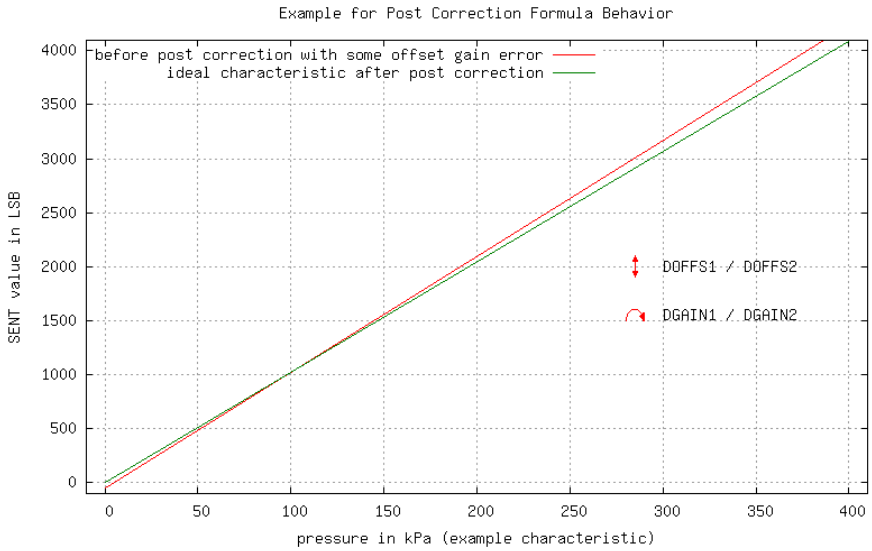


Figure 6.5.2-1: Example for Post Correction Formula Behavior

6.5.3 Sensor Temperature Signal Correction

The above given formula $P_{SENT}(p_{ADC},T_{SENT})$ uses a pre-corrected temperature T_{SENT}, which is the same temperature, which will be used for SENT transmission of sensor temperature.
That is why this temperature T_{SENT} has to be calculated first before parameters c_{xy} for pressure linearization are calculated.

There is a third order trimming formula used for temperature linearization implemented:

$$T_{SENT}(T_{RAW}) = Q_3 \cdot T_{RAW}^3 + Q_2 \cdot T_{RAW}^2 + Q_1 \cdot T_{RAW} + Q_0$$

where model parameters Q_0, Q_1, Q_2 and Q_3 are stored in the corresponding 16 bit NVM registers. There is another auxiliary internal parameter Q_4 used. All parameters are calculated by use of a provided calibration library.

Because of maximum two possible temperature sensors used parallel in the same application, there are two sets of coefficients named T1_Q0...Q4 and T2_Q0...Q4, see 6.8.1-1.

Finally we get following default transfer characteristic for temperature according SENT definition for comparison in temperature voter and later on for transmission in fast or slow channel:

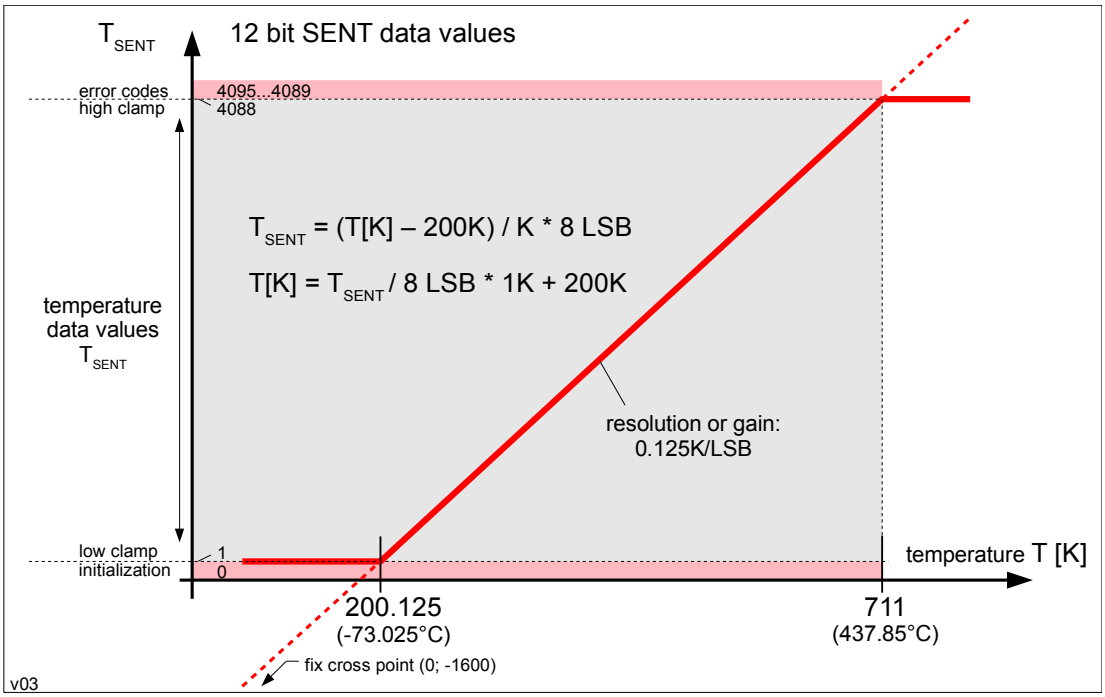


Figure 6.5.3-1: SENT Temperature Default Characteristic Function

6.5.4 NTC Temperature Processing

Beside the normal temperature sensor linearization with 3rd order polynomial as described in chapter 6.5.3, there is another linearization formula implemented especially optimized for external connected resistor dividers with an NTC.
This sensor has to be connected to pin TSEN2 and this formula is selected with bit T2_MODE.**CORR2**=1.

For example the characteristic of a NTC resistor over temperature and the resulting ADC read-out from a resistive divider with NTC and operating point resistor R_{OP} are shown below (6.5.4-1, 6.5.4-2).
Due to the exponential characteristic of $R_{NTC}(T)$, also the output of the divider is strongly non-linear.

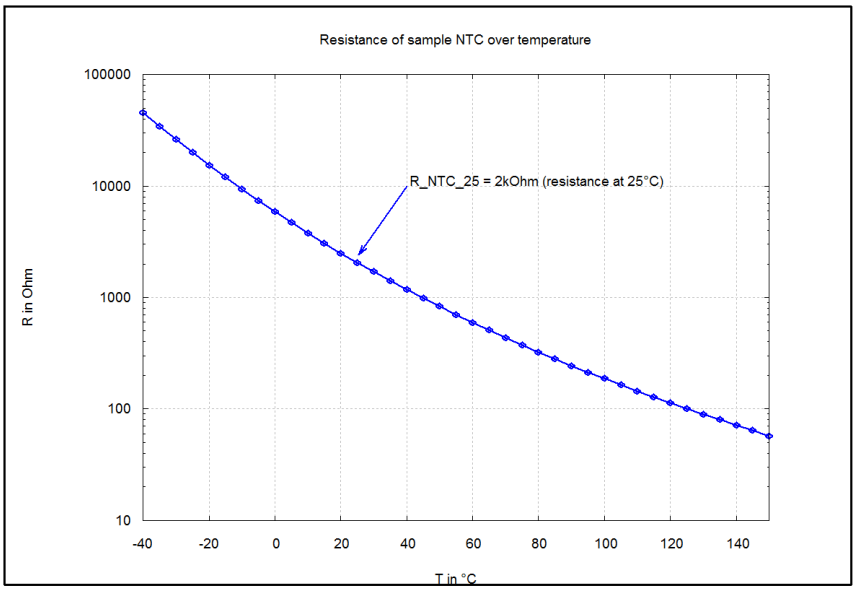


Figure 6.5.4-1: Typical NTC Characteristic vs. Temperature

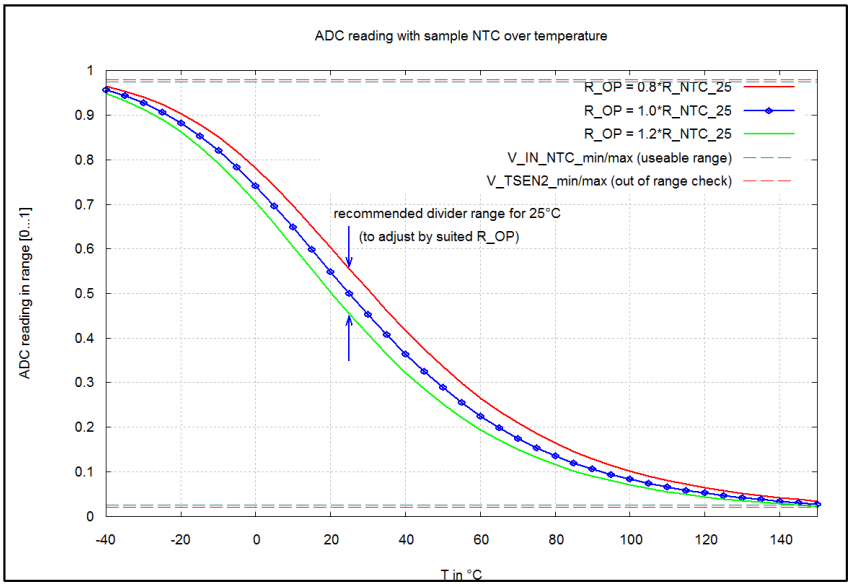


Figure 6.5.4-2: Typical ADC Readout vs. Temperature

In 6.5.4-2 above additional to the characteristic of the resistor divider the usable input range and the limits for the "out of range" check are displayed depicted. Details for this check see chapter 6.10.7.

By using a *Steinhart-Hart* like calculation formula, the ADC read-out according to example above can be converted to a linear characteristic with linearization parameters A, B, C, D stored in NVM cells T2_Q0..3.

It is assumed, that NTC characteristic behaves according following formula:

$$T_{NTC}(R) = \frac{1}{A + B \cdot \ln\left(\frac{R}{R_0}\right) + C \cdot \ln^2\left(\frac{R}{R_0}\right) + D \cdot \ln^3\left(\frac{R}{R_0}\right)} \quad \text{with:} \quad R_0 = R(T_0) \quad \text{and} \quad T_0 = \frac{1}{A}$$

To reach the necessary tolerance, the recommended range of R_{OP} is defined relative to R_{NTC_25} and the possible model parameters A, B, C and D have to fulfill some demands, see 4.4.3-1.

Finally the result after linearization is again in SENT LSBs as already depicted in 6.5.3-1 before.

Tolerance Band

If NTC element behaves like given formula and calibration is done, calculated NTC temperature is within a certain tolerance band. This is defined by parameters $E_{T,NTC}$, $E_{T,NTC,-40C}$ and $E_{T,NTC,125C}$ and with linear behavior between defined temperatures as shown exemplarily in the next diagram (6.5.4-3).

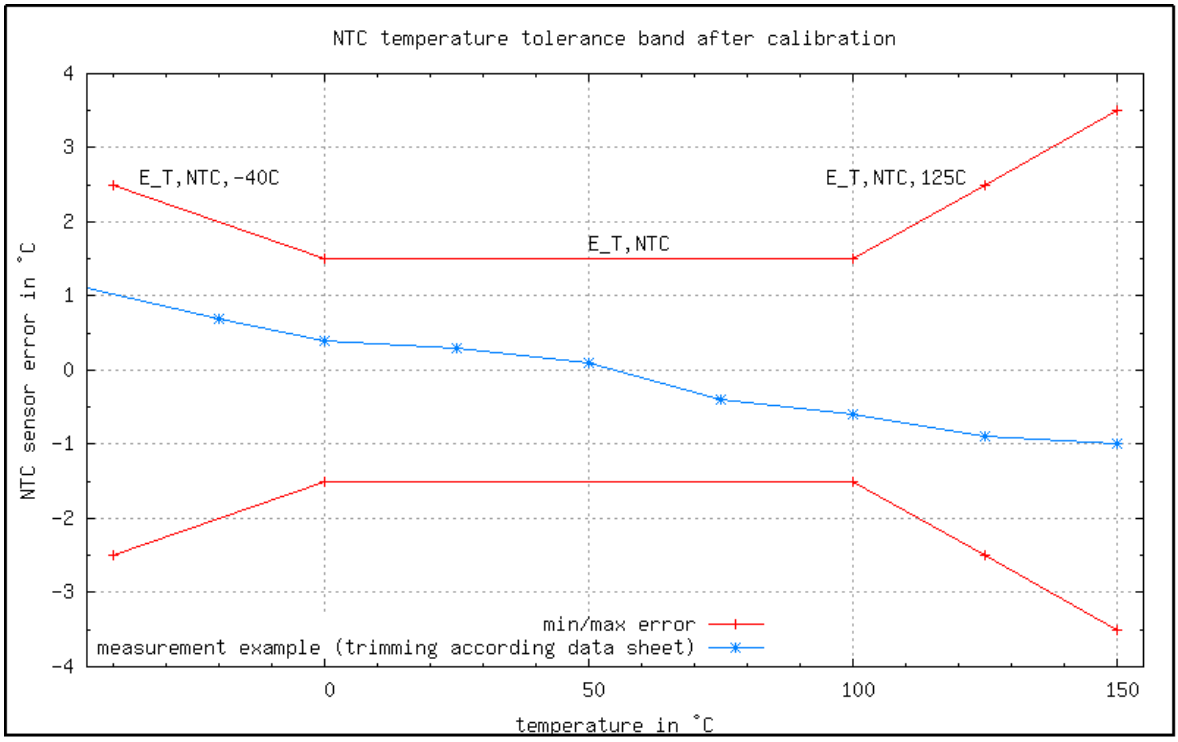


Figure 6.5.4-3: Tolerance Band of Calculated NTC temperature

Note:
The example error curve depicted in 6.5.4-3 above was measured after a trimming just according NTC data sheet. With device individual NTC trimming remaining error band can be even smaller.

6.5.5 Data Flow and Time Scheduling

An overview about data flow and data dependencies and update scheme is shown in the next figure.
The green filled boxes show parameter taken directly from NVM memory and used for individual parametrization of calculation. Yellow boxes contain interim or final result vectors for pressure or temperatures.

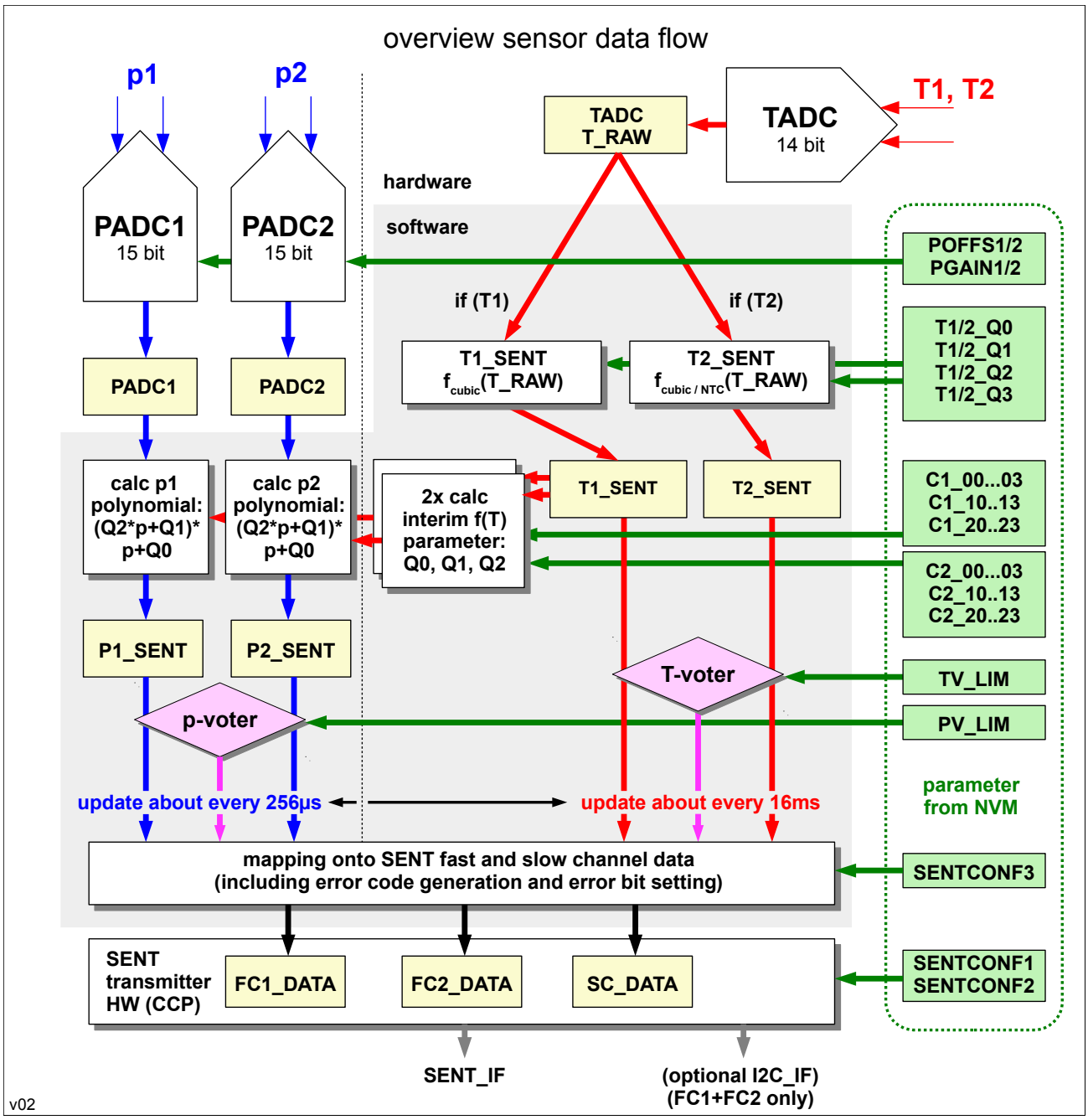


Figure 6.5.5-1: Overview of Sensor Data Flow

6.6 SENT_DIG / SENT_IF - SENT and Programming Interface

The pin OUT is dedicated to realize serial communication with the SSP. It may be used in two different operation modes:

- as a uni-directional SENT output, in Application Mode, or
- as a bi-directional serial-I/O interface (SIO) for calibration and configuration, in Configuration Mode

Both modes are more detailed described in the sub-chapters below.

6.6.1 SENT Mode

SENT (**S**ingle **E**dge **N**ibble **T**ransmission) is a one wire protocol that encodes data nibbles (four bits) by one pulse per nibble. The pulse length is measured between two falling edges and reflects the nibble value. The minimum nibble pulse length is 12 clock ticks (representing the nibble value 0x0) and the maximum nibble pulse length is 27 clock ticks (12 + 15 ticks, representing 0xF). Thereby the nominal width of the low pulse generation is 5 tick times.

The communication is unidirectional: the SSP slave sends pressure signal values autonomously whereas the master acts as a receiver only.

6.6.1.1 SENT Physical Interface

The SENT physical interface is implemented in accordance to SAE 2716 APR2016, with specific type classes as described in the chapters below.
It provides a push-pull output driver on pin OUT to generate the digital output data.
The output is protected against overvoltage and reverse polarity.

The required external circuitry is given in the following picture, with parameter values listed below in 6.6.1.1-1.

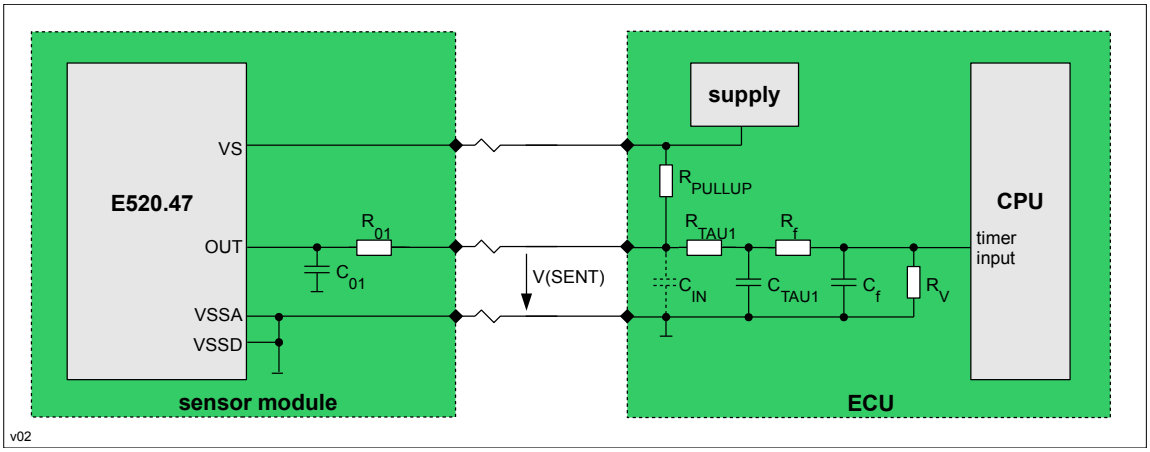


Figure 6.6.1.1-1: External Circuitry for SENT Transmitter and Receiver

Table 6.6.1.1-1: Parameters of passive components on SENT transmitter/receiver, see 6.6.1.1-1

Description	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
SENT receiver pull-up resistor	R_{PULLUP}	9.5	-	55	kΩ
SENT receiver input filter 1 resistor [1)]	R_{TAU1}	448	560	672	Ω
SENT receiver input filter 1 capacitor [1)]	C_{TAU1}	1.54	2.20	2.86	nF
SENT receiver input filter 1 time constant	TAU_1	0.74	-	1.73	µs
SENT receiver parasitic input capacitance [2)]	C_{IN}	-	-	100	pF
SENT receiver input filter 2 time constant [3)]	TAU_2	0.6	-	1.4	µs
SENT receiver EMI filter resistor	R_f	4	-	-	kΩ
SENT transmitter EMI filter resistor	R_{01}	90	100	110	Ω
SENT transmitter EMI filter capacitor	C_{01}	1.54	2.20	2.86	nF

1) Device tolerance must meet overall tolerance target of time constant TAU_1.
2) Maximum parasitic wiring capacitance 500pF.
3) Determined by R_V, R_f and C_f. R_V and R_f creating optional level converter from 5V output to 3.3V receiver input (typical values: R_V = 12kΩ, R_f = 6.8kΩ, C_f = 220pF)

The pulse shape of a typical data pulse on the SENT interconnection wire is shown in the figure below.

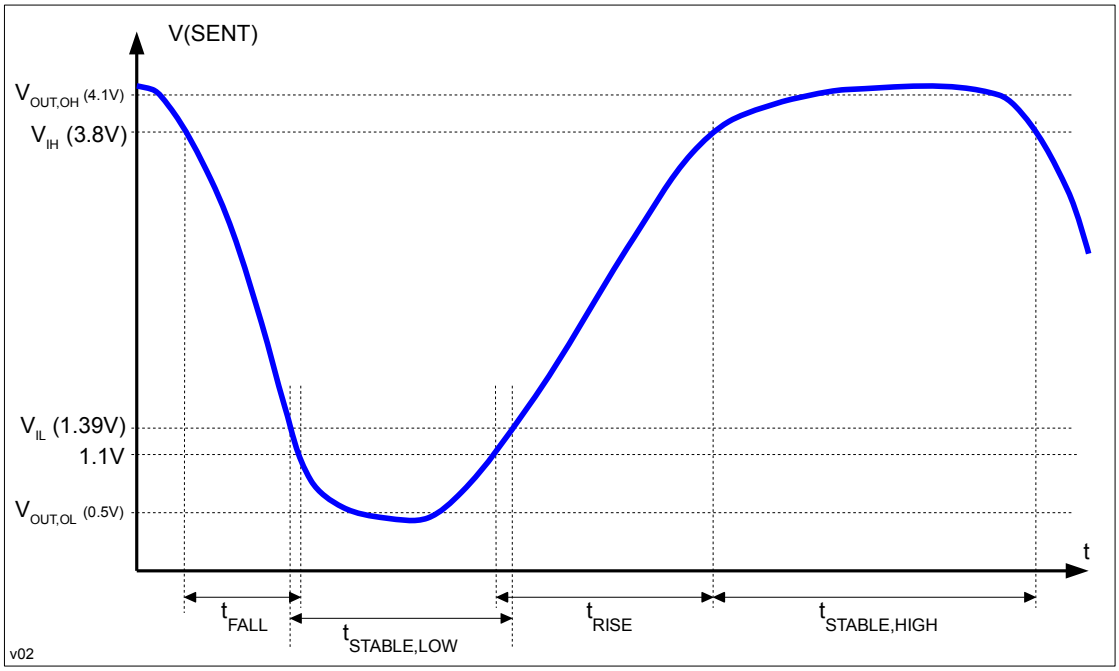


Figure 6.6.1.1-2: SENT Signal at Interconnection Wire

6.6.1.2 SENT Fast Channel Message Format

Each so called SENT *message* consists of six to ten negative pulses on the transmission line without or with pause pulse (**NPP**=1 or 0), respectively. The following picture illustrates one sent message for six data nibbles each coding 4 bits and here without the optional pause pulse.

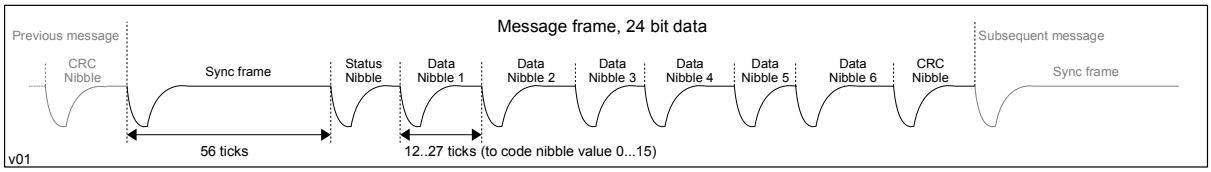


*Figure 6.6.1.2-1: SENT Message without Pause Pulse (bit **NPP**=1)*

The elementary unit of time measurement in the context of the SENT protocol is called a *clock tick* (T_{TICK}). By default this time is 3µs long, but other values can be configured with SENTCONF1.**TICKSEL[4:0]** between nominal 3..31µs in steps of 1µs.

The message starts with the *sync frame* which is always 56 clock ticks long. This pulse is used by the receiver to detect the start of that message and to measure the transmitters clock tick time. Next is the *status nibble*, followed by three, four or six data nibbles and a checksum nibble (CRC). Since the pulse times depend on the transmitted values (except for the sync frame) the length of such a message is not fixed. With the configuration bit **NPP** being cleared, a *pause pulse* can be added after the CRC nibble. The length of that pulse is always adapted to the previously sent data such that a constant message length of minimum 282 clock ticks (for 8 nibble setup) is guaranteed, see the following picture.

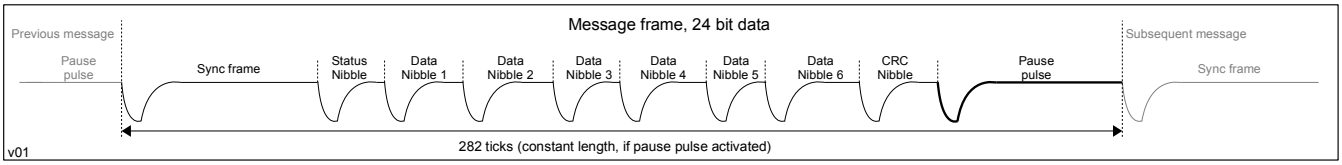


*Figure 6.6.1.2-2: SENT Message with Pause Pulse (bits **NPP**=0 and **PP_LEN[7:0]**=0x5D)*

This overall protocol length with *pause pulse* setting (**NPP**=1) can be programmed between 3..768 * t_{TICK} in steps of 3* t_{TICK} with setting in **PP_LEN[7:0]** in register SENTCONF3. The formula for protocol length is as follows:

$$t_{prot} = (\mathbf{PP\_LEN} + 1) * 3 \text{ ticks}$$

There are different minimum settings necessary for PP_LEN, depending on selected FC_MODE. See Table 6.6.1.2-1 below.

Status Nibble

The status nibble bits contain the following data:

- Bit 0 is set if and only if the transmitted value at fast channel 1 (abbreviated FC1) is 4090 (diagnostic error) or 1 or 4088 (lower and upper clamp values) or 4095 (production state).
- Bit 1 is the same for fast channel 2.
- Bit 2 and 3 contain information for serial data transmission in the *slow channel* (abbreviated SC).

Data Nibble and FC Modes

Data values are always transmitted within 3 nibbles each 4 bit, resulting in 12 data bits. The only exception is the high speed mode H.3 with 4 nibbles each 3 data bits.
Data nibbles 1 to 3 always contain pressure data. The pressure value is sent as a 12-bit unsigned integer number. For the 1st data value **FC1** the most significant nibble MSN is sent first. For the 2nd data value **FC2** normally the least significant nibble LSN is sent first.
The used fast channel values can be selected by bits **FC1_SRC[2:0]** and **FC2_SRC[2:0]** in SENFCONF4 register.

SENT standardizes several application specific protocols of which the SSP provides the following selectable with setting **FC_MODE[2:0]** in SENTCONF1 register:

Table 6.6.1.2-1: Overview about FC Modes

Name	*Ref. in SENT Norm*	*FC_MODE [2:0]*	*FC1: Data Nibbles 1..3*	*FC2: Data Nibbles 4..6*	*PP_LEN_{min}*	*Length in Ticks*
P/-	H.5	1	12 bit data: MSN, MidN, LSN	zero, zero, zero	78 (0x4E)	237
P/S	H.4	2	12 bit data: MSN, MidN, LSN	counter MSN, LSN, inverted copy of MSN	93 (0x5D)	282
P/x 2x MSN 1st	-	1	12 bit data: MSN, MidN, LSN	12 bit data: MSN, MidN, LSN	93 (0x5D)	282
P/x	H.1	3	12 bit data: MSN, MidN, LSN	12 bit data: LSN, MidN, MSN	93 (0x5D)	282
P 3x 4bit	H.2	4	12 bit data: MSN, MidN, LSN	no nibble 4, 5, 6	66 (0x42)	201
P (hs) 4x 3bit	H.3	5	9 bit data: MSN, MidMSN, MidLSN	further 3 bit data: LSN; no nibble 5, 6	65 (0x41)	198

Additional data is provided via **enhanced serial messages**, see below in paragraph **Slow Channel Data**.

Some values are reserved for special purposes, as illustrated in the next table.

Table 6.6.1.2-2: Error Codes in Data Nibbles

signal interpretation	*signal value*	*error bit in status nibble* [2]
sensor still in *production state* [3]	4095	1
unused error codes	4091..4094	-
diagnostic error	4090	1
unused error code	4089	-
high clamp	4088	1
pressure data	2..4087	0
low clamp	1	1
initialization [1]	0	0

1) This code will never be sent because the SENT interface is activated only after the initialization is complete.
2) Status bit 0 is the error bit for the first fast channel, bit 1 for the second fast channel.
3) This state can indicate that configuration and calibration of sensor is not complete. It can be activated by special code for setting parameter **FC1_SRC** and **FC2_SRC**, details see in definition of register SENTCONF4.

CRC Nibble

The CRC nibble contains checksum data. Its generation is defined in the SAE J2716 standard.

SENT Option P/-

This option provides a way to transfer pressure data from the sensor only.
In this case the fast channel contains only the pressure information and further 3 data nibbles are set to zero, which provides shortest length for unused 3 data nibbles 4...6.

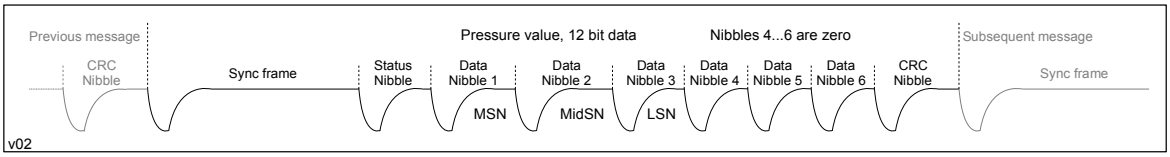


*Figure 6.6.1.2-3: SENT Option P/- (here **NPP**=1)*

SENT Option P/S

In this option pressure is transferred with additional redundancy information in nibbles 4...6:

- Data nibble 4 and 5 contain an 8-bit rolling counter, most significant nibble sent first. This modulo-256 counter is incremented with every message.
- Data nibble 6 is the bitwise inverted data nibble 1.

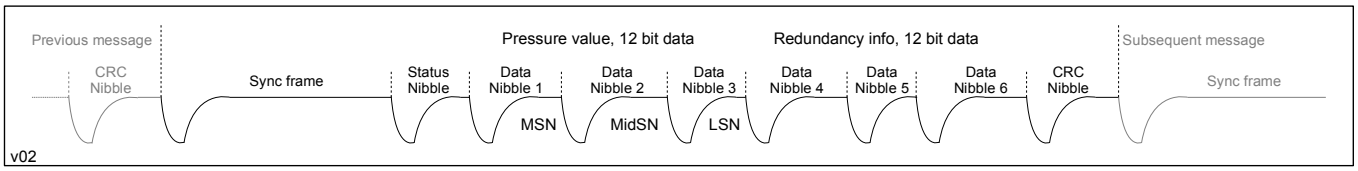


*Figure 6.6.1.2-4: SENT Option P/S (here **NPP**=1)*

SENT Option P/x (P/T or P/P)

This SENT option provides transmission of the pressure value and additionally another pressure value or a temperature value:

- Data Nibble 4 to 6 carries a 2nd pressure value or temperature data, both selected from different sources by **FC2_SRC[2:0]** .
- Via **FC_MODE** is selectable, if 2nd data value is sent LSN first or MSN first, see Table 6.6.1.2-1.

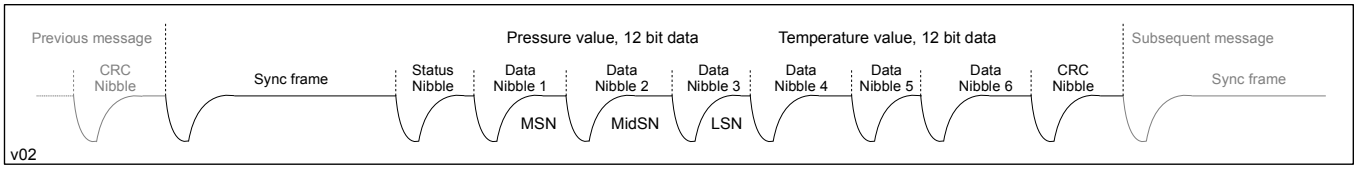


*Figure 6.6.1.2-5: SENT Option P/T (here **NPP**=1, setting P/P similar)*

SENT Option P

This SENT option provides transmission of one pressure value only within a 5 nibble frame:

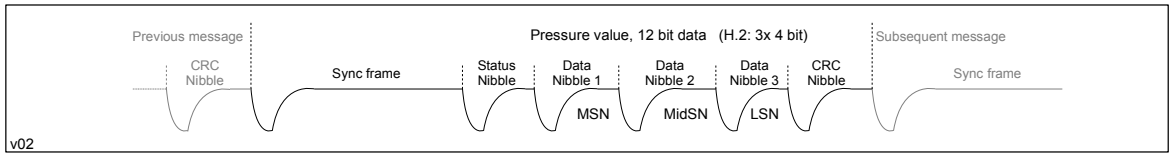


*Figure 6.6.1.2-6: SENT Option P (here **NPP**=1)*

SENT Option P (High Speed, 4x 3 Bit)

This SENT option provides transmission of one pressure value only within a 6 nibble frame, where the 12 bit data is coded in four 3-bit-nibbles as follows:

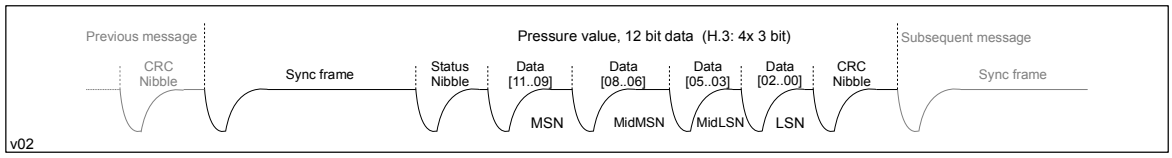


*Figure 6.6.1.2-7: SENT Option P (here **NPP**=1)*

Temperature Data Mapping

Temperature data on SENT is always between 1 and 4088. A value of 0 appears during initialization, values of 4089 and above are reserved for error codes.
For the default temperature characteristic see also 6.5.3-1.

The temperature sent by SENT is calculated from the absolute temperature by

$$T_{SENT} = 8 \cdot (T_{ABS}[K] - 200)$$

The absolute temperature can be calculated from the SENT data by

$$T_{ABS}[K] = \frac{T_{SENT}}{8} + 200$$

T_{ABS} is an unsigned 12-bit fixed point number with the binary point between bit 2 and bit 3. The lowest temperature (T_{SENT} = 1) corresponds to 200.125 K (-73.0 °C), the highest temperature (T_{SENT} = 4088) is 711 K (437.9 °C).

The specific temperature characteristic T_{SENT}=f(T_{ABS}) is determined during calibration. So it is possible to calibrate other temperature characteristics too by change of calibration setting, although it is not recommended to leave SENT standard characteristic.

6.6.1.3 Slow Channel Data

The bits 2 and 3 in the status nibble of each fast channel message embed data for the so called *serial data transmission*. Depending on bit **SC_MODE** 16 (short serial message format) or 18 (enhanced message format) of these bit pairs that are transmitted in consecutive messages result in one *serial message*. This is called the *slow channel* (SC). For configuration details see register SENTCONF2.

The format of enhanced serial messages (with 8-bit ID) and a short serial Message are shown in the following pictures:

SENT message number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
status nibble bit 3	1	1	1	1	1	1	0	C	ID[7:4]				0	ID[3:0]				0
status nibble bit 2	CRC6[5:0]						DATA[11:0]											

*Figure 6.6.1.3-1: Embedding One **Enhanced Serial Message** in 18 Consecutive Fast Channel Messages*

SENT message number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
status nibble bit 3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
status nibble bit 2	Message ID[3:0]				DATA[7:0]								CRC[3:0]			

*Figure 6.6.1.3-2: Embedding One **Short Serial Message** in 16 Consecutive Fast Channel Messages*

An enhanced slow channel message carries 8 bits ID and 12 bits data information. Additionally a 6 bit CRC checksum allows integrity checking. A subset of all possible IDs is sent in a repetitive manner.

Note:
The configuration bit C in 6.6.1.3-1 is determined by SENTCONF2.**SC_CONF**. Normally this bit is 0. Setting this bit to 1 would indicate that the receiver should interpret only ID[7:4] as ID and the bits ID[3:0] as additional data bits DATA[15:12]. In this special case the ID would have only 4 bits and the DATA would have 16 bits.

Slow Channel Sequence

There is a free programmable sequence of slow channel messages, which will be transmitted cyclically.
All data values have 12 bit length. The different available data types are listed in the table below.

Table 6.6.1.3-1: Slow Channel Message IDs

ID[7:0] [3]	*ID Recommended*	*Content Type*	*DATA[11:0] description*	*Comment / Name*
0x01	(fix)	dynamic data	diagnostic error code	DEC, see Table 6.6.1.4-1
any	0x1C	sensor data	pressure value $P1_{SENT}$	
any	0x1D	sensor data	pressure value $P2_{SENT}$	
any	0x23	sensor data	pressure value $T1_{SENT}$	
any	0x24	sensor data	pressure value $T2_{SENT}$	
any	0x29	ID data	sensor ID #1	SID1 [2], byte ID3 of unique chip ID
any	0x2A	ID data	sensor ID #2	SID2 [2], byte ID2 of unique chip ID
any	0x2B	ID data	sensor ID #3	SID3 [2], byte ID1 of unique chip ID
any	0x2C	ID data	sensor ID #4	SID4 [2], byte ID0 of unique chip ID
any	0x90	fix data [1]	OEM part number #1	OEM1
any	0x91	fix data [1]	OEM part number #2	OEM2
any	0x92	fix data [1]	OEM part number #3	OEM3
any	0x93	fix data [1]	OEM part number #4	OEM4
any	0x94	fix data [1]	OEM part number #5	OEM5
any	0x95	fix data [1]	OEM part number #6	OEM6
any	0x96	fix data [1]	OEM part number #7	OEM7
any	0x97	fix data [1]	OEM part number #8	OEM8
any	any	fix data	any	any
			examples for fix data:	
any	0x03	fix data	sensor type	S_TYPE
any	0x04	fix data	configuration code	CCODE
any	0x05	fix data	manufacturer code	MCODE
any	0x06	fix data	SENT standard revision	SENT_REV
any	0x07	fix data	pressure characteristic X1	PX1
any	0x08	fix data	pressure characteristic X2	PX2
any	0x09	fix data	pressure characteristic Y1	PY1
any	0x0A	fix data	pressure characteristic Y2	PY2
any	0x80	fix data	for manufacturer use #1	MFU1
any	0x81	fix data	for manufacturer use #2	MFU2
any	0x82	fix data	for manufacturer use #3	MFU3

1) pointer to fix data in OEM NVM block
2) 8 bit data (plus zero nibble) read from special part of NVM, mapping see Figure -
3) ID codes except 0x01 for DIAG_ERR_CODE (DEC) are configured in NVM using configuration software.

Following figure shows an example SC sequence defined in EEPROM-NVM. Here cycle length is 28 messages.
For this example a complete loop takes 28*18=504 single protocols.

No	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
MID	01	03	04	05	06	07	08	01	80	23	09	0A	29	81	01	2A	2B	2C	82	90	91	01	92	93	94	95	96	97

Figure 6.6.1.3-3: Example for Slow Channel Message Cycle

Elmos provides a configuration software, which supports the individual programming of necessary SC sequence in a very easy way. An example setup is shown in the following figure.

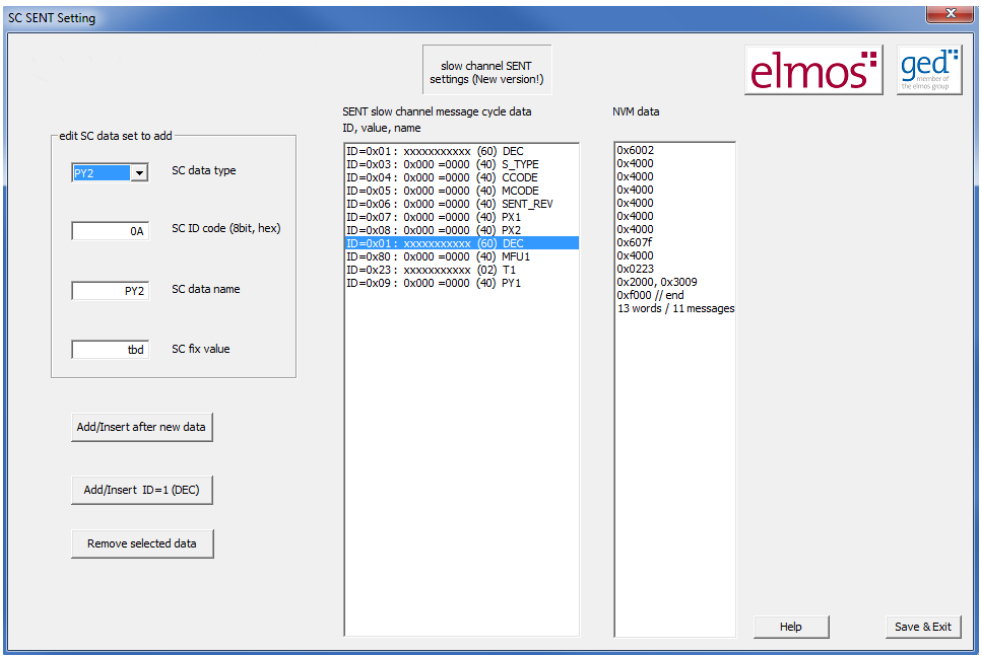


Figure 6.6.1.3-4: Example Setup for SC Sequence Configuration

Sensor ID

There is a product unique chip ID, which is transmitted via slow channel messages SID1..4.

6.6.1.4 Error Handling in SENT Interface

Diagnostic error codes are sent with slow channel ID 0x01.

The following table lists the **diagnostic error codes** in descending order of priority (which matters if two different error codes would occur at the same time).

Table 6.6.1.4-1: Diagnostic Error Codes (DEC)

DEC	*definition*	*fast channel code*	*details (see chapter 6.10)*
0x020	undervoltage detected	T1=T2=p1=p2=4090	supply undervoltage at pin VS (if V5L_ERR is set)
0x021	overvoltage detected	T1=T2=p1=p2=4090	supply overvoltage at pin VS (if V5H_ERR is set)
0x92y	environment BIST error	T1=p1=p2=4090 T1=p1=p2=4090	if any BIST error bit set in ERRC4[7:6] nibble y is defined as: bit 2 : VSM_ERR (VS monitor check error) bit 3 : OT_ERR (chip overtemperature error)
0x93y	numerical calculation BIST error	p1=4090 p2=4090 T1=p1=p2=4090 p1=p2=4090	if any BIST error bit set in ERRC4[3:0] nibble y is defined as: bit 0 : PC1_ERR (p_1 calculation failed) bit 1 : PC2_ERR (p_2 calculation failed) bit 2 : TC1_ERR (T_1 calculation failed) bit 3 : S1_ERR (bridge supply short)
0x94y	pressure sensor BIST error	p1=4090 p1=4090 p1=4090 p1=4090	if any BIST error bit set in ERRC2[3:0] nibble y is defined as: bit 0 : S01_ERR (bridge 1 supply open) bit 1 : S21_ERR (bridge 1 short to supply) bit 2 : S31_ERR (bridge 1 input open) bit 3 : S41_ERR (bridge 1 inputs short)
0x95y	pressure sensor BIST error	p2=4090 p2=4090 p2=4090 p2=4090	if any BIST error bit set in ERRC2[7:4] nibble y is defined as: bit 0 : S02_ERR (bridge 2 supply open) bit 1 : S22_ERR (bridge 2 short to supply) bit 2 : S32_ERR (bridge 2 input open) bit 3 : S42_ERR (bridge 2 inputs short)
0x96y	sensor path BIST error	p1=4090 p2=4090 T1=p1=p2=4090	if any BIST error bit set in ERRC1[3:0] nibble y is defined as: bit 0 : PSP1_ERR (p_1 sensor path error) bit 1 : PSP2_ERR (p_2 sensor path error) bit 2 : TSP_ERR (T_1 sensor path error)
0x97y	temperature sensor BIST error	1) T1=p1=p2=4090 T2=4090 T_{TSEN2}=4090	if any BIST error bit set in ERRC3[7:4] nibble y is defined as: bit 0 : RT1_ERR (range error at T_1; short or open ...) bit 1 : RT2_ERR (range error at T_2; short or open ...) bit 2 : NOP_ERR (NTC/PTC/... at TSEN2 open)
0x98y	saturation error	2) p1=1/4088 p2=1/4088 T1=1/4088, p=4090 T2=1/4088	if any BIST error bit set in ERRC3[3:0] nibble y is defined as: bit 0 : P1_SAT (p_1 over- or underflow) bit 1 : P2_SAT (p_2 over- or underflow) bit 2 : T1_SAT (T_1 over- or underflow) bit 3 : T2_SAT (T_2 over- or underflow)

DEC	*definition*	*fast channel code*	*details (see chapter 6.10)*
0x99y	voter error	T1=p1=p2=4090 p1=p2=4090	if any BIST error bit set in ERRC1[7:6] nibble y is defined as: bit 2 : TV_ERR (T_1 does not match T_2) bit 3 : PV_ERR (p_1 does not match p_2)
0x001	FC_1 data out of range (max) or invalid	FC_1=4088 FC_1=4090	if saturation occurred (overflow) if no valid value is known
0x002	FC_1 data out of range (min)	FC_1=1	if saturation occurred (underflow)
0x004	FC_2 data out of range (max) or invalid	FC_2=4088 FC_2=4090	if saturation occurred (overflow) if no valid value is known
0x005	FC_2 data out of range (min)	FC_2=1	if saturation occurred (underflow)
0x000	no error		

1) T_{TSEN2} means temperature channel mapped to pin TSEN2, which could be T1 or T2.
If T_{TSEN2}=T1 this error T1=4090 causes p1=p2=4090 too.
2) 1 means underflow, 4088 means overflow

Depending on the configuration, the SSP will perform several power-on self tests after power-up. During this test no SENT messages will be transmitted.

If slow channel data with the message ID 0x01 is to be sent and an enabled diagnosis error occurs, the SSP will transmit the fast channel error value 4090 with the status nibble bit 0 and/or bit 1 set to 1, depending on which fast channel shows an error code.
The diagnostic error code in the slow channel contains information about the error source. If no enabled error is present the diagnostic error code will be 0x000.

6.6.1.4-1 below depicts the flow chart for SENT diagnosis error code calculation according the defined priority for different error types.

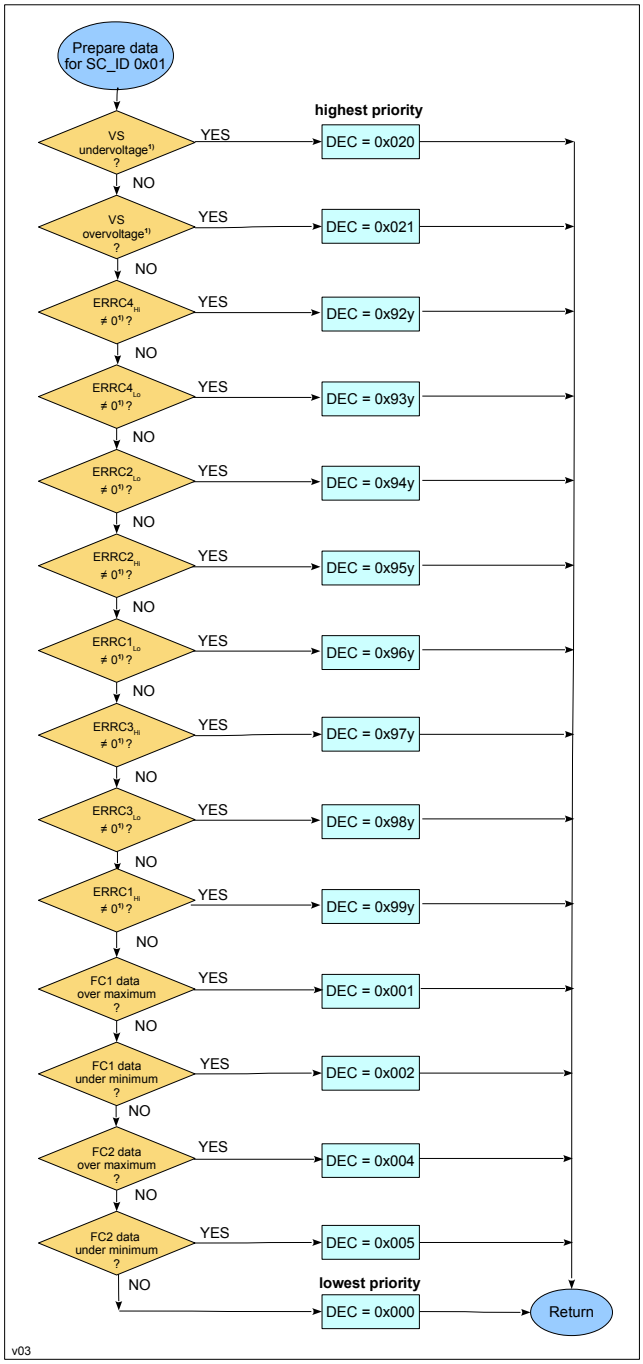


Figure 6.6.1.4-1: Error Flowchart

1) only if appropriate enable bit is set

Calculation of the slow channel CRC happens at the end of the last fast channel message (MSGN=18).

The error bits in the status nibble are set by software (FC2_DATA_H.**STAT**). The secure nibble for P/S mode is calculated by software too and written into FC1_DATA_H.**SEC**.

The SENT protocol engine generates the fast channel CRC checksum as well as the slow channel CRC checksum.

SENT Watchdog

There is an SENT watchdog implemented to avoid sending of outdated data, if DPU does not write SENT registers anymore.
Details see special chapter 6.10.19.

6.6.2 SIO Mode (Serial Input Output)

The serial input/output interface (SIO) is provided in order to simplify calibration and configuration.
It supports bidirectional serial communication through the OUT pin.
To achieve true single-wire operation the SIO interface shares its pin with the SENT output.
When the IC is receiving data in SIO mode, the SENT driver is switched to high impedance state (high-Z).
The SIO interface works as a slave only. This means, it never will initiate communication.

The SIO data transmission uses the Manchester Code (Bi-Phase-L, falling edge is a logical 1) with a typical baud rate of BR_{SIO}.

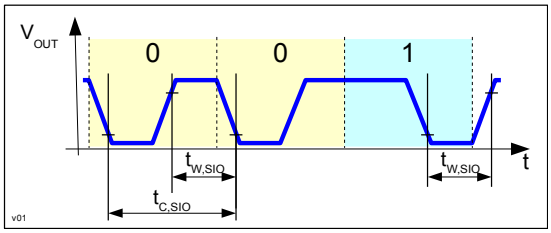


Figure 6.6.2-1: SIO Bit Timing Diagram

The following 6.6.2-2 shows a SIO protocol example during ***configuration mode*** . Two commands are transmitted by the bus master. The first command is a WRITE_NVM command that writes a 16 bit value into the user NVM. The second command GET_P is used to retrieve pressure measurement data.

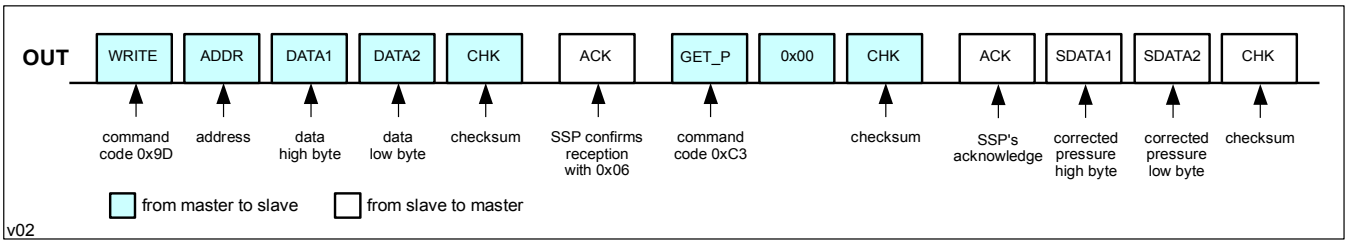


Figure 6.6.2-2: SIO Communication Protocol Example

Data is transferred byte wise. Each byte is preceded by a start bit which is always '1'. Each Manchester coded bit includes either a falling edge (**1**) or a rising edge (**0**) in the middle of a bit cycle time interval $t_{C,SIO}$.

To ensure proper decoding of the received data the bus level should be driven low after the last bit of a byte for at least one bit time $t_{C,SIO}$. After the start bit the MSB is transferred first (see 6.6.2-3). The first rising edge indicates the start of the byte transmission.
Note: If the LSB is a 0, the SIO line must be driven to 0V actively.

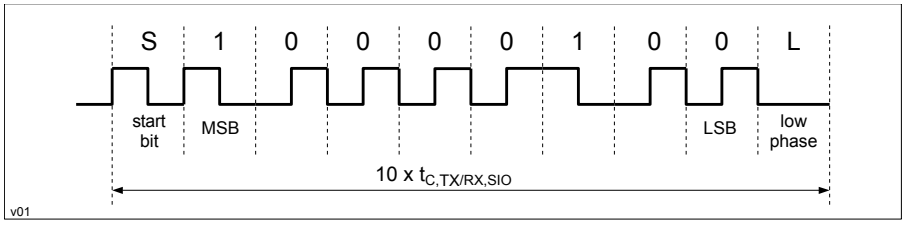


Figure 6.6.2-3: Manchester Coded Byte (example: command ENACONF 0x84)

6.6.3 SENT_IF Registers

There are some SENT configuration registers existing twice in non-volatile memory (NVM) and in special function registers (SFR). The NVM data can be programmed in configuration mode via SIO interface. After power-on the content is copied to the corresponding SFR registers to enable the intended settings.

Table 6.6.3-1: Register **SENTCONF1** SFR and NVM (0x7C) SENT configuration register (copied from **NVM**)

	MSB							***LSB***
Content	FC_MODE[2:0]			TICKSEL[4:0]				
Reset value	0			0				
Access	R/W			R/W				
Bit Description	**FC_MODE[2:0]** : fast channel mode (details see overview Table 6.6.1.2-1) 000_b = SENT disabled 001_b = send FC2_DATA or zeros in second channel with MSN first 010_b = send secure information (for mode P/S) 011_b = send FC2_DATA in second channel with LSN first 100_b = send FC1 only, in three 4-bit data nibbles 101_b = send FC1 only, in four 3-bit data nibbles **TICKSEL[4:0]** : SENT clock tick selection in units of $t_{TICK,LSB}$ (possible range 1 .. 31 µs) value 0 gives 3µs value 1 or 2 give 1µs or 2µs (not recommended; problems with SC sequence possible)							

Table 6.6.3-2: Register **SENTCONF2** SFR and NVM (0x7D) SENT configuration register (copied from **NVM**)

	MSB							***LSB***
Content	SC_MODE	SC_CONF	NPP	-	-	-	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**SC_MODE** : slow channel mode 0_b = enhanced 1_b = short **SC_CONF** : slow channel configuration bit C (sent in status/communication nibble, bit 3, see Figure 6.6.1.3-1) If this bit is set, the upper 4 bits of register SC_ID are the ID (4 bits only) and the lower 4 bits of SC_ID are the 4 upper bits of the data (16 bits). **Note:** • This has no influence on the SENT transmitter hardware. This only is a matter of interpretation of the data. • The configuration bit only appears in enhanced mode. **NPP** : No SENT **P**ause **P**ulse 0_b: pause pulse (length defined by **PP_LEN** setting) 1_b: no pause pulse							

Table 6.6.3-3: Register **SENTCONF3** SFR and NVM (0x7E) SENT PP_LEN definition(copied from **NVM**)

	MSB							***LSB***
Content	PP_LEN[7:0]							
Reset value	00000000							
Access	R							
Bit Description	**PP_LEN[7:0]** : SENT pause pulse length definition: • according binary value with 3 t_{TICK} per LSB • protocol length with pause pulse is: (PP_LEN+1) * 3 ticks • so range up to 768 ticks is covered • there is a minimum PP_LEN value depending on selected FC_MODE necessary, if minimum is violated here the value will be increased to necessary minimum ==> for both see Table 6.6.1.2-1							

Table 6.6.3-4: Register **SENTCONF4** NVM SENT fast channel data selection (in **NVM**)

	MSB							***LSB***
Content			FC2_SRC[2:0]			FC1_SRC[2:0]		
Reset value	0	0	000			000		
Access	R	R	R			R		
Bit Description	**FC2_SRC[2:0]** : selects data for fast channel 2 0 = always 0 (for mode P/-) 1 = temperature T1 2 = temperature T2 3 = pressure P2 4..6 = (reserved) 7 = IC in production state ==> FC2=4095 **FC1_SRC[2:0]** : selects data for fast channel 1 0 = reserved 1 = pressure P1 2 = pressure P2 3 = pressure difference P1 - P2 4..6 = (reserved) 7 = IC in production state ==> FC1=4095							

6.7 CONTROL - Digital Control, I2C Interface and Test Mode Logic

6.7.1 Inter IC Interface (I2C)

The I2C bus interface provides access to the internal command processor for configuration and calibration purposes, and to access measurement results (raw data as well as processed data). The I2C interface may not be used simultaneously with the SIO interface. When data is transferred via the I2C interface, no SIO activity is allowed and vice versa.
To use the I2C interface the bit **I2C_ENA** in register I2C_CONF has to be set to 1. If this bit is 0, then no I2C operation is possible. In this case the pins SCL and SDA may be used as general purpose input/outputs (GPIO).

The interface is I2C standard mode compatible. It does not utilize clock stretching mechanism.

The I2C bus interface works as a slave only, this means it never initiates communication.

For the command format reference refer to the Common Command Processor description.
For I2C bus functionality and protocol during normal operation refer to the related description of the Common Command Processor.

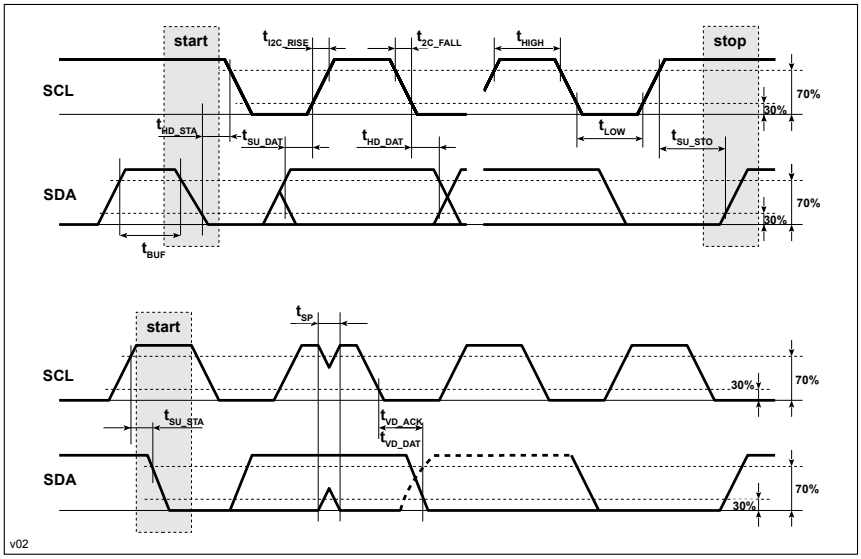


Figure 6.7.1-1: I2C Timing Diagram

I2C Byte Format

The next figure depicts the I2C byte format:

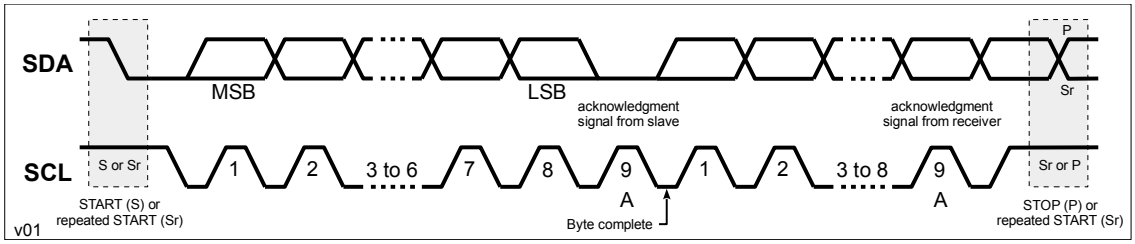


Figure 6.7.1-2: I2C Byte Format

I2C: NVM Coded Secondary Address

The I2C interface responds to 1 out of 4 addresses selected by the bits **I2C_ADR[1:0]** in register I2C_CTRL.

Table 6.7.1-1: I2C : NVM Coded Address Selection

I2C_ADR1	*I2C_ADR0*	*Address (Hex)*
0	0	0x50
0	1	0x51
1	0	0x52
1	1	0x53

I2C Communication Protocol Example

Subsequent 6.7.1-3 depicts an I2C communication protocol example where the bus master issues the WRITE_NVM command.

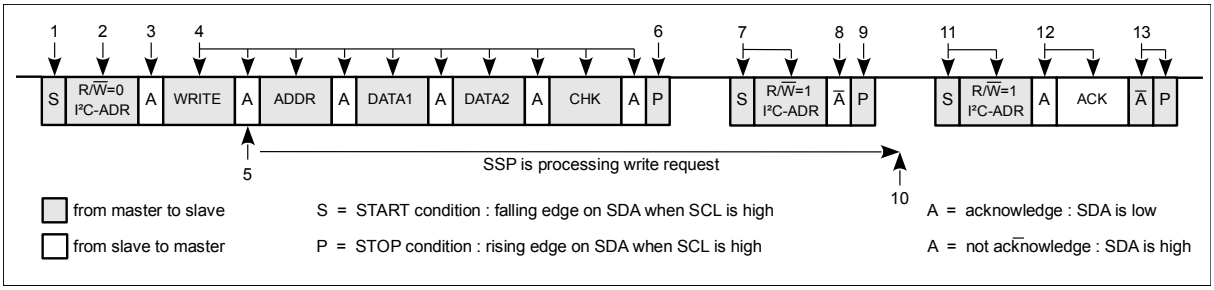


Figure 6.7.1-3: I2C Protocol Example for Command WRITE

1. The bus master applies the I2C start condition (negative edge on SDA while SCL is high).
2. The bus master addresses the SSP for writing by sending a valid slave address with the R/W bit being cleared.
3. The SSP slave acknowledges reception of that address by dominantly pulling SDA low. The SSP is ready for reception of the command byte.
4. The bus master transfers five bytes: the command byte 0x9D (WRITE_NVM), the address of the NVM cell, the value to write into that cell (two bytes) and the checksum. Each byte is acknowledged by the SSP.
5. The SSP starts processing the WRITE_NVM command.
6. The master closes the message frame by applying the I2C stop condition (positive edge on SDA while SCL is high).
7. The bus master polls the SSP by addressing it for read access. This involves sending the start condition followed by a byte that contains the slave address with the R/W bit being set.
8. Since the SSP did not finish processing the WRITE_NVM command yet, it responds by not acknowledging the read request (SDA is kept high).
9. The bus master closes the unacknowledged frame by applying the stop condition.
10. The SSP finished processing the WRITE_NVM command. Hence, following I2C frames will be acknowledged from now on.
11. The bus master's second attempt to read out the pressure value.
12. The slave responds by acknowledging (SDA pulled down) the read request and sending the answer which is just the ACK byte (0x06).
13. Finally the master closes the I2C frame by not acknowledging the received byte (SDA is kept high) and applying the stop condition.

Anyhow, since the maximum processing time for each command is given, polling is not necessary.

Another example shows the protocol for the command READ_NVM:

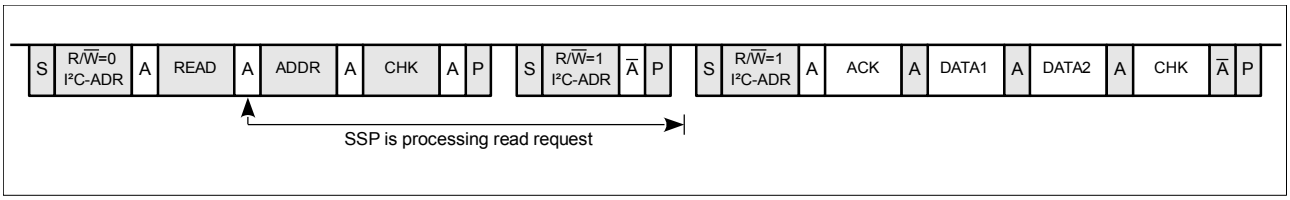


Figure 6.7.1-4: I2C Protocol Example for Command READ_NVM

I2C Readout without a Preceding Command

It is also possible to read out the corrected pressure and temperature signals via the I2C interface without having sent a command before. This mode is called "commandless answer".

The SSP is addressed with a read frame (R/W is high). The data that is sent by the SSP resembles the SENT fast channel data. The upper four bits are always zero.

Which data words will be sent, depends on the SENT fast channel settings (**FC1_SRC** and **FC2_SRC** in SENT-CONF4).

The bit **I2C_MODE** in register **I2C_CTRL** determines if one or two data words are sent.

0 = only FC1_DATA is sent
1 = FC1_DATA and FC2_DATA are sent

A commandless answer starts with a CLA_ACK (0x0E, commandless answer acknowledge).

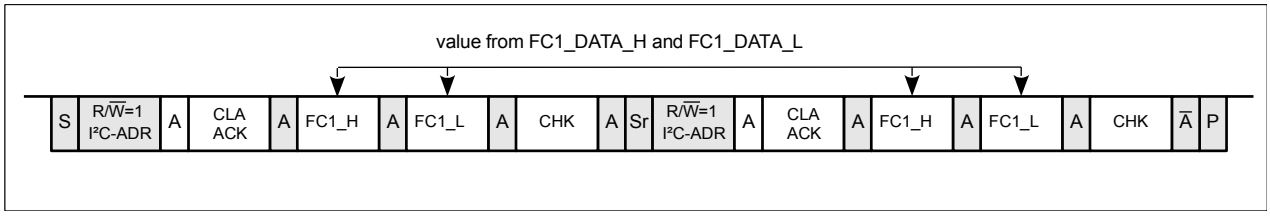


Figure 6.7.1-5: I2C Commandless Answer : Data from FC1_DATA only

If any enabled error is present the commandless answer starts with a CLA_BEL (0x0F) instead of a CLA_ACK (0x0E), refer to second answer in 6.7.1-6.

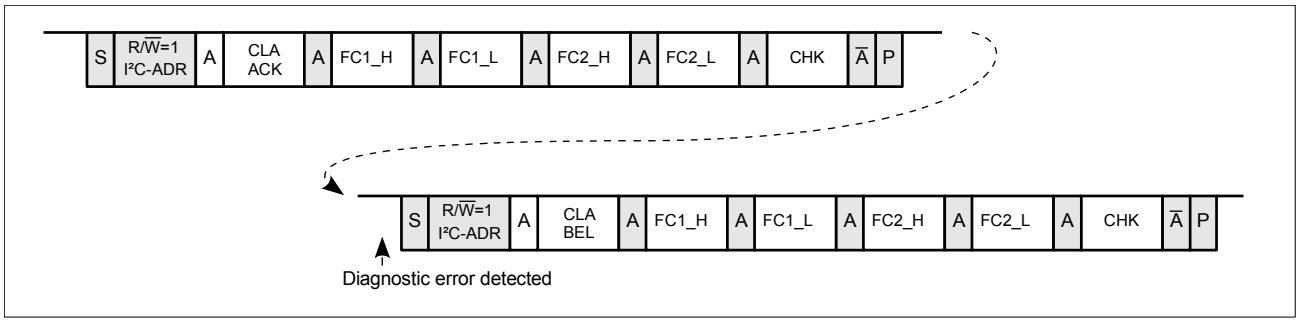


Figure 6.7.1-6: I2C Commandless Answer : Data from FC1_DATA and FC2_DATA

The following control register stores I2C setting information.

Table 6.7.1-2: Register **I2C_CTRL** SFR and NVM (0x77) control bits for I2C interface (some bits copied from **NVM**)

	MSB						***LSB***
Content	-	SCL_OUT	SDA_OUT	CCP_LCK	I2C_ADR[1:0]	I2C_ENA	I2C_MODE
Reset value	0	1	1	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**SCL_OUT** : controls SCL logic level, if **I2C_ENA**=0 0: SCL pin pulled to Low 1: SCL pin high-impedance **SDA_OUT** : controls SDA logic level, if **I2C_ENA**=0 0: SDA pin pulled to Low 1: SDA pin high-impedance **CCP_LCK** : prevents CCP from interpreting commands, especially useful for I2C CLA mode. 0: CCP ready to interpret commands on I2C/SIO 1: CCP not interpreting commands on I2C/SIO note: this bit value is independent from content of corresponding NVM register and controlled by program code only **I2C_ADR[1:0**] : selection of lower two bits [1:0] of I2C address: 0: addr. 0x50 1: addr. 0x51 2: addr. 0x52 3: addr. 0x53 **I2C_ENA** : enables I2C interface: 0: I2C pins (SCL, SDA) used as GPIO pins 1: I2C interface enabled **I2C_MODE** : select if 1 or 2 data words are sent in commandless answer: 0: only FC1_DATA is sent 1: FC1_DATA and FC2_DATA are sent						

6.7.2 Common Command Processor (CCP)

Besides the SENT output on pin OUT the device provides access to calibration and configuration functions. Thus this device provides an I2C bus interface and a Serial Input/Output (SIO) which realizes a one wire interface function by pin sharing with the SENT output.

A Common Command Processor (CCP) processes incoming commands and responds respectively, independent on where the command came from. Thus a flexible configuration using different types of user interfaces for a maximum of convenience and flexibility is possible.

In any case the device behaves as slave, in particular it will never initiate a communication.

Not all commands are applicable in all operation modes.

6.7.2.1 Common Command Processor Modes

After power-on the reset delay elapses first.

Then the SSP enters ***time window mode*** and a time window opens for the duration t_{Window}.
This time window is used to restrict the entrance into the ***configuration mode*** and the ***diagnostic mode***.
The time window is active only once per power-on.

During the time window after power-on the SENT output is in high impedance.

- If the command **ENACONF** or **ENADIAG** does not arrive within the time window the SSP goes into the ***operational mode*** , the SENT output becomes active and the SIO is disabled. Digital communication is then restricted to the I2C interface.
- If the command **ENACONF** or **ENADIAG** arrives via SIO or I2C within the time window the ***configuration mode*** or ***diagnostic mode*** is entered.

Only by applying reset the IC will leave this modes and can be put back to ***operational mode***.

6.7.2.2 CCP Command Format

The bus master initiates communication by sending a command to the SSP. A command is a sequence of two to five bytes. The first byte in this sequence is the command code, the last byte is the checksum. The bytes in between are parameters of the command. The checksum is the sum of all preceding bytes plus one modulo 256.

After command reception, the SSP requires some processing time to generate an answer. This processing time causes a delay that depends on the command code.

In case of SIO communication, the answer will be sent autonomously by the SSP when the delay has elapsed.

In case of I2C communication the SSP cannot send data autonomously. Therefore the bus master can either:

- wait, until the delay has elapsed and then get the answer, or
- poll the SSP.

When the delay has elapsed, the answer can be retrieved by the bus master. In the I2C case this happens via an I2C read access.

When the bus master in case of I2C communication tries to retrieve data from the SSP before the answer has been generated, the SSP will not acknowledge any received byte. In particular the I2C address byte will not be acknowledged.

SIO Communication Protocol Example

The following 6.7.2.2-1 shows a SIO protocol example during ***configuration mode*** . Two commands are transmitted by the bus master. The first command is a WRITE_NVM command that writes a 16 bit value into the user NVM. The second command GET_P is used to retrieve pressure measurement data.

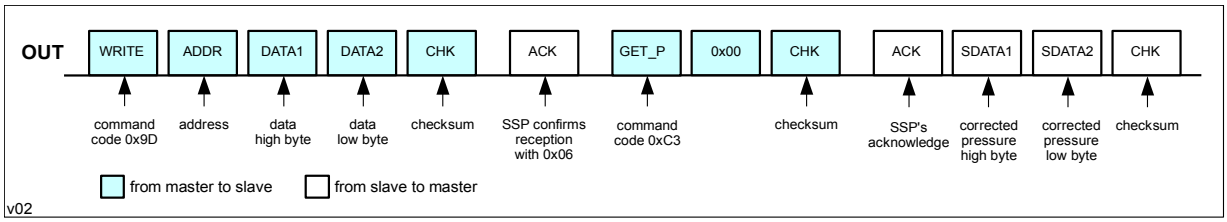


Figure 6.7.2.2-1: SIO Communication Protocol Example

6.7.2.3 CCP Commands

Table 6.7.2.3-1: Command Table

Command Name	***Command Code***	***Validity*** [1)]	***Description***
ENACONF	0x84	W	Go to configuration state. Activate full access to the SSP (read, write, BIST start and NVM update)
ENADIAG	0x8C	W	Go to diagnosis state. Activate restricted access to the SSP (read and BIST start)
READ_REG	0x9B	C, D	Read 8 bit register value
WRITE_REG	0x94	C	Write 8 bit value to register
READ_NVM	0x93	C, D	Read 16 bit value from NVM
WRITE_NVM	0x9D	C	Write 16 bit value to NVM
BIST	0xB4	C, D	Execute sensor path BISTs
GET_P	0xC3	C, D	Read pressure
GET_T	0xCB	C, D	Read temperature
GETELID	0xCA	C, D	Read ELMOS Device ID
GETELFA	0xDA	C, D	Read ELMOS Product Family ID
GETROMCRC	0xEA	C, D	Read ROM CRC

[1)] W - during Start-up Window, C - Configuration State, D - Diagnosis State

Table 6.7.2.3-2: Command ENACONF

Command Name	***ENACONF - enable full access***
Function	Go to **configuration state**. Activates full access to the SSP (read, write and NVM update)
Validity	• Only during SIO command window t_{Window} • If there is an NVM area which is not write protected.
Command Code	Byte 1 : 0x84
Following Bytes	Byte 2 : 0xE5 (constant) Byte 3 : 0x5E (constant) Byte 4 : 0xC8 (checksum)
Answer	Byte 1 : • 0x06 (ACK). if configuration state is entered • 0x15 (NACK), if command, any parameter or checksum is invalid

Table 6.7.2.3-3: Command ENADIAG

Command Name	*ENADIAG - enable restricted access*
Function	Go to **diagnosis state**. Activate restricted access to the SSP (read)
Validity	Only during SIO command window t_{Window}
Command Code	Byte 1 : 0x8C
Following Bytes	Byte 2 : 0xE5 (constant) Byte 3 : 0x5E (constant) Byte 4 : 0xD0 (checksum)
Answer	Byte 1 : • 0x06 (ACK), if diagnostic state is entered • 0x15 (NACK), if command, any parameter or checksum is invalid

Table 6.7.2.3-4: Command READ_REG

Command Name	*READ_REG - read 8 bit value*
Function	Read an 8 bit value from register
Validity	• After activation of configuration or diagnosis state • Only addresses between 0x70 and 0x7E are allowed
Command Code	Byte 1 : 0x9B
Following Bytes	Byte 2 : Address Byte 3 : Checksum
Answer	Byte 1 : • 0x06 (ACK) => Byte 2 and Byte 3 will be sent • 0x15 (NACK), if address or checksum is invalid => no further Byte will be sent Byte 2 : Read byte Byte 3 : Checksum

Table 6.7.2.3-5: Command WRITE_REG

Command Name	*WRITE_REG - write 8 bit value*
Function	Write an 8 bit value to register
Validity	• After activation of configuration state • Only addresses between 0x70 and 0x7E are allowed
Command Code	Byte 1 : 0x94
Following Bytes	Byte 2 : Address Byte 3 : Byte to write Byte 4 : Checksum
Answer	Byte 1 : • 0x06 (ACK), if value was written • 0x15 (NACK), if command, address or checksum is invalid

Table 6.7.2.3-6: Command READ_NVM

Command Name	*READ_NVM - read 16 bit value*
Function	Read a 16 bit value from NVM
Validity	• After activation of configuration or diagnosis state • Only addresses between 0x00 and 0x5F are allowed
Command Code	Byte 1 : 0x93
Following Bytes	Byte 2 : Address Byte 3 : Checksum

Command Name	*READ_NVM - read 16 bit value*
Answer	Byte 1 : • 0x06 (ACK) => Byte 2 - Byte 4 will be sent • 0x15 (NACK), if address or checksum is invalid => no further Byte will be sent Byte 2 : High byte Byte 3 : Low byte Byte 4 : Checksum

Table 6.7.2.3-7: Command WRITE_NVM

Command Name	*WRITE_NVM - write 16 bit value*
Function	Write a 16 bit value to NVM
Validity	• After activation of configuration state • Only addresses between 0x00 and 0x55 are allowed • Writing to NVM takes about 8 milliseconds (typical: 4ms erase + 4ms write)
Command Code	Byte 1 : 0x9D
Following Bytes	Byte 2 : Address Byte 3 : High Byte to write Byte 4 : Low Byte to write Byte 5 : Checksum
Answer	Byte 1 : • 0x06 (ACK), if value was written • 0x15 (NACK), if command, address or checksum is invalid

Table 6.7.2.3-8: Command BIST

Command Name	*BIST - execute sensor path BISTs*
Function	Execute pressure and temperature sensor path BISTs
Validity	After activation of configuration or diagnosis state
Command Code	Byte 1 : 0xB4

Following Bytes	Byte 2 :
	• Bit[0]
	  • 0_b : select p1
	  • 1_b : select p2
	Byte 3 : value for PBISTSIG
	
	Byte 4 : Checksum

Answer	Byte 1 : • 0x06 (ACK), if answer is ready • 0x15 (NACK), if checksum is invalid Byte 2 : High byte of PADC Byte 3 : Low byte of PADC Byte 4 : High byte of TADC Byte 5 : Low byte of TADC Byte 6 : Checksum

Table 6.7.2.3-9: Command GET_P

Command Name	***GET_P - read pressure value***
Function	Read pressure values according to selection
Validity	After activation of configuration or diagnosis state
Command Code	Byte 1 : 0xC3

Following Bytes	Byte 2 :
	• Bit[0]
	  • 0_b : select corrected pressure (12 bit SENT value with 4 leading zero bits)
	  • 1_b : select uncorrected pressure (ADC value with lower bit(s) added to fill 16 bits)
	• Bit[1]
	  • 0_b : send p1 only
	  • 1_b : send p1 and p2
	Byte 3 : Checksum

Answer	Byte 1 : • 0x06 (ACK), if answer is ready • 0x07 (BEL), if answer is ready and an enabled error is present • 0x15 (NACK), if checksum is invalid *received Byte2[1] = 0_b: (p1 only)* Byte 2 : High byte of p1 Byte 3 : Low byte of p1 Byte 4 : Checksum *received Byte2[1] = 1_b: (p1 and p2)* Byte 2 : High byte of p1 Byte 3 : Low byte of p1 Byte 4 : High byte of p2 Byte 5 : Low byte of p2 Byte 6 : Checksum

Table 6.7.2.3-10: Command GET_T

Command Name	*GET_T - read temperature value*
Function	Read pressure values according to selection
Validity	After activation of configuration or diagnosis state
Command Code	Byte 1 : 0xCB

Following Bytes	Byte 2 :
	• Bit[0]
	  • 0_b : select corrected temperature (12 bit SENT value with 4 leading zero bits)
	  • 1_b : select uncorrected temperature (T_{raw})
	• Bit[1]
	  • 0_b : send T1 only
	  • 1_b : send T1 and T2
	Byte 3 : Checksum

Answer	Byte 1 : (**note:** can be delayed maximal by around T_{TADC_CONV} for each if new T measurement) • 0x06 (ACK), if answer is ready • 0x07 (BEL), if answer is ready and an enabled error is present • 0x15 (NACK), if checksum is invalid *received Byte2[1] = 0_b: (T1 only)* Byte 2 : High byte of T1 Byte 3 : Low byte of T1 Byte 4 : Checksum *received Byte2[1] = 1_b: (T1 and T2)* Byte 2 : High byte of T1 Byte 3 : Low byte of T1 Byte 4 : High byte of T2 Byte 5 : Low byte of T2 Byte 6 : Checksum

Table 6.7.2.3-11: Command GETELID

Command Name	*GETELID - read ELMOS device ID*
Function	Read ELMOS Device ID
Validity	After activation of configuration or diagnosis state
Command Code	Byte 1 : 0xCA
Following Bytes	Byte 2 : 0xCB (checksum)
Answer	Byte 1 : • 0x06 (ACK) => Byte 2 - 6 will be sent • 0x15 (NACK), if checksum is invalid => no further Byte will be sent Byte 2 - 5 : ELMOS ID, highest byte first [1)] Byte 6 : Checksum

1) stored in NVM registers 0x56-0x57 (2*16 bit)

Table 6.7.2.3-12: Command GETELFA

Command Name	*GETELFA - read ELMOS Product Family ID*
Function	Read ELMOS Product Family ID
Validity	After activation of configuration or diagnosis state

Command Name	*GETELFA - read ELMOS Product Family ID*
Command Code	Byte 1 : 0xDA
Following Bytes	Byte 2 : 0xDB (checksum)
Answer	Byte 1 : • 0x06 (ACK), if answer is ready => Byte 2 - 6 will be sent • 0x15 (NACK), if checksum is invalid => no further Byte will be sent Byte 2 : Project Number (=0x2F=47) Byte 3 : Product Family[11:4] (=0x**20**8=520) Byte 4 : Product Family[03:0] (=0x20**8**=520) + HW version[3:0] (M52047A=1) Byte 5 : SW version[7:0] (M52047A=1) Byte 6 : Checksum

Table 6.7.2.3-13: Command GETROMCRC

Command Name	*GETROMCRC - read ROM CRC*
Function	Read the ROM checksum (CRC)
Validity	After activation of configuration or diagnosis state
Command Code	Byte 1 : 0xEA
Following Bytes	Byte 2 : 0xEB (checksum)
Answer	Byte 1 : • 0x06 (ACK) => Byte 2 - 4 will be sent • 0x15 (NACK), if checksum is invalid => no further Byte will be sent Byte 2 - 3 : ROM CRC, highest byte first [1)] Byte 4 : Checksum

1) stored in last ROM cell

Note:
The common command processor CCP receives data regardless from which interface it has been received. It also decides to which destination the data is to be sent. If at least one byte was received via I2C then the answer is directed to I2C, too. Only if all received bytes come from the SIO then the answer is sent to the SIO.
This implies communication should not happen simultaneously via SIO and I2C.

6.8 NVM - Non-Volatile Memory

6.8.1 NVM (Configuration Memory)

As configuration memory a 128x16 bits NVM is implemented. The NVM stores:

- internal IC trimming data
- IC configuration bits
- bridge and temperature sensor characteristic correction parameters
- further data like IDs or OEM specific data

The NVM data can be read or written in Configuration Mode via SIO (at pin OUT) or via the I2C interface. For details see chapters 6.6 and 6.7.

The following table shows the NVM content map:

Table 6.8.1-1: NVM Memory Map

Address	*Name*	*Delivery State*	*Format 1)*	*Description*
Block 1	==========	=========	==========	**OEM range**
0x00 .. 0x07	OEM[0..7]	8x 0x0000	I 12	SENT slow channel data: OEM part number or other information
0x08	LOCK1	4) 0x5A51	I 16	for write protection of 0x00 .. 0x09
0x09	CRC1	5) 0xBBB0	I 16	checksum for 0x00 .. 0x08
Block 2	==========	=========	==========	**sensor calibration range**
0x0A .. 0x33	MSG[0 .. 41]	42	42 * M 16	SENT slow channel data
0x34 .. 0x37		4 * 0x0000		4 * 16 bits free
0x38	2) DGAIN1, DOFFS1	0x0000	2 * F 8	linear delta-gain and delta-offset correction of channel P1
0x39	2) DGAIN2, DOFFS2	0x0000	2 * F 8	linear delta-gain and delta-offset correction of channel P2
0x3A	2) I2C_CTRL	0x0060	like SFR	value for I2C_CTRL (8 bits free)
0x3B	2) PGAIN1, POFFS1	0x4000	like SFRs	values for PGAIN1, POFFS1
0x3C	2) PGAIN2, POFFS2	0x0000	like SFRs	values for PGAIN2, POFFS2
0x3D	2) SENTCONF1, SENTCONF2	0x0083	like SFRs	values for SENTCONF1 and SENTCONF2
0x3E	2) SENTCONF3, SENTCONF4	0x015D	bits	values for SENTCONF3 and SENTCONF4
0x3F	2) ERR_EN1, ERR_EN2	0xFF3F	bits	BIST enable bits
0x40	2) ERR_EN3, ERR_EN4	0xC83F	bits	BIST enable bits
0x41	P_DIFF_0	0x0366	I 16	SENT output for pressure difference 0 for FC1='p1-p2'

Address	Name	Delivery State	Format 1)	Description
0x42	3) RT1_LIM	0xE613	2 * I 8	maximum (upper) and minimum (lower 8 bit) for TADC valid range check for logical temperature T1
0x43	3) RT2_LIM	0xE613	2 * I 8	maximum (upper) and minimum (lower 8 bit) for TADC valid range check for logical temperature T2
0x44	PV_LIM	0x0000	I 16	maximum pressure difference (for P voter)
0x45	3) TV_LIM	0x0000	2 * F 8	maximum temperature differences (for T voter)
0x46	TNUM1_ADC	0x0000	like TADC	synthetic T-ADC value #1 for numeric BIST
0x47	TNUM1_OUT	0x0000	I 16	expected output (SENT)
0x48	PNUM1_ADC	0x0000	like PADC	synthetic P-ADC value #1 for numeric BIST
0x49	PNUM1_OUT	0x0000	I 16	expected output (SENT)
0x4A	PNUM2_ADC	0x0000	like PADC	synthetic P-ADC value #2 for numeric BIST
0x4B	PNUM2_OUT	0x0000	I 16	expected output (SENT)
0x4C	2) PSP_DAC	0x0101	2 * I 8	DAC values for sensor path BIST (p2 (upper) and p1)
0x4D	3) PSP1_LIM	0x8E80	2 * I 8	expected PADC1 values for pressure path BIST (minimum and maximum, upper 8 bits)
0x4E	3) PSP2_LIM	0x8E80	2 * I 8	expected PADC2 values for pressure path BIST (minimum and maximum, upper 8 bits)
0x4F	3) TSP_LIM	0x6759	2 * I 8	expected TADC values for temperature path BIST (minimum and maximum, upper 8 bits)
0x50	C1_00	0x0200	F 16	pressure linearization: offset (sensor 1)
0x51	C1_01	0x0000	F 16	pressure linearization: temperature 1st order
0x52	C1_02	0x0000	F 16	pressure linearization: temperature 2nd order
0x53	C1_03	0x0000	F 16	pressure linearization: temperature 3rd order
0x54	C1_10	0x0400	F 16	pressure linearization: pressure 1st order
0x55	C1_11	0x0000	F 16	pressure linearization: pressure 1st order, temperature 1st order
0x56	C1_12	0x0000	F 16	pressure linearization: pressure 1st order, temperature 2nd order
0x57	C1_13	0x0000	F 16	pressure linearization: pressure 1st order, temperature 3rd order
0x58	C1_20	0x0000	F 16	pressure linearization: pressure 2nd order
0x59	C1_21	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 1st order
0x5A	C1_22	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 2nd order
0x5B	C1_23	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 3rd order
0x5C	C2_00	0x0200	F 16	pressure linearization: offset (sensor 2)
0x5D	C2_01	0x0000	F 16	pressure linearization: temperature 1st order
0x5E	C2_02	0x0000	F 16	pressure linearization: temperature 2nd order
0x5F	C2_03	0x0000	F 16	pressure linearization: temperature 3rd order
0x60	C2_10	0x0400	F 16	pressure linearization: pressure 1st order
0x61	C2_11	0x0000	F 16	pressure linearization: pressure 1st order, temperature 1st order

Address	Name	Delivery State	Format 1)	Description
0x62	C2_12	0x0000	F 16	pressure linearization: pressure 1st order, temperature 2nd order
0x63	C2_13	0x0000	F 16	pressure linearization: pressure 1st order, temperature 3rd order
0x64	C2_20	0x0000	F 16	pressure linearization: pressure 2nd order
0x65	C2_21	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 1st order
0x66	C2_22	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 2nd order
0x67	C2_23	0x0000	F 16	pressure linearization: pressure 2nd order, temperature 3rd order
0x68	2) T1_MODE	0x0000		for temperature #1 (8 bits free)
0x69	T1_Q0	0x1FF2	F 16	for trimming
0x6A	T1_Q1	0xF8DA	F 16	
0x6B	T1_Q2	0x0000	F 16	
0x6C	T1_Q3	0x0000	F 16	
0x6D	T1_Q4	0x3E5F		for prescaling
0x6E	2) T2_MODE	0x0001		for temperature #2 (8 bits free)
0x6F	T2_Q0	0x1FF2	F 16	for trimming
0x70	T2_Q1	0xF8DA	F 16	
0x71	T2_Q3	0x0000	F 16	
0x72	T2_Q3	0x0000	F 16	
0x73	T2_Q4	0x3E5F		for prescaling
0x74	LOCK2	4) 0x5A52	I 16	for write protection of 0x0A .. 0x75
0x75	CRC2	5) 0x3638	I 16	checksum from 0x0A .. 0x74

1) Format:

- F 16 - 16 bit fixed point
- F 8 - 8 bit fixed point
- I 16 - 16 bit integer
- I 12 - 12 bit integer
- I 8 - 8 bit integer
- M 16 - special coding for SENT slow channel sequence as explained in the tables below

2) If only one 8 bit value is stored in one (16 bit) NVM cell, the lower 8 bits are used. If two 8 bit values are stored, the first value (like PGAIN1 or ERR_EN3) is stored in the lower 8 bits and the second value (like POFFS1 or ERR_EN4) are stored in the higher 8 bits.

3) The upper limit (maximum) for sensor path BISTs and for the T voter are stored in the upper 8 bits of the NVM cell, the lower limit (minimum) is stored in the lower 8 bits.

4) Every data block has a separate locking mechanism. There is only one 16 bit code, which enables writing into this block. All other LOCKx data words lock the writing. The defined delivery code allows the writing.
In configuration mode "unlock code" from delivery can be changed to a lock code (all other values). Then further write operations are still possible as long as configuration mode is not left. It has to be considered, that the CRC code for the block to lock is correct before leaving configuration code. The locking gets active with next start of configuration mode.

5) CRC calculated, fitting to the delivered NVM content.

6) Delivery state contains here fix values instead of individual temperature sensor diode calibration values (roughly fitting to a "typical" diode). The exact and individual bridge sensor temperature calibration is to be done within and in combination with pressure sensor calibration process.

NVM CRC Calculation

The following C code fragment shows how to calculate the NVM's 16 bit CRC checksums to be stored in last NVM word of each of the three NVM blocks. This sample shows the calculation for the first block (0x00 to 0x09). The checksum is calculated for the words 0x00 to 0x08 and stored in 0x09.

```
typedef unsigned short uint16_t;

//-----------------------------------------------------
static uint16_t Crc(uint16_t sig, uint16_t data)
//-----------------------------------------------------
{
  uint16_t bit15 = (sig >> 15) & 1;
  uint16_t bit14 = (sig >> 14) & 1;
  uint16_t bit12 = (sig >> 12) & 1;
  uint16_t bit3  = (sig >>  3) & 1;
  uint16_t fb = bit15 ^ bit14 ^ bit12 ^ bit3;

  sig = (sig << 1) ^ data ^ fb;
  return sig;
}

//-----------------------------------------------------

  uint16_t aData[128];
  uint16_t nCrc;
  int      iAddr;

  nCrc = (uint16_t)(-1);
  for(i=0x00;iAddr<0x09;iAddr++) {
    nCrc = Crc(nCrc,aData[iAddr]);
  }

  aData[0x09] = nCrc;
```

Figure 6.8.1-1: Code Fragment for NVM CRC Calculation

As to be seen in example, the CRC is calculated from 1st word of block until and including address containing locking word.

6.8.2 OTP (ROM)

The Digital Processing Unit (DPU) takes its code from an OTP memory (One Time Programmable).
The content is initialized before delivery of IC.

This memory has several safety measures implemented. Memory errors can be corrected and if not possible detected. For details see special chapter 6.10.14.

6.9 OSC - Oscillator

There is one central oscillator implemented to deliver logic clock mainly for:

- control logic (CONTROL)
- sigma-delta ADCs for pressure and temperature (PADC1, PADC2, TADC)
- correction unit (CORRECT)
- all timings in interfaces (SENT_DIG, I2C, SIO)

The oscillator is trimmed in production at ELMOS. Trim data are read from the non-volatile memory at device start-up from reset state.

6.10 Functional Safety

This IC is developed according to **ISO26262**, based on safety requirements rated up to **ASIL C**.

6.10.1 Safety Measures and Diagnosis

Functional Safety is the responsibility of the system integrator. For customers with requirements up to ASIL C the use of the following safety measures might be mandatory.
As well we highly recommend P/S (pressure secure) configuration of SENT interface.

6.10.1.1 Fault Tolerance Time Interval - FTTI

The terms needed for calculation of FTTI shall be defined here:

- **FTTI:** fault tolerance time ==> time between fault is present in the system until safe state can be reached
- **DT:** diagnostic time ==> time between fault is present in the system until fault is detected within sensor IC
- **FRT:** fault reaction time ==> time between fault is detected within sensor IC until next level system reaches safe state here we assume:
  - 1 SENT protocol transmission times with fastest tick time definition of 3µs if the diagnostic reaction is IC reset
  - 1..2 SENT protocol transmission times with fastest tick time definition of 3µs otherwise

Necessary respectively fastest FTTI calculates as follows:

$$FTTI = DT + FRT$$

We define additionally a **diagnostic cycle time**, which describes the repetition rate of a specific safety measure. Usually the diagnostic time should be larger or equal to this diagnostic cycle time, but from the examples below we also see situations with diagnostic time shorter than the cycle time. This is due to a time interleaved data acquisition and data processing. Therefore, even cases exist, where the effect of faults to transmitted pressure data are delayed longer than the detection of a fault which results in diagnostic time zero (DT = 0).
See below for some examples in detail.

The 6.10.1.1-1 defines several failure timing terms which are later on given for the different safety measures in the overview table below. The specific situation for safety measure SM21 (bridge sensor diagnostic) is depicted.

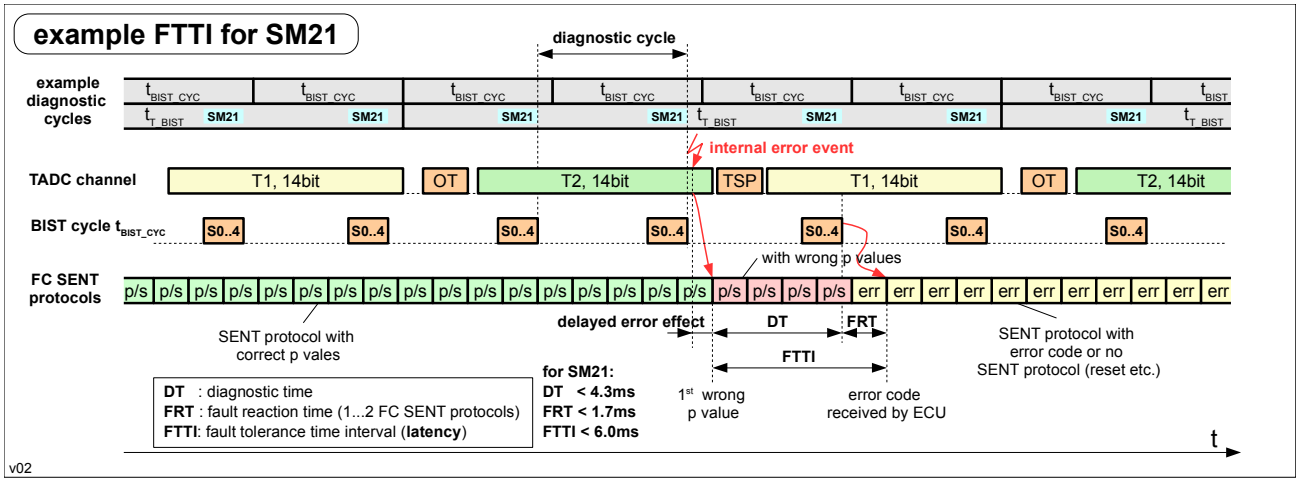


Figure 6.10.1.1-1: Definition of Failure Timing Terms, Example SM21

It follows a further example for FTTI calculation for SM34 (temperature digital calculation BIST for channel T1). Only wrong T1 values can cause wrong linearization and by that wrong pressure values.

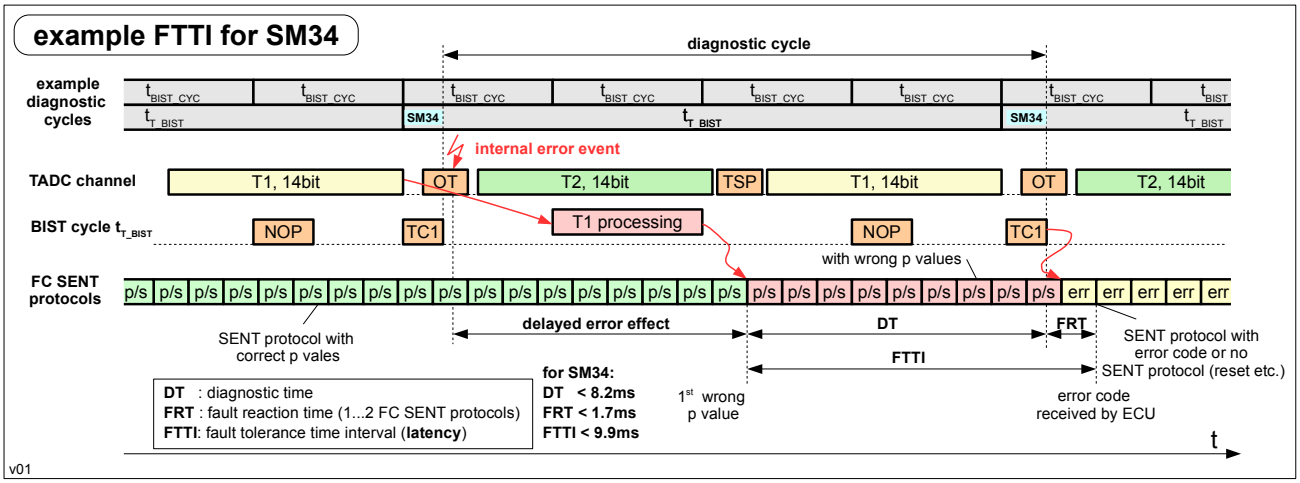


Figure 6.10.1.1-2: Definition of Failure Timing Terms, Example SM34

Next example depicts FTTI calculation for SM61 (TV - temperature voter). For safety reasons the usage of both possible temperature channels T1 and T2 with independent temperature sensors and the comparison of both values with this SM61 for temperature voting is recommended. The FTTI can be derived as follows:

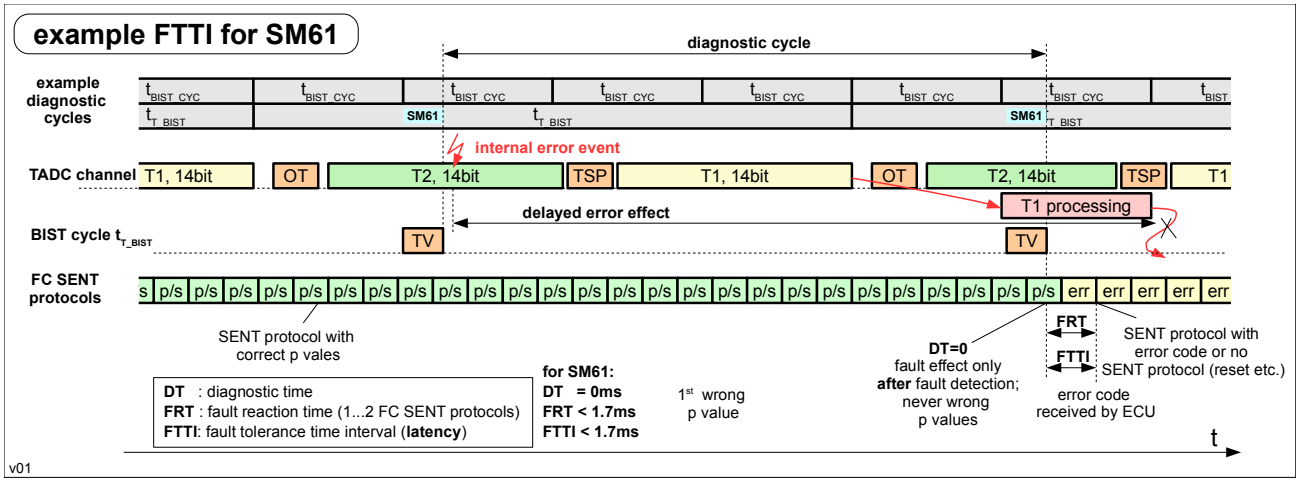


Figure 6.10.1.1-3: Definition of Failure Timing Terms, Example SM61

6.10.1.2 Safety Measures Overview

The IC provides a large set of self test functions which can be classified as:

- supply voltage monitors
- digital control flow window watchdog
- sensor surveillance tests (bridge and temperature sensor diagnosis)
- BIST: complex system self tests for memories and signal flow (**B**uilt **I**n **S**elf **T**est)
- interface checks

Most checks can be controlled via enable flags, see later in chapter 6.10.1.

Table 6.10.1.2-1: Overview about Safety Measures

SM-ID	Name	Reaction / Info 1)	Description	Cycle 2)	DT 3)	FTTI 6)
SM01	V5L_ERR	FC+SC	supply voltage monitoring VS undervoltage	$1/f_{PSEN\_UPDT}$	0.25ms	2.0ms
SM02	V5H_ERR	FC+SC	supply voltage monitoring VS overvoltage	$1/f_{PSEN\_UPDT}$	0.25ms	2.0ms
SM03	VDDA_UV VDDA_OV	reset 4)	regulator voltage monitoring VDDA undervoltage and overvoltage	0	0	0.9ms 7)
SM04	VDDD_UV VDDD_OV	reset 4)	regulator voltage monitoring VDDD undervoltage and overvoltage	0	0	0.9ms 7)
SM05	CAP_LOSS	reset 4)	VDDA capacitor loss check	t_{BIST_CYC}	4.3ms	5.1ms 7)
SM07	OVP/RVP	(protection)	reverse and overvoltage protection at pin VS	no diag.	-	-
SM08	RDN_REF	reset	redundant 2nd band-gap reference: voting between 1st and 2nd reference	0	0	0.9ms 7)
SM09	VSM_ERR	FC+SC	self test of internal VS monitors for overvoltage and undervoltage (against **latent** monitor failure)	t_{T_BIST}	17.2ms	18.9ms 9)
SM11	WD	reset 5)	internal window watchdog for correct task scheduling (control flow)	t_{BIST_CYC}	5.4ms	6.3ms 7)
SM21	S0, S1, S2, S3, S4	FC+SC	bridge sensor diagnostic (different terminal opens and shorts)	t_{BIST_CYC}	4.3ms	6.0ms
SM22	NOP_ERR	FC+SC	NTC (or PTC, ...) sensor open at pin TSEN2 (pin open respectively too high impedance)	t_{T_BIST}	3.8ms	5.5ms
SM23	RT2_ERR	FC+SC	NTC (or PTC, ...) sensor value out of range at pin TSEN2 (TADC value unexpected low or high)	t_{T_BIST}	0	1.7ms
SM24	RTx_ERR	FC+SC	diode sensor diagnostic (unexpected low or high diode voltage)	t_{T_BIST}	0	1.7ms
SM25	OT_ERR	FC+SC	IC overtemperature monitor	t_{T_BIST}	18.2ms	19.9ms 10)
SM31	PSP1_ERR PSP2_ERR	FC+SC	pressure analogue signal path power-up BIST for channels p1 and p2 (**latent faults only**)	next power-up	next power-up	next power-up 9)
SM32	PC1_ERR PC2_ERR	FC+SC	pressure digital calculation BIST for channel p1 and channel p2	t_{BIST_CYC}	4.3ms	6.0ms
SM33	TSP_ERR	FC+SC	temperature analogue signal path BIST	t_{T_BIST}	3.6ms	5.3ms
SM34	TC1_ERR	FC+SC	temperature digital calculation BIST for channel T1	t_{T_BIST}	8.2ms	9.9ms
SM41	RAM_CHCK	reset	RAM check at power-up (**latent faults only**)	next power-up	next power-up	next power-up 9)
SM42	RAM_PAR	reset	RAM content parity check	0	0	0.9ms 7)
SM43	NVM_CRC	reset	configuration NVM content check by 16 bit CRC calculation	t_{BIST_CYC}	5.1ms	6.8ms
SM44	ROM_CRC	reset	ROM (OTP) content check by 16 bit CRC calculation	t_{ROM_BIST}	9.0ms	9.9ms 8)
SM45	REG_PAR	reset	register parity check	0	0	0.9ms 7)

SM-ID	Name	Reaction / Info 1)	Description	Cycle 2)	DT 3)	FTTI 6)
SM46	ROM_ECC	(protection)	error correction code (ECC) for OTP word: logic corrects 1-bit errors and detects 2-bit errors (which leads to a IC rest)	no diag.	-	-
SM47	NVM_KEY	(protection)	protection against unwanted write of configuration NVM	no diag.	-	-
SM48	NVM_COR	(protection)	inherent redundancy in configuration NVM bit cell	no diag.	-	-
SM49	PRG_CHCK	(protection)	check after programming with different read-thresholds for deep programming level	no diag.	-	-
SM50	REG_UPD	(protection)	register update (cyclic hardware register refresh from CRC checked configuration NVM memory)	no diag.	-	-
SM51	T1_SAT T2_SAT	FC+SC	temperature sensor saturation check for channel T1 and T2	t_{T_BIST}	0	1.7ms
SM52	P1_SAT P2_SAT	FC+SC	pressure sensor saturation check for channel p1 and p2	$1/f_{PSEN\_UPDT}$	0	1.7ms
SM61	TV_ERR	FC+SC	temperature voter: compare of both temperature measurement channels T1 and T2	t_{T_BIST}	0	1.7ms
SM62	PV_ERR	FC+SC	pressure voter: compare of both pressure measurement channels p1 and p2	$1/f_{PSEN\_UPDT}$	0	1.7ms
SM63	DPU_CHCK	reset	Digital Processing Unit (DPU) check (with special tests for pressure and temperature voter)	t_{BIST_CYC}	4.3ms	6.0ms
SM64	ILL_OPC	reset	illegal opcode detection	0	0	0.9ms 7)
SM91	IF_CHCK	FC+SC	interface check of FC- and SC-SENT data (evaluation of data CRC and of message counter in P/S SENT mode; P/S mode of interface recommended for safety applications; sync pulse plausibility check in receiver)	1 FC protocol	(system level)	1ms possible
SM92	IF_CHCK2	FC	interface consistency check of FC data: receiving ECU shall check, status error bit is set if and only if at least one FC value is 1, 4088 or 4090 (necessary to ensure error detection, if one of this error signals is blocked by an internal or external single fault)	1 FC protocol	(system level)	1ms possible
SM93	SENT_WD	reset	check for outdated SENT FC data (internal digital interface check)	1 FC protocol	4 FC protocols	4.2ms

Note: Frequently used abbreviations: SM=Safety Mechanism; SC=Slow Channel SENT; FC=Flow Channel SENT
1) Information channel for diagnostic result: **FC+SC**: error is reported via SENT fast and slow channel; **reset**: error causes reset event and restart of IC. Periodically restart has to be detected on system level.
2) Diagnostic cycle time according definition in 6.10.1.1-1.
3) Diagnostic time (DT) according definition in 6.10.1.1-1.
Effective latency (FTTI) can be calculated by adding of duration of two transmitted FC SENT protocols.
4) This reset event sets the bit PON=1 to indicate, that power-on reset happened (WD bit is cleared to 0).
5) This reset event sets the bit WD=1 to indicate, that watchdog reset happened (PON bit is untouched).
6) FTTI = DT + FRT; fault reaction time FRT < 2x t_{SENT_PROT} (here assumed with p/s mode with 3µs ticks and pause pulse)
7) For reset as fault reaction we calculate with FRT of one SENT protocol duration (current protocol corrupted or next protocol missing).
8) Diagnostic time for ROM check is in worst case two ROM check cycles long. For FTTI one SENT protocol length has to be added to notice, that IC made reset.
9) The corresponding SM is considered only for **latent error diagnostic**, so longer FTTI is allowed.
10) SM not considered in FIT rate calculation, because FTTI > 10ms.

6.10.1.3 Safety Measures Sequence

All types of BISTs can be enabled via special BIST control registers, see chapter 6.10.1.3-1.
Nevertheless there is a fixed scheduler frame with the pressure and temperature measurements and BISTs. This frame is independent from enabled or disabled BISTs.

After power on there is a time window t_{Window} to allow login into configuration or diagnostic mode via SIO interface. During that time pin OUT is tristate and SENT interface is still blocked.
Parallel to listening for possible SIO commands internally most BIST checks are performed **before** first SENT protocols are sent. 6.10.1.3-1 depicts this sequence.

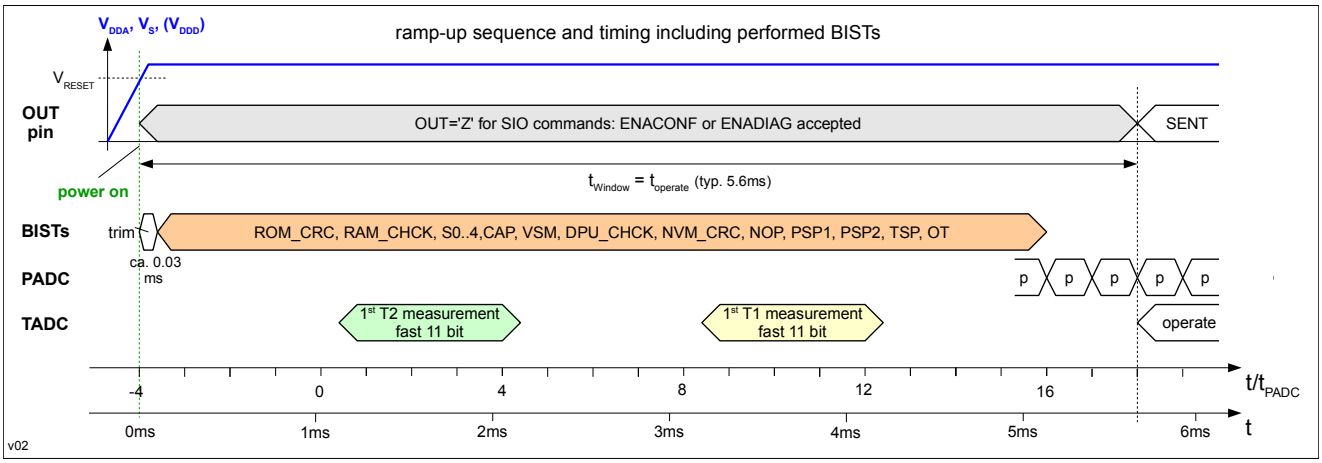


Figure 6.10.1.3-1: Start-up Timing and BISTs

After operation mode is reached a sequence according 6.10.1.3-2 is repeated endless until power-down or until any BIST check causes a reset event.

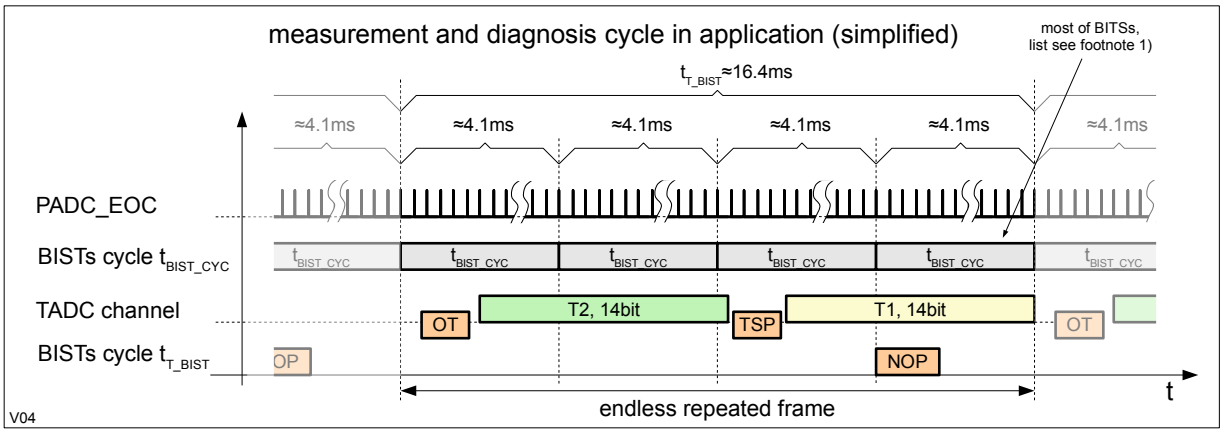


Figure 6.10.1.3-2: Overview Measurement and BIST Main Cycle

After power-on the IC starts again with sequence shown in 6.10.1.3-1. If reset was caused by any BIST (and not by supply voltage level) the general sequence is the same, but then the SIO login would be locked.
BISTs performed during the cycle time t_{BIST_CYC} are listed in 6.10.1.2-1 with cycle time 4.1ms.

6.10.1.4 Safety Measures Enabling Registers

This chapter describes the four NVM registers with enable bits for certain diagnostic and BIST tests or other checks. Only if the enable bits are set to 1, the corresponding check will be performed and the error bit will be set in case of a detected error.

Note:
ERR_EN1/2 as well as ERR_EN3/4 share each one 16-bit NVM word. ERR_EN1/3 are the low bytes and ERR_EN2/4 are the high bytes of this word.

Table 6.10.1.4-1: Error check enable registers [NVM]

Register Name	*Address*	*Description*
ERR_EN1 [NVM]		BIST enable bits (in NVM)
ERR_EN2 [NVM]		BIST enable bits (in NVM)
ERR_EN3 [NVM]		BIST enable bits (in NVM)
ERR_EN4 [NVM]		BIST enable bits (in NVM)

Table 6.10.1.4-2: Register **ERR_EN1 [NVM]** BIST enable bits (in NVM)

	MSB							*LSB*
Content	PV_EN	TV_EN	V5H_EN	V5L_EN	CAP_EN	TSP_EN	PSP2_EN	PSP1_EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**PV_EN** : enable pressure voter check **TV_EN** : enable temperature voter check **V5H_EN** : enable V_{VS} out of range error; too high **V5L_EN** : enable V_{VS} out of range error; too low **CAP_EN** : enable VDDA buffer capacitor check **TSP_EN** : enable temperature signal path BIST **PSP2_EN** : enable power-up pressure signal path BIST, channel 2 **PSP1_EN** : enable power-up pressure signal path BIST, channel 1							

Table 6.10.1.4-3: Register **ERR_EN2 [NVM]** BIST enable bits (in NVM)

	MSB							*LSB*
Content	S42_EN	S32_EN	S22_EN	S02_EN	S41_EN	S31_EN	S21_EN	S01_EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**S42_EN** : enable short detection between INN2 and INP2 **S32_EN** : enable open detection at INN2, INP2 **S22_EN** : enable short detection between (INN2, INP2) and (EXHI, EXLO) **S02_EN** : enable open detection between EXHI and EXLO (diagnosis at pin INN2 and INP2) **S41_EN** : enable short detection between INN1 and INP1 **S31_EN** : enable open detection at INN1, INP1 **S21_EN** : enable short detection between (INN1, INP1) and (EXHI, EXLO) **S01_EN** : enable open detection between EXHI and EXLO (diagnosis at pin INN1 and INP1)							

Table 6.10.1.4-4: Register **ERR_EN3** ^{NVM} BIST enable bits (in NVM)

	MSB							***LSB***
Content	-	NOP_EN	RT2_EN	RT1_EN	T2SAT_EN	T1SAT_EN	P2SAT_EN	P1SAT_EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**NOP_EN** : enable TSEN2 too high impedance or open detection Note: Do not enable if sensor at TSEN2 is mapped to logical temperature channel T1. **RT2_EN** : enable out of range check for TADC values of logical temperature channel T2 Note: Limits to apply are flexible defined in NVM. **RT1_EN** : enable out of range check for TADC values of logical temperature channel T1 Note: Limits to apply are flexible defined in NVM. **T2SAT_EN** : enable T2 calculation saturation error check **T1SAT_EN** : enable T1 calculation saturation error check **P2SAT_EN** : enable P2 calculation saturation error check **P1SAT_EN** : enable P1 calculation saturation error check **Note:** ...SAT_EN bits only to disable DEC error code generation for unused channels.							

Table 6.10.1.4-5: Register **ERR_EN4** ^{NVM} BIST enable bits (in NVM)

	MSB							***LSB***
Content	OT_EN	VSM_EN	-	-	S1_EN	TC1_EN	PC2_EN	PC1_EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**OT_EN** : enable IC overtemperature check **VSM_EN** : enable VS monitor BIST **S1_EN** : enable short detection between EXHI and EXLO **TC1_EN** : enable numerical calculation BIST for channel T1 **PC2_EN** : enable numerical calculation BIST for channel p2 **PC1_EN** : enable numerical calculation BIST for channel p1							

It is highly recommended to generally enable all applicable safety measures for the specific application.

There are only a few exceptions, for example:
- if IC is used without any NTC connected to pin TSEN2 ==> we recommend to set **NOP_EN=0** to disable sensor diagnosis for NTC sensor and to avoid possible wrong error messages.
- if one bridge input is not used at all (for non-safety applications) ==> the corresponding bridge connection checks have to be disabled
- if channels are not used ==> the corresponding saturation checks shall be disabled
- if only one temperature channel is used ==> we recommend to set **RT2_EN=0** to disable TADC range check for unused channel T2

6.10.1.5 Error Indication Registers

Corresponding to the four enable registers from preceding sub-chapter there are four registers with error indication bits and additionally one further ERRC5 register for error indication of checks without enable bits.
Register number and position directly correspond to the enable bits. These registers can be read out in configuration or diagnostic mode.
From this data SENT error information is generated, see 6.6.1.4-1.

Table 6.10.1.5-1: Error check result registers

Register Name	*Address*	*Description*
ERRC1	0x72	error check result register (1st byte)
ERRC2	0x73	error check result register (2nd byte)
ERRC3	0x74	error check result register (3rd byte)
ERRC4	0x75	error check result register (4th byte)
ERRC5	0x76	error check result register (4th byte)

Table 6.10.1.5-2: Register **ERRC1** (0x72) error check result register (1st byte)

	MSB							*LSB*
Content	PV_ERR	TV_ERR	V5H_ERR	V5L_ERR	-	TSP_ERR	PSP2_ERR	PSP1_ERR
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**PV_ERR** : pressure voter check error **TV_ERR** : temperature voter check error **V5H_ERR** : V_{VS} out of range error; too high **V5L_ERR** : V_{VS} out of range error; too low **TSP_ERR** : temperature signal path BIST error **PSP2_ERR** : power-up pressure signal path BIST error, channel p2 **PSP1_ERR** : power-up pressure signal path BIST error, channel p1							

Table 6.10.1.5-3: Register **ERRC2** (0x73) error check result register (2nd byte)

	MSB							*LSB*
Content	S42_ERR	S32_ERR	S22_ERR	S02_ERR	S41_ERR	S31_ERR	S21_ERR	S01_ERR
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**S42_ERR** : input short (INN2 to INP2) **S32_ERR** : open sensor at INN2, INP2 **S22_ERR** : short between (INN2, INP2) and (EXHI, EXLO) **S02_ERR** : open at bridge excitation between EXHI and EXLO (diagnosis at pin INN2 and INP2) **S41_ERR** : input short (INN1 to INP1) **S31_ERR** : open sensor at INN1, INP1 **S21_ERR** : short between (INN1, INP1) and (EXHI, EXLO) **S01_ERR** : open at bridge excitation between EXHI and EXLO (diagnosis at pin INN1 and INP1)							

Table 6.10.1.5-4: Register **ERRC3** (0x74) error check result register (3rd byte)

	MSB							***LSB***
Content	-	NOP_ERR	RT2_ERR	RT1_ERR	T2_SAT	T1_SAT	P2_SAT	P1_SAT
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NOP_ERR** : open error at pin TSEN2 (or too high impedance) **RT2_ERR** : out of range check for logical channel T2 (diode short or open according levels V_{DIO_SHORT} and V_{DIO_OPEN} or NTC range limits, see parameters V_{NTC_MIN} and V_{NTC_MAX}) **RT1_ERR** : out of range check for logical channel T1 (diode short or open according levels V_{DIO_SHORT} and V_{DIO_OPEN} or NTC range limits, see parameters V_{NTC_MIN} and V_{NTC_MAX}) **T2_SAT** : saturation error during T2 calculation **T1_SAT** : saturation error during T1 calculation **P2_SAT** : saturation error during P2 calculation **P1_SAT** : saturation error during P1 calculation							

Table 6.10.1.5-5: Register **ERRC4** (0x75) error check result register (4th byte)

	MSB							***LSB***
Content	OT_ERR	VSM_ERR	-	-	S1_ERR	TC1_ERR	PC2_ERR	PC1_ERR
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**OT_ERR** : IC overtemperature error **VSM_ERR** : VS monitor BIST error **S1_ERR** : short between EXHI and EXLO **TC1_ERR** : numerical calculation BIST error for channel T1 **PC2_ERR** : numerical calculation BIST error for channel p2 **PC1_ERR** : numerical calculation BIST error for channel p1							

Table 6.10.1.5-6: Register **ERRC5** (0x76) error check result register (4th byte)

	MSB							***LSB***
Content	-	NV3_ERR	NV2_ERR	NV1_ERR	-	-	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NV3_ERR** : NVM error in CRC3 **NV2_ERR** : NVM error in CRC2 **NV1_ERR** : NVM error in CRC1							

Note:

The bits NVM1_ERR, NVM2_ERR and NVM3_ERR only appear in diagnostic or configuration mode. NVM CRC errors detected in operational mode lead to a reset.

6.10.2 Voltage Monitors - SM01, SM02, SM03, SM04

The IC provides diagnostic functions to **supervise the availability of supply voltage** in the specified range as follows:

- main supply voltage monitor for V_{VS} (too high / too low, see chapter 6.2)
- power-on-reset generator (POR) monitoring internal analogue V_{VDDA} and digital V_{VDDD} (see chapter 6.2)
- overvoltage monitoring of internal analogue V_{VDDA} and digital V_{VDDD}

Check of VS can be enabled by setting **V5H_EN** and/or **V5L_EN** in error enable NVM registers ERRCx.
If in that case the supply V_{VS} is lower than V_{VS_LOW} or above V_{VS_HIGH} the error bits **V5H_ERR** or **V5L_ERR** will be set to 1 which can be read from a diagnosis register and via SENT data output.

In case the digital or analogue supply regulator output drops below or rises above a critical threshold a power-on-reset is triggered.

6.10.3 Buffer Capacitor Loss Check - SM05

Because external buffer capacitance C_{VDDA} at pin VDDA is needed for precise measurement, there is additionally a capacitor loss check implemented. This diagnosis is enabled with **CAP_EN**=1.
An activated and failed test causes IC reset and restart as from power-up.

6.10.4 VS Monitor Check - SM09

To avoid latent errors in VS overvoltage and undervoltage monitor there is a VS monitor check (self test) implemented, which runs once during start-up sequence before any SENT transmission starts and cyclically in operating mode.
The check can be enabled/disabled with bit **VSM_EN**.
If check enabled, a potential error in this self test would be indicated via bit **VSM_ERR** in register ERRC4.
This leads to an error propagation into SENT FC and SC data.

6.10.5 Window Watchdog (WD) - SM11

To avoid accidental failures during operation (e.g. caused by transient disturbances) a **window watchdog** monitor is integrated. This watchdog checks for the following:

- the correct working of task scheduling, calculation and control engine
- proper operation of main DPU clock by means of a separate watchdog oscillator (running at f_{INT})

Expected watchdog trigger period is t_{BIST_CYC}, same as for most BIST checks. Watchdog window is chosen center-aligned around that period.

If the watchdog monitor is not triggered within the specified window, reaction is as follows:

- flag bit **WD** is set in MISC_STAT register
- system reset is triggered

After reset the IC starts with nearly the same sequence as for normal power-on. Only the SIO command window is not started as usual, so nothing would be interpreted as SIO command.

6.10.6 Bridge Sensor Diagnosis - SM21

The chip provides surveillance for the sensor and its connections to the device. The following events can be detected:

- **S0x_ERR**: open at bridge excitation EXHI, EXLO (checked by monitoring voltages of INPx and INNx)
- **S1_ERR**: short of bridge excitation (between EXHI and EXLO)
- **S2x_ERR**: short of sensor outputs (INPx, INNx) to bridge excitation (EXHI, EXLO)
- **S3x_ERR**: open at sensor outputs INPx, INNx (with sensor pull-ups enabled)
- **S4x_ERR**: short circuit between INPx and INNx (special self test with pull-down at INNx)

Except of **S1_ERR** all other checks are done and to enable separately for each of the two input channels (x stands for "1" or "2").
If, for instance, the input channel INP2 and INN2 is not used, the corresponding checks have to be disabled to avoid wrong error diagnosis.

The check whether all bridge voltages are inside the specified range is done by means of a comparator circuitry. To detect open circuits at INPx or INNx the corresponding internal pull-up resistors need to be enabled by internal diagnosis logic.

Because a short circuit between INPx and INNx cannot be just detected by a comparator only, an additional self test is implemented to be activated with enable bit **S4x_EN=1**. Therefore a test signal by pull-down of input INNx is activated to check for shorts between INPx and INNx.

All checks are controlled by a special logic and are done subsequently and within a fast diagnosis interval (cycle) of t_{BIST_CYC}.
A simplified overview about the implemented checks and control signals shows Figure 6.10.6-1.

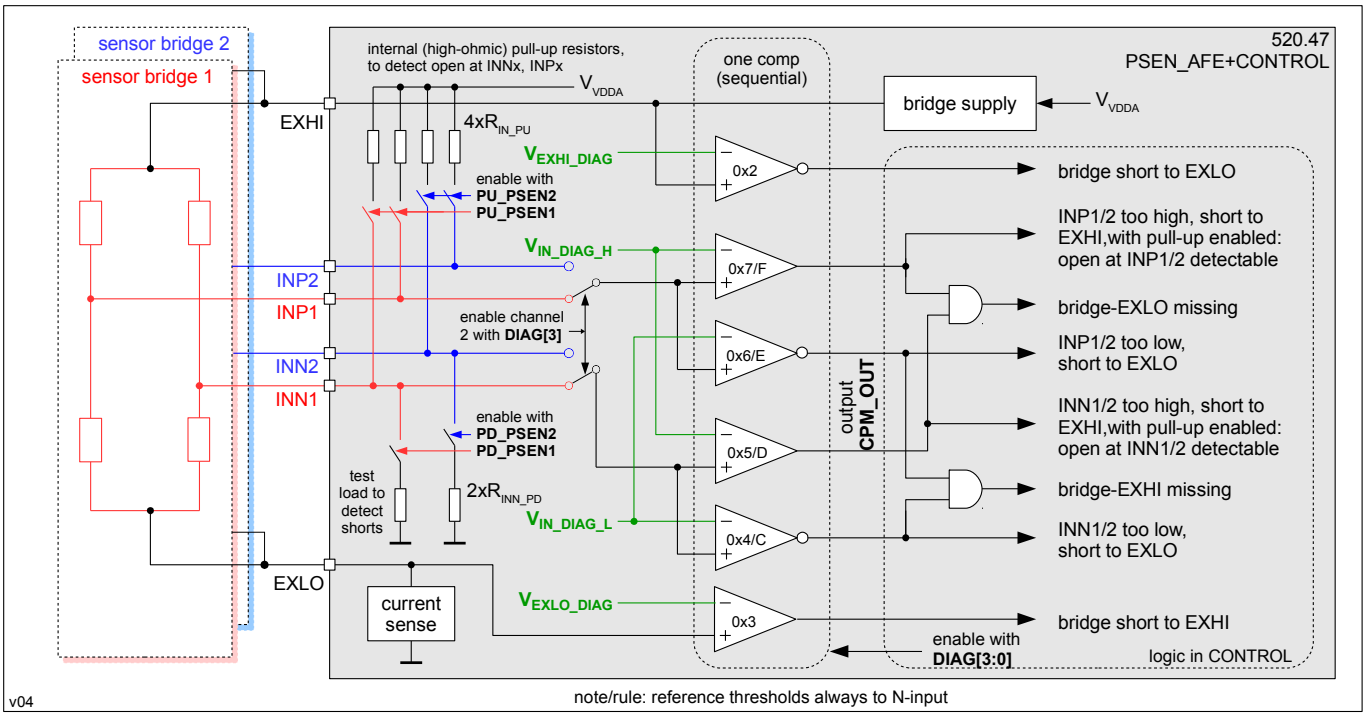


Figure 6.10.6-1: Sensor Diagnosis

An overview about possible tests and further information to the tests is listed in the table below.

Table 6.10.6-1: Sensor Bridge Diagnostic Checks

Enable Bit	Duration / Cycle	Check	DIAG Codes	Detail Result Bit	Result Error Bit

S01_EN	t_{BIST_CYC}	open detection at bridge excitation EXHI
		if (INN1EXLO .and. INP1EXLO) then open
		or
		open detection at bridge excitation EXLO
		if (INN1EXHI .and. INP1EXHI) then open
			-	-	S01_ERR

S02_EN	t_{BIST_CYC}	open detection at bridge excitation EXHI
		if (INN2EXLO .and. INP2EXLO) then open
		or
		open detection at bridge excitation EXLO
		if (INN2EXHI .and. INP2EXHI) then open
			-	-	S02_ERR

S1_EN	t_{BIST_CYC}	short detection between EXHI/LO (EXHI too low)	0x2	SHBRL	S1_ERR
S1_EN	t_{BIST_CYC}	short detection between EXHI/LO (EXLO too high)	0x3	SHBRH	S1_ERR
S21_EN	t_{BIST_CYC}	short detection between INN1 and EXLO	0x4	INN1EXLO	S21_ERR
S21_EN	t_{BIST_CYC}	short detection between INN1 and EXHI	0x5	INN1EXHI	S21_ERR
S21_EN	t_{BIST_CYC}	short detection between INP1 and EXLO	0x6	INP1EXLO	S21_ERR
S21_EN	t_{BIST_CYC}	short detection between INP1 and EXHI	0x7	INP1EXHI	S21_ERR
S22_EN	t_{BIST_CYC}	short detection between INN2 and EXLO	0xC	INN2EXLO	S22_ERR
S22_EN	t_{BIST_CYC}	short detection between INN2 and EXHI	0xD	INN2EXHI	S22_ERR
S22_EN	t_{BIST_CYC}	short detection between INP2 and EXLO	0xE	INP2EXLO	S22_ERR
S22_EN	t_{BIST_CYC}	short detection between INP2 and EXHI	0xF	INP2EXHI	S22_ERR
S31_EN	t_{BIST_CYC}	open detection at sensor input INN1	1) 0x5	OPINN1	S31_ERR
S31_EN	t_{BIST_CYC}	open detection at sensor input INP1	1) 0x7	OPINP1	S31_ERR
S32_EN	t_{BIST_CYC}	open detection at sensor input INN2	1) 0xD	OPINN2	S32_ERR
S32_EN	t_{BIST_CYC}	open detection at sensor input INP2	1) 0xF	OPINP2	S32_ERR
S41_EN	t_{BIST_CYC}	short detection between INN1 and INP1 (pressure sensor input BIST)	2) 0x6, 0x4	-	S41_ERR
S42_EN	t_{BIST_CYC}	short detection between INN2 and INP2 (pressure sensor input BIST)	2) 0xE, 0xC	-	S42_ERR

1) For this check additionally set: PU_PSEN=1
2) For this check additionally set: PD_PSEN=1

Two special register control and manage diagnostic functions. Both can be read out in configuration or diagnostic mode:

Table 6.10.6-2: Register Table DIAG_RES

Register Name	Address	Description
DIAG_RES1	0x70	diagnosis result register for bridge 1
DIAG_RES2	0x71	diagnosis result register for bridge 2

Table 6.10.6-3: Register **DIAG_RES1** (0x70) diagnosis result register for bridge 1

	MSB							***LSB***
Content	OPINP1	OPINN1	SHBRL	SHBRH	INP1EXHI	INP1EXLO	INN1EXHI	INN1EXLO
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**OPINP1** : sensor open at pin INP1 **OPINN1** : sensor open at pin INN1 **SHBRL** : sensor bridge short, EXHI too low **SHBRH** : sensor bridge short, EXLO too high **INP1EXHI** : sensor INP1 short to EXHI or high voltage note: if (INP1EXHI=1 .and. INN1EXHI=1) then "sensor open at pin EXLO" **INP1EXLO** : sensor INP1 short to EXLO or low voltage note: if (INP1EXLO=1 .and. INN1EXLO=1) then "sensor open at pin EXHI" **INN1EXHI** : sensor INN1 short to EXHI or high voltage **INN1EXLO** : sensor INN1 short to EXLO or low voltage							

Table 6.10.6-4: Register **DIAG_RES2** (0x71) diagnosis result register for bridge 2

	MSB							***LSB***
Content	OPINP2	OPINN2	-	-	INP2EXHI	INP2EXLO	INN2EXHI	INN2EXLO
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**OPINP2** : sensor open at pin INP **OPINN2** : sensor open at pin INN **INP2EXHI** : sensor INP2 short to EXHI or high voltage note: if (INP2EXHI=1 .and. INN2EXHI=1) then "sensor open at pin EXLO" **INP2EXLO** : sensor IN2P short to EXLO or low voltage note: if (INP2EXLO=1 .and. INN2EXLO=1) then "sensor open at pin EXHI" **INN2EXHI** : sensor INN2 short to EXHI or high voltage **INN2EXLO** : sensor INN2 short to EXLO or low voltage							

6.10.7 NTC Sensor Diagnosis - SM22, SM23

The chip provides check of open connection and plausible input signals for the NTC sensor connected at pin TSEN2 to the device.
But these checks can be likely used for other sensors potentially connected to this pin too.

Following diagnosis mechanisms are implemented:

- **NOP_ERR**: open at pin TSEN2 (by impedance check) Note: Do not enable with NOP_EN=1 if physical temperature sensor at TSEN2 is mapped to logical temperature channel T1. Check would disturb T1 measurement.
- **RT1_ERR, RT2_ERR**: input range check for logical temperature channel 1 or 2 (check if input TSEN2 is close to the TADC rails to detect for example shorts to VSSA and VDDA or extreme signals caused by an open R_{NTC} or R_{OP})

The tests are to enable with bits **NOP_EN** and **RT1_EN** or **RT2_EN** in ERR_ENx registers.
The diagnosis NOP_EN shall be disabled if input TSEN2 is not used to avoid wrong diagnosis errors.
The limits for RT1 or RT2 check are flexible definable in NVM words RT1_LIM or RT2_LIM. For applications with NTC sensor as example see setting and corresponding limits defined in V_{NTC_MIN} and V_{NTC_MAX}.

Example for calculation of RTx_LIM setting:

Goal: Diode voltage at channel T1 shall be checked against about 100mV as "short limit"
Setting: TGAIN=1 (diode range; full scale $V_{FS} = V_{VDDA}/3 = 4V/3 = 1.333V$)

Calculation of minimum limit:
V_{MIN} / V_{FS} = RT1_LIM[7:0] / 256 ==> **RT1_LIM[7:0] = V_{MIN} / V_{FS} * 256 = 19 = 0x13**

The open check is done by comparison of impedances at TSEN2 pin to internal references R_{TSEN2_PU} and R_{TSEN2_PD} by means of a comparator circuitry. To detect open circuit at TSEN2 the internal pull-up and pull-down resistors and certain diagnostic modes need to be enabled.

All checks are controlled by a special logic and are done subsequently.
A simplified overview about the implemented checks and control signals shows following figure.

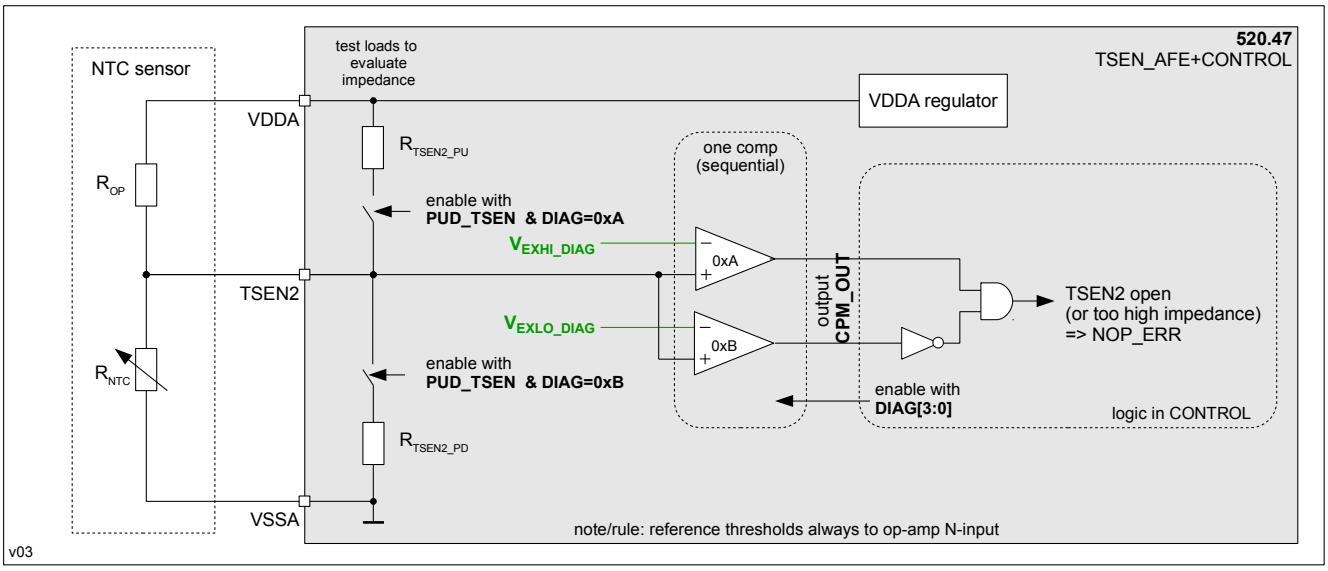


Figure 6.10.7-1: NTC Sensor Diagnosis

An overview about possible tests and further information to the tests is listed in the table below.
Note: Here the same V_{VDDA} related thresholds V_{EXHI_DIAG} and V_{EXLO_DIAG} are used as for sensor bridge diagnosis.

Table 6.10.7-1: NTC Sensor Diagnostic Checks at pin TSEN2

Enable Bit	*Duration / Cycle*	*Check*	*DIAG Codes*	*Result Error Bit*
NOP_EN	t_{BIST_CYC}	open detection at sensor input TSEN2: • check, if TSEN2 can be pulled above V_{EXHI_DIAG} • check, if TSEN2 can be pulled below V_{EXLO_DIAG}	0xA 0xB	NOP_ERR
RT1_EN or RT2_EN	t_{BIST_CYC}	input signal range check at sensor input TSEN2: • check, if TSEN2 < V_{NTC_MIN}=f(RTx_LIM) ==> signal too low • check, if TSEN2 > V_{NTC_MAX}=f(RTx_LIM) ==> signal too high **Note**: Check is based on ADC values, so real voltage thresholds depend on selected full scale range of TADC.	-	RT1_ERR or RT2_ERR

6.10.8 Diode Sensor Diagnosis - SM24

Diode Range Check

If internal and/or external diode sensor is used for logical channels T1 or T2, then a diode short and open test will be performed.

if ((V_{DIO} < V_{DIO_SHORT}) or (V_{DIO} > V_{DIO_OPEN})) then {
"diode shorted or open" => no valid sensor temperature ==> **DT1_ERR**=1 or **DT2_ERR**=1
diagnostic error code and derived potential FC value error coding see 6.6.1.4-1)
}

The thresholds for V_{DIO_SHORT} and V_{DIO_OPEN} are flexible definable in NVW words RT1_LIM and RT2_LIM. Therefore RTx_LIM[15:8] contain the upper 8 bits of TADC result vector as maximum limit, whereas RTx_LIM[7:0] contain the upper 8 bits of TADC result as minimum limit.

An overview about possible tests and further information to the tests is listed in the table below.

Table 6.10.8-1: Diode Sensor Diagnostic Check

Enable Bit	*Duration / Cycle*	*Check*	*Condition*	*Result Error Bit*
RT1_EN	t_{T_BIST}	short and open detection at internal or external sensor diode at channel 1: • error, if diode voltage drop < V_{DIO_SHORT}=f(RT1_LIM[7:0]) • error, if diode voltage drop > V_{DIO_OPEN}=f(RT1_LIM[15:8])	TCHAN1=0 or 1 TGAIN1=0 or 1	RT1_ERR
RT2_EN	t_{T_BIST}	ditto for diode sensor at temperature channel 2 (if applicable)	TCHAN2=0 or 1 TGAIN2=0 or 1	RT2_ERR

6.10.9 Chip Overtemperature Check - SM25

Independent from selected temperature channel there will be performed an additional chip temperature measurement to detect and avoid IC running at too high temperature. In case of chip temperature >T_{OT_ERR} corresponding error codes on SENT FC and SC will be transmitted.
Further information to the tests is listed in the table below.

Table 6.10.9-1: IC Overtemperature Check

Enable Bit	*Duration / Cycle*	*Check*	*Condition*	*Result Error Bit*
OT_EN	t_{T_BIST}	chip overtemperature detection with means of internal sensor diode: • error, if T_{junc} > T_{OT_ERR}	none	OT_ERR

6.10.10 Pressure Signal Path BIST - SM31

The pressure signal path BIST can be enabled with NVM bits **PSP1_EN** and **PSP2_EN**. If **PSPx_EN=1** the check of corresponding p channel runs once after power-up. If check is enabled and finished, the info result bits **PSPx_ERR** are set. If an error occurred, the result bit **PSPx_ERR** is set to 1.

During the test the path to the sensor bridge is opened and an internal generated differential signal is applied individually to PADC1 or PADC2 input instead.
The BIST has the following features and parameters:

- the BIST is performed with the same setting for gain and offset as used within the application for each channel separately selectable
- the internal input signal DAC generates individual differential voltages stored in 16 bit NVM register PSP_DAC (one 8 bit value for each channel)
- individual minimum and maximum test limits for each channel stored in NVM registers PSP1_LIM and PSP2_LIM (always the 8 most significant bits of PADC result)

Suited test limits are generated during calibration process when the necessary gain and offset settings and caused by that the fitting PSP_DAC values are fixed. This will be supported by Elmos calibration software.

6.10.11 Pressure Digital Calculation BIST - SM32

The pressure digital calculation path BIST can be enabled with NVM bits **PC1_EN** and **PC2_EN**.
If this check is enabled, it runs cyclically once within t_{BIST_CYC} and during the start-up sequence. If an error occurred, the result bit **PC1_ERR** or **PC2_ERR** is set to 1.
The pressure calculations are performed using PNUM1_ADC or PNUM2_ADC from NVM instead of true PADC values. The expected results are PNUM1_OUT or PNUM2_OUT from NVM.
There are no test limits. The calculated and the expected results have to be exactly the same.

The temperature dependent coefficients are calculated by the temperature digital calculation BIST even if this BIST is disabled (TC1_EN = 0).

6.10.12 Temperature Signal Path BIST - SM33

The temperature signal path BIST can be enabled with NVM bit **TSP_EN**. If **TSP_EN=1** the check runs cyclically once within t_{T_BIST} and during start-up sequence. If an error occurred, the result bit **TSP_ERR** is set to 1.

During the test the path to the temperature sensor connection is opened and an internal generated signal is applied to TADC instead. This mode can be activated by internal bit TBIST.
The BIST has the following features and parameters:

- the BIST is performed with the same setting for gain as used within the application for logical temperature channel T1 used for sensor linearization
- the internal BIST hardware generates differential input voltages suited to the selected TADC gain setting
- individual minimum and maximum test limits for each channel stored in NVM registers TSP_LIM (the 8 most significant bits of TADC result only)

Suited test limits are generated during calibration process when the necessary gain setting is fixed. This will be supported by Elmos calibration software.

The subsequent table shows the mapping between selected gain TGAIN1 and suited TBIST test limits to store in NVM register TSP_LIM.

Table 6.10.12-1: TSP_LIM Test Limits Depending on TGAIN1 Setting

TGAIN1[1:0]	*Minimum Limit in LSB*	*Expected Typical Value in LSB*	*Maximum Limit in LSB*	*TSP_LIM Value for NVM*
0, 1	97 (0x61)	104 (13/32=40.625%)	111 (0x6F)	0x6F61
2	49 (0x31)	56 (7/32=21.875%)	63 (0x3F)	0x3F31
3	121 (0x79)	128 (1/2=50.0%)	135 (0x87)	0x8779

6.10.13 Temperature Digital Calculation BIST - SM34

The temperature signal path BIST can be enabled with NVM bit **TC1_EN**. If **TC1_EN=1** the check runs cyclically once within t_{T_BIST} and during start-up sequence. If an error occurred, the result bit **TC1_ERR** is set to 1.

The temperature calculations are performed using TNUM1_ADC from NVM instead of the true TADC value. The temperature dependent coefficients are calculated for P1 and P2 even is the TC1 check is disabled.

The expected result is TNUM1_OUT from NVM. This is checked only if the TC1 BIST is enabled.
There are no test limits. The calculated and the expected result has to be exactly the same.

6.10.14 Memory BIST and Protection Measures

6.10.14.1 RAM BIST - SM41, SM42

To check the function of RAM memory there are following BISTs implemented:

- **RAM_CHCK**: complete RAM block check which runs once is the IC start-up sequence
- **RAM_PAR**: continuously running parity check for every RAM cell

Both checks would cause an IC reset in case of error.
A further safe operation would be no longer possible.

6.10.14.2 NVM BIST and Protection Measures - SM43, SM47, SM48, SM49

To check the function of NVM **configuration** memory there are following BISTs and protection measures are implemented:

- **NVM_CRC**: for each three separate memory blocks a 16 bit CRC is calculated once within t_{BIST_CYC} and compared with stored CRC
- **NVM_KEY**: any NVM write needs a special key to unlock the hardware
- **NVM_COR**: there is an inherent redundancy in each NVM storage cell to increase reliability of storage
- **PRG_CHCK**: there is a programming depth check within SIO write command to ensure deep programming after write

The CRC check causes a reset in error case, all other measures are protection measures only.

Detailed Description

For the algorithm how to calculate the CRC checksum see 6.8.1-1.

For the check of programming depth (PRG_CHCK) it is necessary, that the acknowledge information of SIO write command is received and interpreted. A write operation without valid ACK information might be not correct programmed.

6.10.14.3 ROM BIST and Protection Measures - SM44, SM46

To check the function of ROM(OTP) memory there are following BISTs implemented:

- **ROM_CRC**: a 16 bit CRC is calculated once within t_{ROM_BIST} and compared with stored CRC
- **ROM_ECC**: in every cell redundant data for an *error correcting code* is stored to correct 1-bit errors and to detect 2-bit errors

A CRC error or a non correctable ECC error would cause an IC reset.
A further safe operation would be no longer possible.

6.10.14.4 Register BIST - SM45, SM50

To check the function of registers there are following BISTs implemented:

- **REG_PAR**: continuously running parity check for output registers
- **REG_UPD**: there is a cyclically update of certain setting registers with values from NVM storage

The register parity check would cause an IC reset in case of error.
A further safe operation would be no longer possible.

6.10.15 Sensor Saturation Check - SM51, SM52

The saturation check insures that the calculation output value get invalid (error code) in case of numerical or ADC overflow or underflow.
Potential errors are indicated via error bits **T1_SAT**, **T2_SAT**, **P1_SAT** and **P2_SAT**. In that case the corresponding FC value gets 1 or 4088 depending on the direction of overflow. If not clear if over- or underflow the result will be 4090.

There are additional enable bits **T1SAT_EN**, **T2SAT_EN**, **P1SAT_EN** and **P2SAT_EN** to disable the error indication in SC DEC value for unused channels.

6.10.16 Temperature Voter (TV) - SM61

To improve functional safety in case of failure it is possible to use two temperature sensors for pressure sensor temperature measurement and to compare both results with a temperature voter (TV).
The voting is performed after each new $T1_{SENT}$ calculation from new measurement and before this value is used for next bridge compensation calculation.

To enable this, the bit **TV_EN** in register ERR_EN1 has to be set.

In this case the temperature channel T1 (diode or bridge current) gives the sensor temperature and the second temperature channel T2 gives a redundant temperature which is compared to T1.
Then the difference T2 - T1 is compared against TV_MIN and TV_MAX.
All values are interpreted as signed (SENT units) here.

Differences of

$$2 * TV\_MIN <= T2_{SENT} - T1_{SENT} <= 2 * TV\_MAX$$

are assumed as valid.

TV_MIN and TV_MAX, 8 bit each, are stored in two's complement code each with a range -128...127 in the NVM in register TV_LIM.
To fit into 8 bits and extend the possible temperature range the stored values TV_MIN and TV_MAX are multiplied by 2. This means that one LSB of the NVM values TV_MIN and TV_MAX corresponds to 2 SENT units (nominally 2*1/8K = 0.25 K).

If the temperature difference is detected as invalid the following actions are done:
- error bit **TV_ERR** in ERRC1 is set to 1 to indicate error
- temperatures T1 is set to error code 4090 (but T2 stays as it was measured)
- as consequence no pressure calculation is possible in this case, pressures P1 and P2 are set to 4090 too

Example:
Is it is allowed for T2 to be 2 K less than T1 or 6 K greater than T1, then

$$-2\ K <= T2 - T1 <= 6\ K$$

is valid.
Transformed to SENT units this means

$$-16 <= T2\_SENT - T1\_SENT <= 48$$

In the NVM the values TV_MIN = -8 and TV_MAX = 24 have to be stored. Negative values are stored in two's complement, for TV_MIN this is 256 - 8 = 248.

This means
TV_MIN = 248 = 0xF8
TV_MAX = 24 = 0x18. ==> to store 0x18F8 into NVM cell TV_LIM

6.10.17 Pressure Voter (PV) - SM62

To improve functional safety in case of failure it is possible to use two pressure sensor channels and to compare both results with a pressure voter (PV).
To enable this check, the bit **PV_EN** in register ERR_EN1 has to be set.
In this case the absolute value of the difference of the pressures in SENT units is compared to PV_LIM (stored in NVM).

Differences of

$|P1_{SENT} - P2_{SENT}| <= PV\_LIM$

are assumed as valid.

PV_LIM is stored as unsigned integer 16 bit value. Because SENT value range is 12 bits only, every test limit is possible.

If the pressure value difference is detected as invalid the following actions are done:
- error bit **PV_ERR** in ERRC1 is set to 1 to indicate error
- both compared pressures P1 and P2 are set to error code 4090

Calculation Example:
It shall be checked, if both pressure channels diverge more then 5% of SENT full scale.
So in SENT units 5%*4095 LSB_{SENT} = 204 LSB_{SENT}.
This value has to be stored as unsigned integer value in NVM cell PV_LIM for following voter check:

$|P1_{SENT} - P2_{SENT}| <= 204$

This means
PV_LIM = 204 = 0x00cc. ==> to store 0x00cc into NVM cell PV_LIM

6.10.18 Processing Engine Check - SM63, SM64

As built in self test for processing engine used in block CORRECT and CONTROL following checks are implemented:

- **DPU_CHK**: Check of critical instructions like LPM and instruction sequences like carry propagation with a special test code. Processing errors lead to an IC reset. The check is repeated once per cycle t_{BIST_CYC}.
- **ILL_OPC**: An illegal opcode in processing machine immediately leads to an IC reset.

6.10.19 SENT Interface Check - SM91, SM92

SENT Interface Check - IF_CHCK

The definition of SENT protocol itself contains certain safety measures. To get these measures active on **system level** several tasks are to do. For the highest level of safety we recommend following the following actions on system level:

- Check if transmitted CRC fits to the protocol data.
- Use P/S mode of SENT protocol. Check if redundant transmitted most significant nibbles of pressure are consistent. Check if counter increases regularly and reaches end value before wrapping to start value.
- Check if sync pulse length is plausible. Refuse protocols where this length is out of SENT specification.

SENT Interface Check - IF_CHCK2

The definition of SENT protocol itself contains certain safety measures. To get these measures active on **system level** several tasks are to do. For the highest level of safety we recommend following the following actions on system level:

- Check if FC data are 1, 4088 or 4090 if corresponding status error bit is set and vice versa.

6.10.20 SENT Watchdog (SENT_WD) - SM93

The digital SENT interface SENT_DIG gets regularly updated FC data from the CORRECT block. If due to an internal hardware error this update is interrupted, the SENT interface might transmit further the outdated (or overaged) data without notice.
To avoid this, the interface contains a watchdog called SENT_WD, which stops the SENT interface after 4 sent protocols without update from the CORRECT bock.

7 Package Reference

7.1 Package QFN20L4

The 520.47 is available in a Pb free, RoHs compliant, QFN20L4 plastic package according to JEDEC MO-220K, VGGD-5. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020E with a soldering peak temperature of 260°C.

Note:
Thermal resistance junction to ambient $R_{th,ja}$ is 45 °C/W, based on JEDEC standard JESD-51-5 and JESD-51-7.

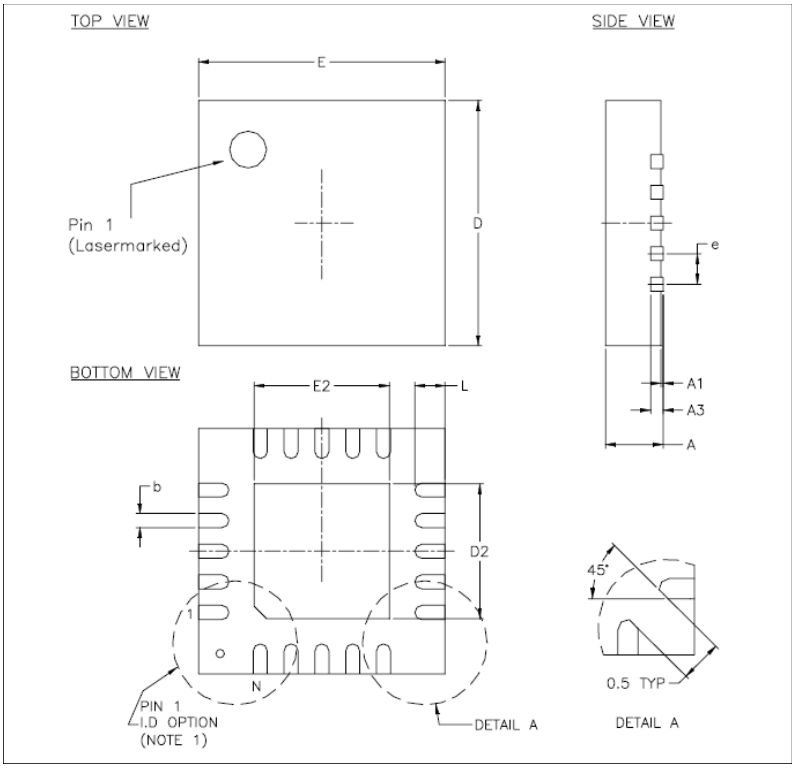


Figure 7.1-1: Package Outline

Note: Contact factory for specific location and type of pin 1 identification.

Table 7.1-1: Package Characteristics

Description	*Symbol*		*mm*			*inch*	
		min	**typ**	**max**	**min**	**typ**	**max**
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.0008	0.002
Thickness of terminal leads, including lead finish	A3		0.20			0.0079	
Width of terminal leads	b	0.18	0.25	0.30	0.0071	0.0098	0.0120
Package length / width	D / E		4.0			0.157	
Length /width of exposed pad	D2 / E2	2.50	2.65	2.80	0.098	0.104	0.110
Lead pitch	e		0.50			0.02	
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		20			20	

Note: Dimensions in mm are valid; the inch values may contain rounding errors

7.2 Bare Die

Dice are delivered as wafers on foil. Sample volumes may be packed in waffle packs.
Wafer thickness after grinding: 400 µm ± 30 µm

Note: Contact factory for detail information on pad-layout E520.47.

8 Typical Applications

The E520.47 can be used to process various resistive bridge inputs. It is designed primarily for piezo-resistive pressure cells. Here, single and double bridge inputs can be processed independently or related to each other for redundancy and mutual supervision of their corresponding outputs for improved functional safety making use of sensor redundancy. Also up to two independent temperature sensors can be connected for redundancy of temperature data acquired or to incorporate independent media temperature measurements.
A typical application circuit is depicted below in 8-1 with two resistive bridges connected to the differential input pairs INP1/INN1 and INP2 /INN2 and an external NTC as media temperature sensor. Here, it is assumed the temperature correction of the pressure bridges is performed by temperature sensing of the internal temperature sensor inside E520.47 or the bridge current sensing method (see chapter 6.4). As an alternative to acquire the bridge-temperature a discrete diode D_{TSEN1} connected between pins EXHI and TSEN1 (cathode) can be used. For plausibility check of the bridge temperature measurement also the NTC measurement connected at pin TSEN2 can be used, if the temperature at the NTC is closely related to the bridge temperature.
The application example below also suggests coupling components of the SENT data interface at the IC output for regular SENT pulse forming and usual buffer and filtering components at the supply input VS and the internal regulator pin VDDA.

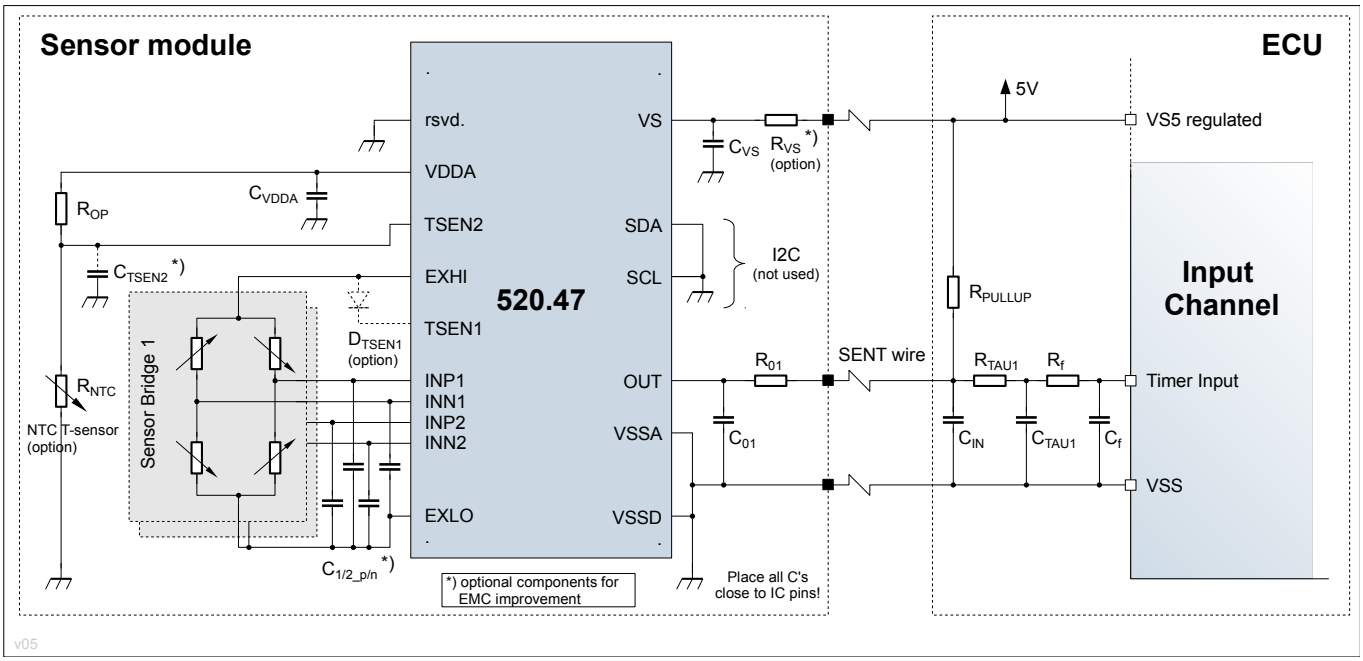


Figure 8-1: Typical Application Circuit - E520.47 with Pressure Bridge and NTC Sensor

Table 8-1: Recommended component values

Description	Symbol	Min	Typ	Max	Unit
Supply buffer capacitor	C_{VS}	80	100	250	nF
Supply series resistance [1]	R_{VS}	0	-	20	Ω
Bypass capacitor at VDDA (internal regulator)	C_{VDDA}	80	100	120	nF
Bridge resistance [2]	R_{BR}	1	-	12	kΩ
Capacitor at sensor cell inputs INP1, INN1, INP2, INN2 [3]	$C_{1\_p/n}$ $C_{2\_P/n}$	0	-	130	pF
NTC resistance, value at room temperature	$R_{NTC,25C}$	2	-	10	kΩ
Operating pull-up resistance of NTC divider [4]	R_{OP}	0.5	1.0	1.2	$R_{NTC,25C}$

Description	Symbol	Min	Typ	Max	Unit
Filter capacitor of NTC divider [5]	C_{TSEN2}	0	4.7	13	nF
SENT transmitter EMI filter capacitor	C_{01}	1.54	2.2	2.86	nF
SENT transmitter EMI filter resistor	R_{01}	90	100	110	Ω

[1] A series resistor at the supply input can be used for additional EMI susceptibility of the device. In any case, the DC voltage drop shall be less than 100 mV to avoid unintended low-voltage indication.

[2] The resistance of the bridge cell(s) connected to EXHI, EXLO shall not decrease below the minimum given to avoid over-current limitation of the voltage excitation driver. Furthermore, the maximum impedance at neither bridge input shall not be exceeded to avoid triggering of the *Sensor Open Test* if enabled.

[3] Wiring of the resistive sensor bridge to the IC inputs should be as short as possible and symmetrical (for corresponding differential inputs) to avoid coupling of electrical disturbances into the sensitive input(s). Depending on the board layout, these unwanted coupling may be suppressed further by adding capacitors to INPx, INNx, respectively. Maximum value must not be exceeded to ensure the *Sensor Open Test* as part of the *Bridge Sensor Diagnosis* (s. 6.10.6).

[4] The pull-up resistor of the NTC divider shall be selected to get 50% voltage near the middle of the temperature range for optimum accuracy here. Also self-heating of the NTC should be considered. See chapter 6.5.4 for more details on NTC linearization.

[5] For optimized EMI susceptibility an additional filter capacitance C_{TSEN2} may be necessary. Especially, in that case the input current drawn I_{TSEN2_IN} by the ADC input plus leakage has to be considered for calculation of T-accuracy. Leakage currents are most critical at high impedance, which is maximum for the NTC at lowest temperatures .

9 Glossary

Table 9-1: Glossary

Abbreviation	*Description*
ADC	analogue to digital converter
ACK	acknowledge
AFE	analogue front-end
BIST	built in self test
CCP	common command processor (processes SIO and I2C commands)
CRC	cyclic redundancy check
DEC	diagnostic error code (SENT protocol)
_DIG	digital part of block
DPU	digital processing unit
ESD	electrostatic discharge
FC	fast channel (of SENT interface)
I2C	inter-integrated circuit (two wire bus interface)
LPF	low pass filter
NTC	negative temperature coefficient thermistor
NVM	non-volatile memory
OSC	oscillator
OTP	one time programmable (memory)
OV	overvoltage
PADC	ADC for pressure values
TADC	ADC for temperature values
SC	slow channel (of SENT interface)
SCL / SDA	serial clock line / serial data line
SENT	single edge nibble transmission (sensor interface protocol defined by SAE International)
SFR	special function register(s)
SIO	serial input/output (serial interface with only one wire)
SM	safety measures
SNR	signal-to-noise ratio
SSP	sensor signal processor
UV	undervoltage
WD	watchdog

10 General

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11 Contact Info

Table 11-1: Contact Information

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