

54ABT16374

16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The ABT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (\overline{OE}) are common to each byte and can be shorted together for full 16-bit operation.

Features

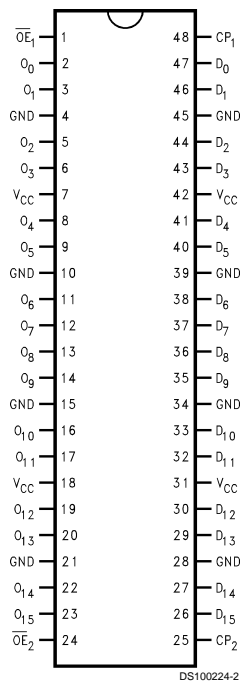
- Separate control logic for each byte
- 16-bit version of the ABT374
- Edge-triggered D-type inputs
- Buffered Positive edge-triggered clock
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection
- Standard Microcircuit Drawing (SMD) 5962-9320101

Ordering Code:

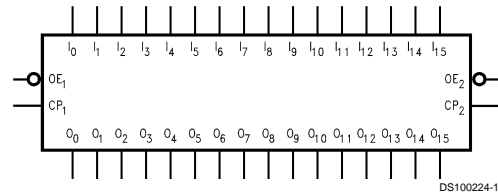
Commercial	Package Number	Package Description
54ABT16374W-QML	WA48A	48-Lead Cerpack

Connection Diagram

Pin Assignment for Cerpack



Logic Symbol



Pin Description

Pin Names	Description
\overline{OE}_n	TRI-STATE Output Enable Input (Active Low)
CP_n	Clock Pulse Input (Active Rising Edge)
D_0-D_{15}	Data Inputs
O_0-O_{15}	TRI-STATE Outputs

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Functional Description

The ABT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable (\overline{OE}_n) LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

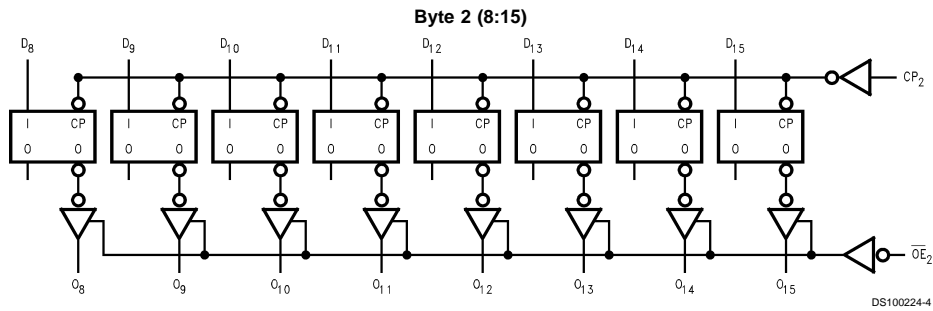
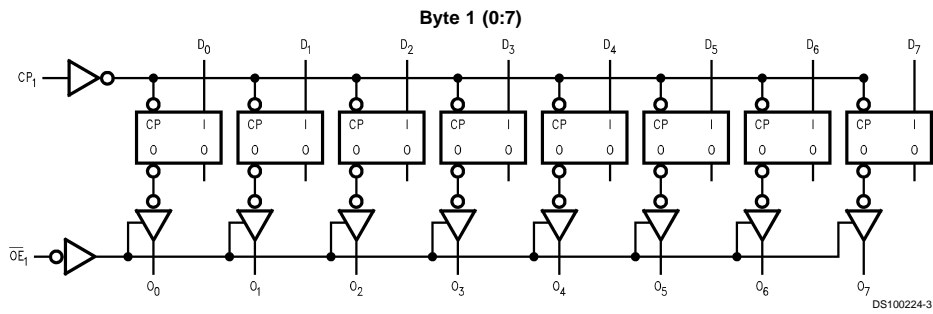
Truth Tables

Inputs			Outputs
CP_1	\overline{OE}_1	D_0-D_7	O_0-O_7
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

Inputs			Outputs
CP_2	\overline{OE}_2	D_8-D_{15}	O_8-O_{15}
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagrams



Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current:

OE Pin	-350 mA
(Across Comm Operating Range)	
Other Pins	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16374			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA
		54ABT	2.0		V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage	54ABT	0.55		V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4)
			5		μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		-5		μA	Max	V _{IN} = 0.5V (Note 4)
			-5		μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current		50		μA	0-5.5V	V _{OUT} = 2.7V; OE = 2.0V
I _{OZL}	Output Leakage Current		-50		μA	0-5.5V	V _{OUT} = 0.5V; OE = 2.0V
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Others V _{CC} or GND
I _{CCH}	Power Supply Current		2.0		mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		62		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		2.0		mA	Max	OE = V _{CC} ; All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA		V _I = V _{CC} - 2.1V
		Outputs TRI-STATE	2.5		mA	Max	Enable Input V _I = V _{CC} - 2.1V
		Outputs TRI-STATE	2.5		mA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC}	No Load		0.30	mA/ MHz	Max	Outputs Open OE = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.1	V	5.0	T _A = 25°C (Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-0.45	V	5.0	T _A = 25°C (Note 5)

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF			
		Min	Max		
f _{max}	Max Clock Frequency	150		MHz	
t _{PLH}	Propagation Delay	1.5	6.9	ns	Figure 2
t _{PZH}	CP to O _n	1.5	6.9	ns	Figure 7
t _{PZL}	Output Enable Time	0.8	6.5	ns	Figure 7
t _{PHZ}	Output Disable Time	1.5	9.6	ns	Figure 7
t _{PLZ}		1.5	7.2		

AC Operating Requirements

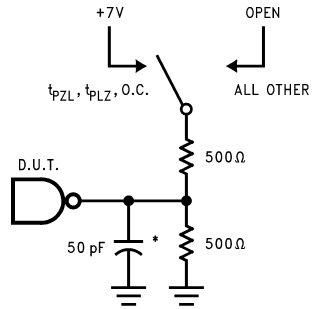
Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF			
		Min	Max		
t _s (H)	Setup Time, HIGH	1.3		ns	Figure 6
t _s (L)	or LOW D _n to CP	1.3			
t _h (H)	Hold Time, HIGH	1.5		ns	Figure 6
t _h (L)	or LOW D _n to CP	1.5			
t _w (H)	Pulse Width, CP	3.3		ns	Figure 5
t _w (L)	HIGH or LOW	3.3			

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T _A = 25°C)
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0V
C _{OUT} (Note 6)	Output Capacitance	11.0	pF	V _{CC} = 5.0V

Note 6: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

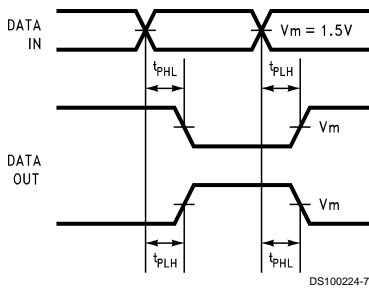


FIGURE 2. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

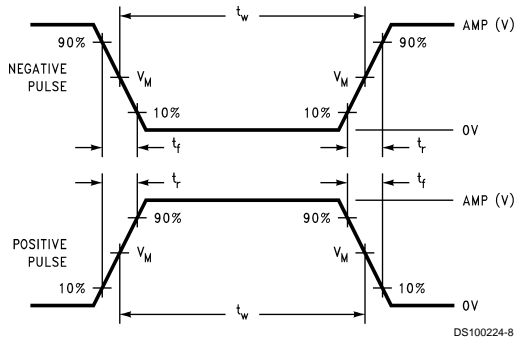


FIGURE 3. Test Input Pulse Requirements

Amplitude	Rep Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

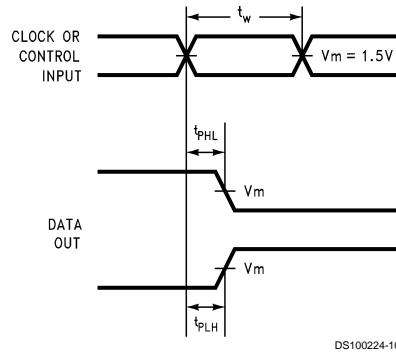


FIGURE 5. Propagation Delay, Pulse Width Waveforms

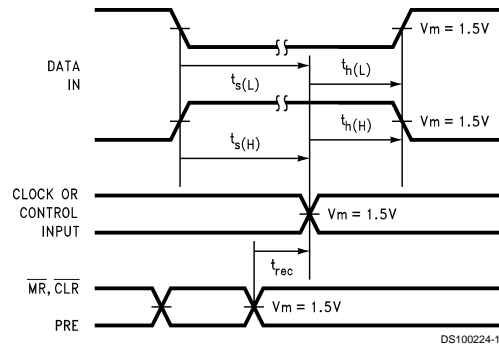


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

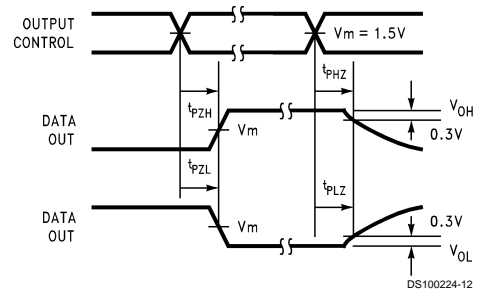
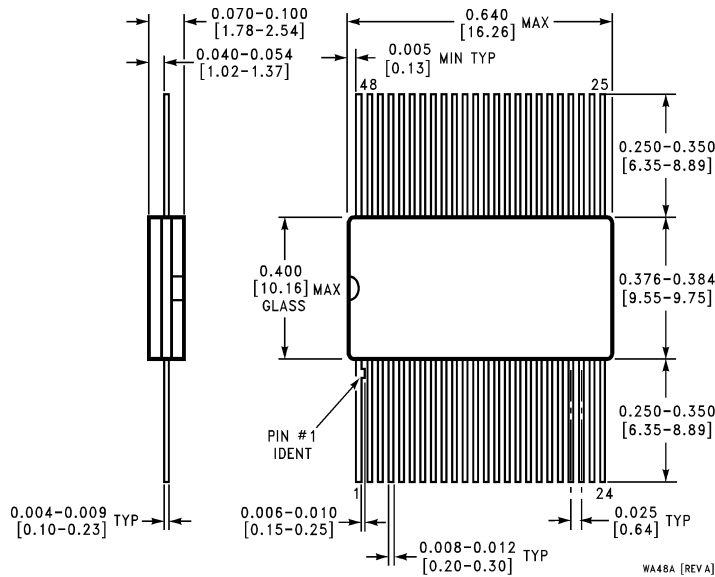


FIGURE 7. TRI-STATE Output HIGH and LOW Enable and Disable Times

Physical Dimensions inches (millimeters) unless otherwise noted




**48-Lead Cerpack
NS Package Number WA48A**

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