

# 54ABT16500

## 18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

### General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{CLKAB}$  is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{CLKAB}$ . Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, and  $\overline{CLKBA}$ . The output enables are complementary ( $\overline{OEAB}$  is active high and  $\overline{OEBA}$  is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9687001

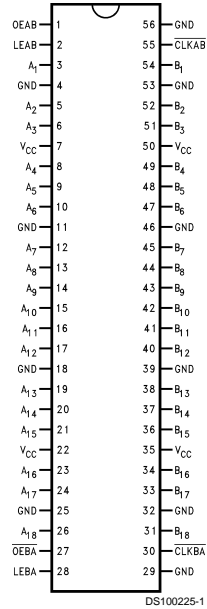
### Ordering Code

Military	Package Number	Package Description
54ABT16500W-QML	WA56A	56-Lead Cerpack

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## Connection Diagram

Pin Assignment for Cerpack



Function Table (Note 1)

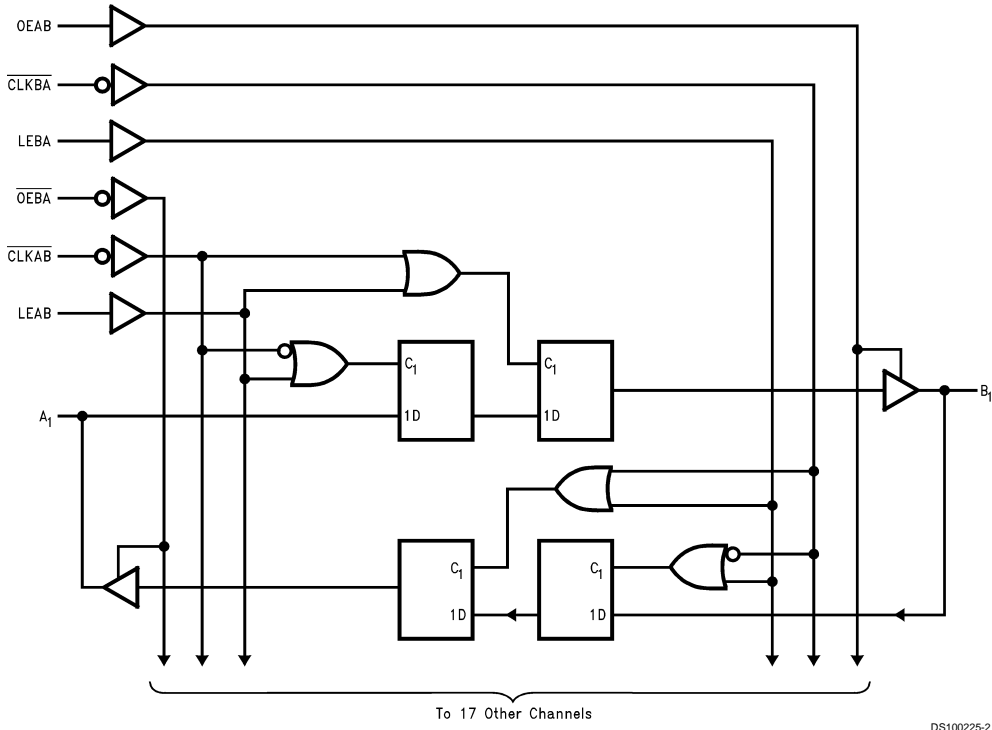
Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub> (Note 2)
H	L	L	X	B <sub>0</sub> (Note 3)

**Note 1:** A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKBA}}$ .

**Note 2:** Output level before the indicated steady-state input conditions were established.

**Note 3:** Output level before the indicated steady-state input conditions were established, provided that  $\overline{\text{CLKAB}}$  was low before LEAB went low.

### Logic Diagram



DS100225-2

## Absolute Maximum Ratings (Note 4)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 4:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 5:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	ABT16500			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Note 6)
				5			V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 6)
				-5			V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			50	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ , OE = 2.0V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-50	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ , OE = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100	-275		mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			68	μA	Max	An or Bn Outputs Low
I <sub>CCZ</sub>	Power Supply Current			1.0	mA	Max	$\overline{OE}_n = V_{CC}$ , All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input			2.5	mA	Max	V <sub>i</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 6)	No Load		0.23	mA/ MHz	Max	Outputs Open Transparent Mode One Bit Toggling, 50% Duty Cycle

**Note 6:** Guaranteed, but not tested.

## DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V <sub>CC</sub>	Conditions C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		1.1	V	5.0	T <sub>A</sub> = 25°C (Note 7)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>		-1.7	V	5.0	T <sub>A</sub> = 25°C (Note 7)

Note 7: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

## AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	150		MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A or B to B or A	1.0	6.5	ns	Figure 4
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEAB or LEBA to B or A	1.0	7.0	ns	Figure 4
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKAB or CLKBA to B or A	1.0	7.5	ns	Figure 4
t <sub>PZH</sub> t <sub>PZL</sub>	Propagation Delay OEAB or OEBA to B or A	1.0	6.3	ns	Figure 6
t <sub>PHZ</sub> t <sub>PLZ</sub>	Propagation Delay OEAB or OEBA to B or A	1.0	7.2	ns	Figure 6
t <sub>PLZ</sub>	OEAB or OEBA to B or A	1.0	6.8		

## AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, A to CLKAB	4.5	4.5	ns	Figure 7
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, A to CLKAB	0	0	ns	Figure 7
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, B to CLKBA	4.0	4.0	ns	Figure 7
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, B to CLKBA	0	0	ns	Figure 7
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, A to LEAB or B to LEBA, CLK High	1.5	1.5	ns	Figure 7
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, A to LEAB or B to LEBA, CLK High	1.5	1.5	ns	Figure 7
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, A to LEAB or B to LEBA, CLK Low	4.5	4.5	ns	Figure 7
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, A to LEAB or B to LEBA, CLK Low	1.5	1.5	ns	Figure 7
t <sub>w</sub> (H) t <sub>w</sub> (L)	Pulse Width, LEAB or LEBA, High	3.3	3.3	ns	Figure 5

### AC Operating Requirements (Continued)

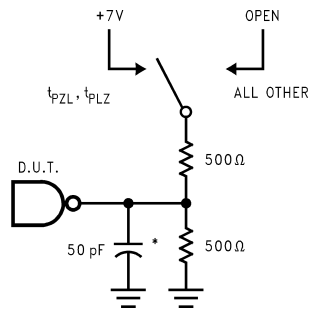
Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C			
		V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>w</sub> (H)	Pulse Width, CLKAB	3.3		ns	Figure 5
t <sub>w</sub> (L)	or CLKBA, High or Low	3.3			

### Capacitance

Symbol	Parameter	Typ	Units	Conditions, T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0.0V
C <sub>I/O</sub> (Note 8)	Output Capacitance	11.0	pF	V <sub>CC</sub> = 5.0V

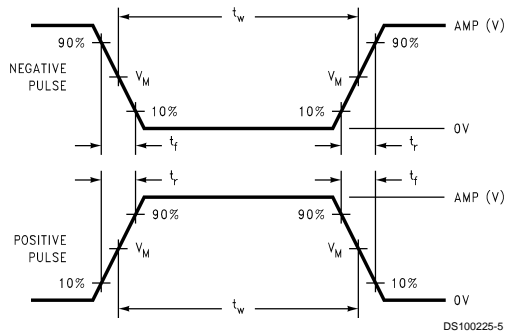
**Note 8:** C<sub>I/O</sub> is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

## AC Loading



\*Includes jig and probe capacitance.

**FIGURE 1. Standard AC Test Load**

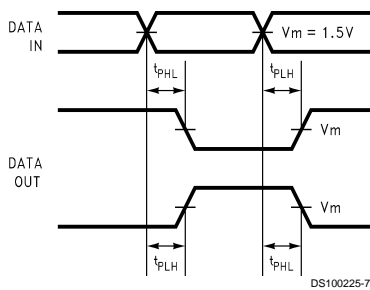


**FIGURE 2.  $V_M = 1.5V$**

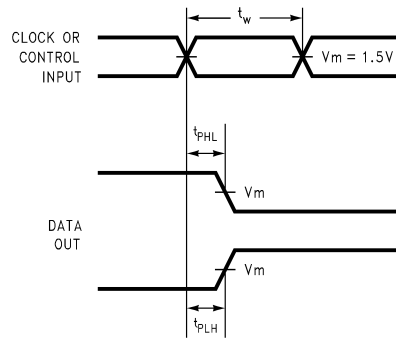
### Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

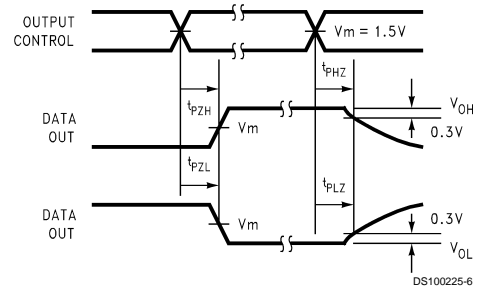
**FIGURE 3. Test Input Signal Requirements**



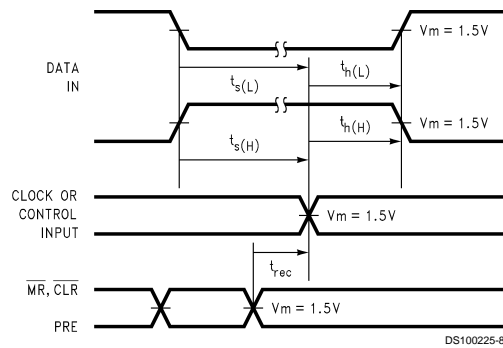
**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 5. Propagation Delay, Pulse Width Waveforms**

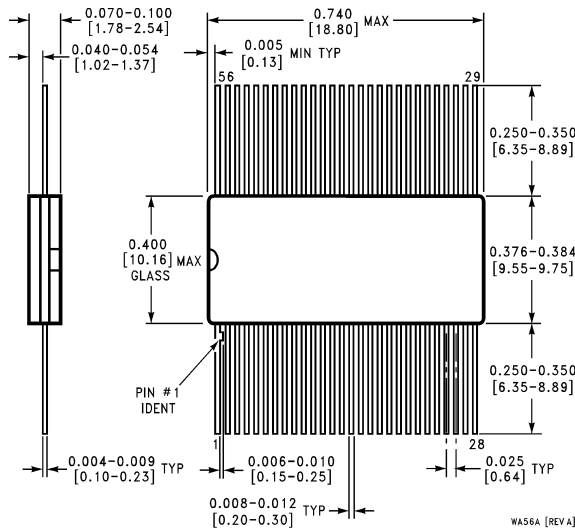


**FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times**



**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Cerpack**  
**NS Package Number WA56A**

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