

## 54ABT374

### Octal D-Type Flip-Flop with TRI-STATE® Outputs

#### General Description

The 'ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

#### Features

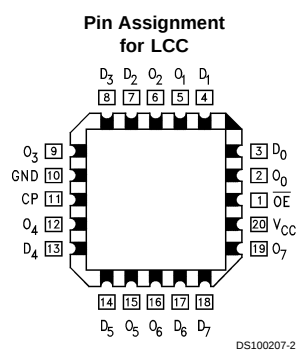
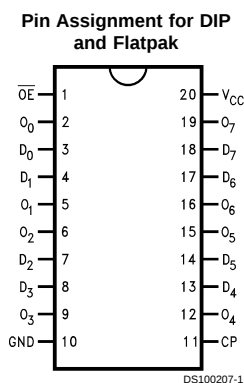
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 48 mA, source capability of 24 mA

- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9314901

#### Ordering Code

| Military      | Package Number | Package Description                           |
|---------------|----------------|-----------------------------------------------|
| 54ABT374J/883 | J20A           | 20-Lead Ceramic Dual-In-Line                  |
| 54ABT374W/883 | W20A           | 20-Lead Cerpack                               |
| 54ABT374E/883 | E20A           | 20-Lead Ceramic Leadless Chip Carrier, Type C |

#### Connection Diagrams



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Pin Descriptions

| Pin Names                      | Description                                |
|--------------------------------|--------------------------------------------|
| D <sub>0</sub> –D <sub>7</sub> | Data Inputs                                |
| CP                             | Clock Pulse Input (Active Rising Edge)     |
| $\overline{OE}$                | TRI-STATE Output Enable Input (Active LOW) |
| O <sub>0</sub> –O <sub>7</sub> | TRI-STATE Outputs                          |

## Functional Description

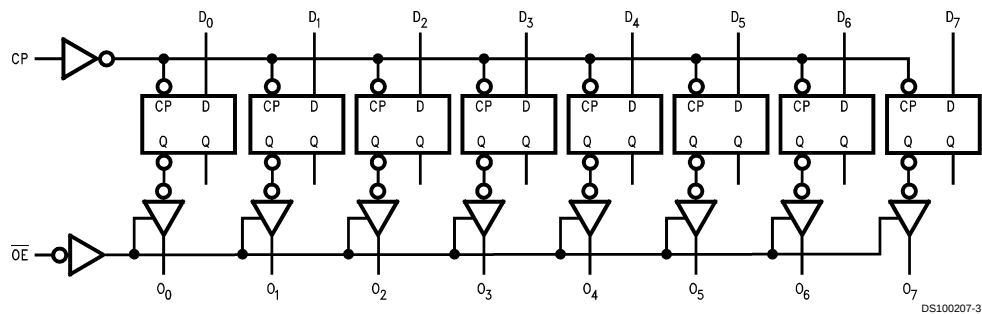
The 'ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Function Table

| Inputs          |    |   | Internal | Outputs | Function          |
|-----------------|----|---|----------|---------|-------------------|
| $\overline{OE}$ | CP | D | Q        | O       |                   |
| H               | H  | L | NC       | Z       | Hold              |
| H               | H  | H | NC       | Z       | Hold              |
| H               | ↗  | L | L        | Z       | Load              |
| H               | ↗  | H | H        | Z       | Load              |
| L               | ↗  | L | L        | L       | Data Available    |
| L               | ↗  | H | H        | H       | Data Available    |
| L               | H  | L | NC       | NC      | No Change in Data |
| L               | H  | H | NC       | NC      | No Change in Data |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

|                                                                  |                                      |
|------------------------------------------------------------------|--------------------------------------|
| Storage Temperature                                              | –65°C to +150°C                      |
| Ambient Temperature under Bias                                   | –55°C to +125°C                      |
| Junction Temperature under Bias                                  |                                      |
| Ceramic                                                          | –55°C to +175°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                      | –0.5V to +7.0V                       |
| Input Voltage (Note 2)                                           | –0.5V to +7.0V                       |
| Input Current (Note 2)                                           | –30 mA to +5.0 mA                    |
| Voltage Applied to Any Output in the Disabled or Power-Off State | –0.5V to 5.5V                        |
| in the HIGH State                                                | –0.5V to V <sub>CC</sub>             |
| Current Applied to Output in LOW State (Max)                     | twice the rated I <sub>OL</sub> (mA) |

DC Latchup Source Current:

|                               |         |
|-------------------------------|---------|
| $\overline{OE}$ Pin           | –150 mA |
| (Across Comm Operating Range) |         |
| Other Pins                    | –500 mA |
| Over Voltage Latchup (I/O)    | 10V     |

## Recommended Operating Conditions

|                              |                         |
|------------------------------|-------------------------|
| Free Air Ambient Temperature |                         |
| Military                     | –55°C to +125°C         |
| Supply Voltage               |                         |
| Military                     | +4.5V to +5.5V          |
| Minimum Input Edge Rate      | ( $\Delta V/\Delta t$ ) |
| Data Input                   | 50 mV/ns                |
| Enable Input                 | 20 mV/ns                |
| Clock Input                  | 100mV/ns                |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol            | Parameter                         | ABT374 |      |      | Units | V <sub>CC</sub> | Conditions                                                               |
|-------------------|-----------------------------------|--------|------|------|-------|-----------------|--------------------------------------------------------------------------|
|                   |                                   | Min    | Typ  | Max  |       |                 |                                                                          |
| V <sub>IH</sub>   | Input HIGH Voltage                | 2.0    |      |      | V     |                 | Recognized HIGH Signal                                                   |
| V <sub>IL</sub>   | Input LOW Voltage                 |        | 0.8  |      | V     |                 | Recognized LOW Signal                                                    |
| V <sub>CD</sub>   | Input Clamp Diode Voltage         |        | –1.2 |      | V     | Min             | I <sub>IN</sub> = –18 mA                                                 |
| V <sub>OH</sub>   | Output HIGH Voltage               | 54ABT  | 2.5  |      | V     | Min             | I <sub>OH</sub> = –3 mA                                                  |
|                   | 54ABT                             |        | 2.0  |      | V     | Min             | I <sub>OH</sub> = –24 mA                                                 |
| V <sub>OL</sub>   | Output LOW Voltage                | 54ABT  |      | 0.55 | V     | Min             | I <sub>OL</sub> = 48 mA                                                  |
| I <sub>IH</sub>   | Input HIGH Current                |        | 5    |      | μA    | Max             | V <sub>IN</sub> = 2.7V (Note 4)                                          |
|                   |                                   |        | 5    |      |       |                 | V <sub>IN</sub> = V <sub>CC</sub>                                        |
| I <sub>BVI</sub>  | Input HIGH Current Breakdown Test |        | 7    |      | μA    | Max             | V <sub>IN</sub> = 7.0V                                                   |
| I <sub>IL</sub>   | Input LOW Current                 |        | –5   |      | μA    | Max             | V <sub>IN</sub> = 0.5V (Note 4)                                          |
|                   |                                   |        | –5   |      |       |                 | V <sub>IN</sub> = 0.0V                                                   |
| V <sub>ID</sub>   | Input Leakage Test                | 4.75   |      |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                      |
| I <sub>OZH</sub>  | Output Leakage Current            |        | 50   |      | μA    | 0 – 5.5V        | V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V                          |
| I <sub>OZL</sub>  | Output Leakage Current            |        | –50  |      | μA    | 0 – 5.5V        | V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V                          |
| I <sub>OS</sub>   | Output Short-Circuit Current      | –100   | –275 |      | mA    | Max             | V <sub>OUT</sub> = 0.0V                                                  |
| I <sub>CEX</sub>  | Output High Leakage Current       |        | 50   |      | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                                       |
| I <sub>ZZ</sub>   | Bus Drainage Test                 |        | 100  |      | μA    | 0.0             | V <sub>OUT</sub> = 5.5V; All Others V <sub>CC</sub> or GND               |
| I <sub>CCH</sub>  | Power Supply Current              |        | 50   |      | μA    | Max             | All Outputs HIGH                                                         |
| I <sub>CCL</sub>  | Power Supply Current              |        | 30   |      | mA    | Max             | All Outputs LOW                                                          |
| I <sub>CCZ</sub>  | Power Supply Current              |        | 50   |      | μA    | Max             | $\overline{OE}$ = V <sub>CC</sub> ; All Others at V <sub>CC</sub> or GND |
| I <sub>CC</sub> T | Additional Outputs Enabled        |        | 2.5  |      | mA    |                 | V <sub>I</sub> = V <sub>CC</sub> – 2.1V                                  |
|                   | I <sub>CC</sub> /Input            |        |      |      |       |                 |                                                                          |
|                   | Outputs TRI-STATE                 |        | 2.5  |      | mA    | Max             | Enable Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V                     |
|                   | Outputs TRI-STATE                 |        | 2.5  |      | mA    |                 | Data Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V                       |
|                   |                                   |        |      |      |       |                 | All Others at V <sub>CC</sub> or GND                                     |

## DC Electrical Characteristics (Continued)

| Symbol           | Parameter                                   | ABT374 |      |     | Units      | V <sub>CC</sub> | Conditions                                                             |
|------------------|---------------------------------------------|--------|------|-----|------------|-----------------|------------------------------------------------------------------------|
|                  |                                             | Min    | Typ  | Max |            |                 |                                                                        |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub> No Load<br>(Note 4) |        | 0.30 |     | mA/<br>MHz | Max             | Outputs Open<br>OE = GND, (Note 3)<br>One Bit Toggling, 50% Duty Cycle |

**Note 3:** For 8-bit toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol           | Parameter            | 54ABT                                                                                        |     | Units |
|------------------|----------------------|----------------------------------------------------------------------------------------------|-----|-------|
|                  |                      | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50 pF |     |       |
|                  |                      | Min                                                                                          | Max |       |
| f <sub>max</sub> | Max Clock Frequency  | 150                                                                                          |     | MHz   |
| t <sub>PLH</sub> | Propagation Delay    | 1.4                                                                                          | 6.6 | ns    |
| t <sub>PHL</sub> | CP to O <sub>n</sub> | 2.0                                                                                          | 7.6 |       |
| t <sub>PZH</sub> | Output Enable Time   | 0.8                                                                                          | 5.7 | ns    |
| t <sub>PZL</sub> |                      | 1.5                                                                                          | 7.2 |       |
| t <sub>PHZ</sub> | Output Disable Time  | 1.3                                                                                          | 7.2 | ns    |
| t <sub>PLZ</sub> |                      | 1.0                                                                                          | 7.0 |       |

## AC Operating Requirements

| Symbol             | Parameter                   | 54ABT                            |     | Units |
|--------------------|-----------------------------|----------------------------------|-----|-------|
|                    |                             | T <sub>A</sub> = −55°C to +125°C |     |       |
|                    |                             | V <sub>CC</sub> = 4.5V to 5.5V   |     |       |
|                    |                             | C <sub>L</sub> = 50 pF           |     |       |
|                    |                             | Min                              | Max |       |
| t <sub>s</sub> (H) | Setup Time, HIGH            | 2.5                              |     | ns    |
| t <sub>s</sub> (L) | or LOW D <sub>n</sub> to CP | 2.5                              |     |       |
| t <sub>h</sub> (H) | Hold Time, HIGH             | 2.5                              |     | ns    |
| t <sub>h</sub> (L) | or LOW D <sub>n</sub> to CP | 2.5                              |     |       |
| t <sub>w</sub> (H) | Pulse Width, CP             | 3.3                              |     | ns    |
| t <sub>w</sub> (L) | HIGH or LOW                 | 3.3                              |     |       |

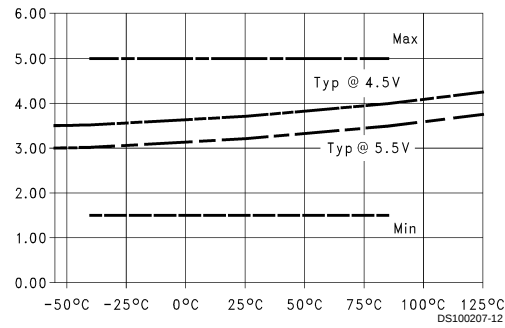
## Capacitance

| Symbol                    | Parameter          | Typ | Units | Conditions (T <sub>A</sub> = 25°C) |
|---------------------------|--------------------|-----|-------|------------------------------------|
| C <sub>IN</sub>           | Input Capacitance  | 5.0 | pF    | V <sub>CC</sub> = 0V               |
| C <sub>OUT</sub> (Note 5) | Output Capacitance | 9.0 | pF    | V <sub>CC</sub> = 5.0V             |

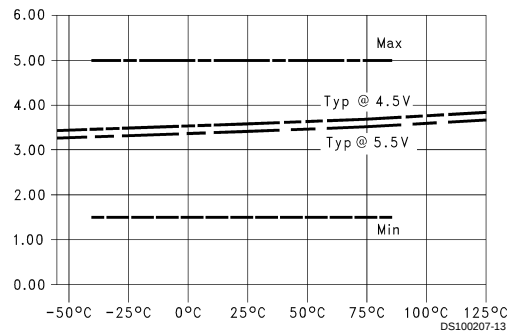
**Note 5:** C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

## Capacitance (Continued)

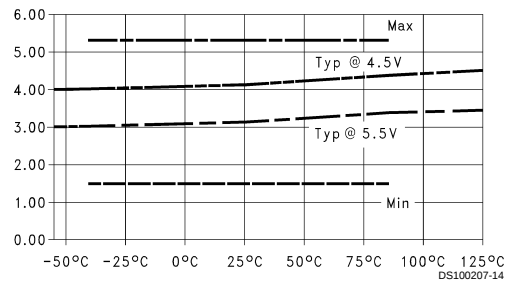
**$t_{PLH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Clock to Output**



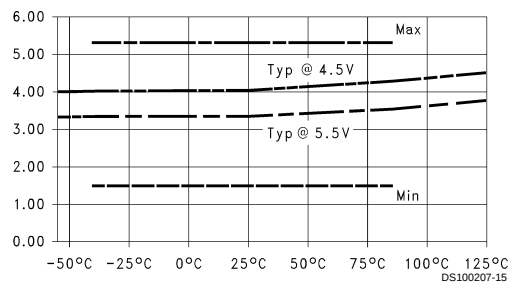
**$t_{PHL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Clock to Output**



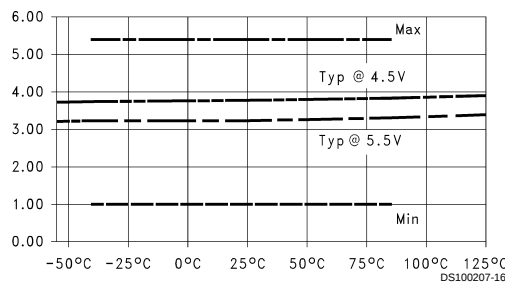
**$t_{PZH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



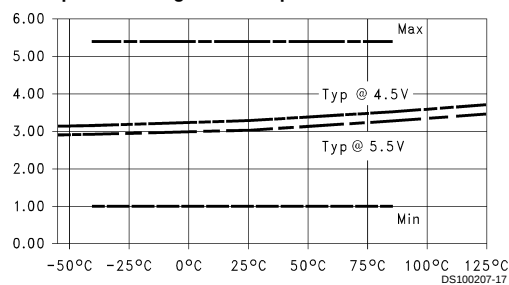
**$t_{PZL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



**$t_{PHZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



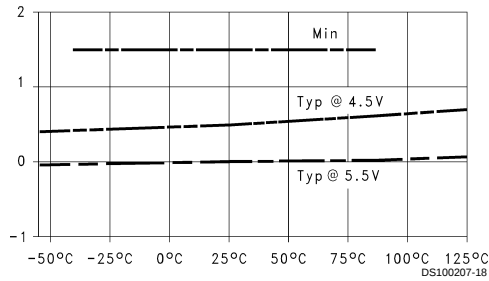
**$t_{PLZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



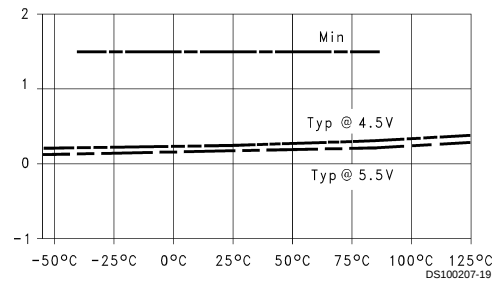
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

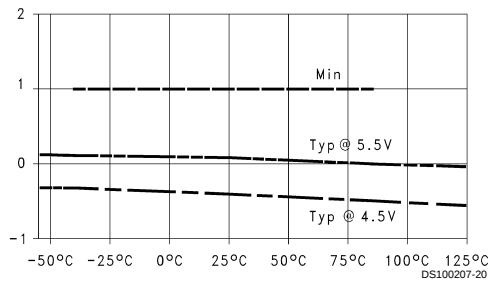
**$t_{SET}$  LOW vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



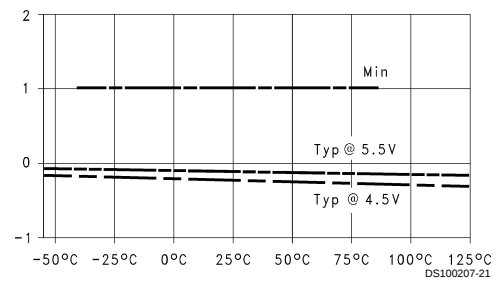
**$t_{SET}$  HIGH vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



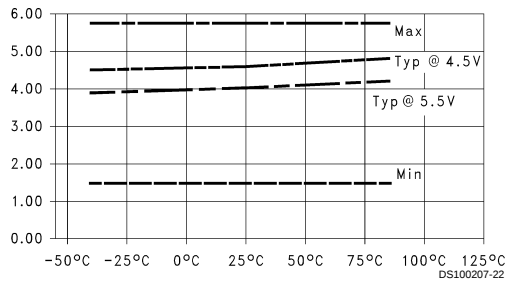
**$t_{HOLD}$  HIGH vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



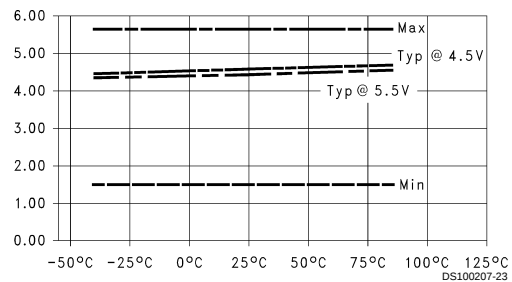
**$t_{HOLD}$  LOW vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



**$t_{PLH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching Clock to Output**



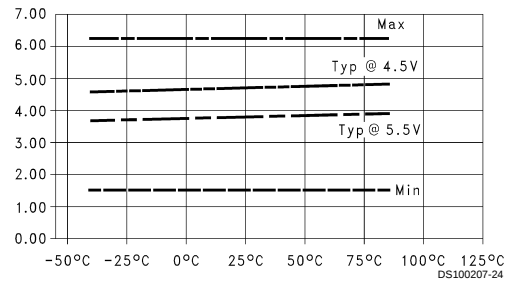
**$t_{PHL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching Clock to Output**



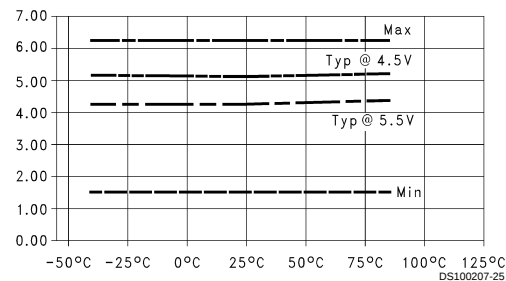
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

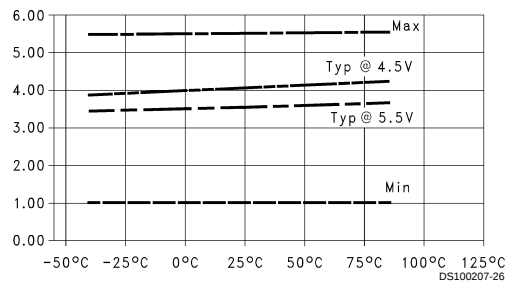
**$t_{PZH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching OE to Output**



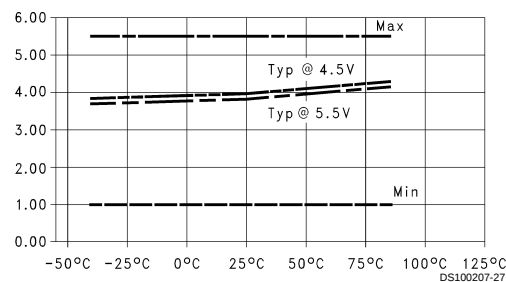
**$t_{PZL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching OE to Output**



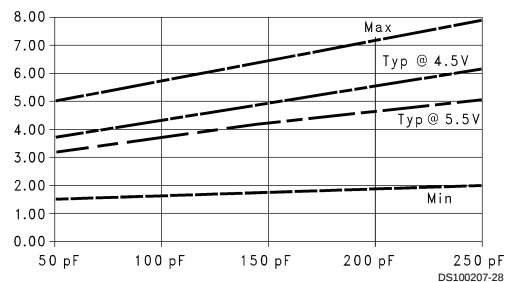
**$t_{PHZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching OE to Output**



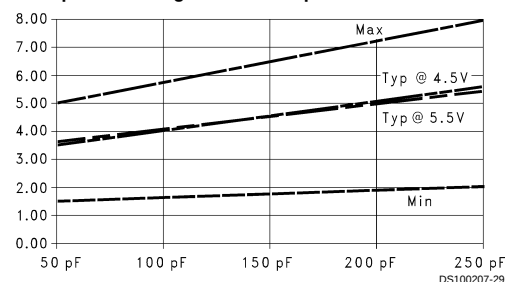
**$t_{PLZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching OE to Output**



**$t_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching Clock to Output**



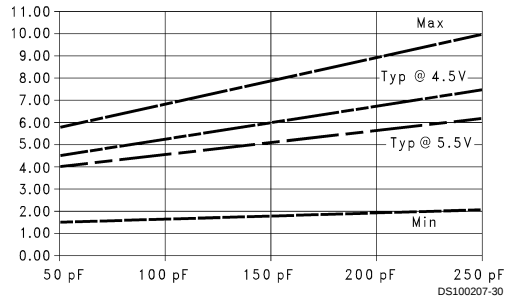
**$t_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching Clock to Output**



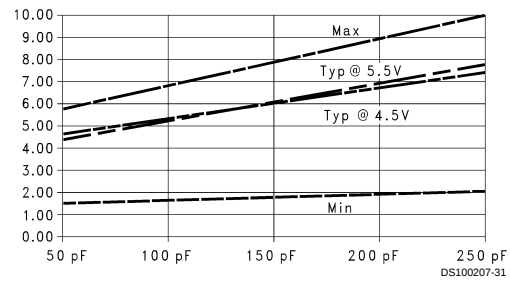
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

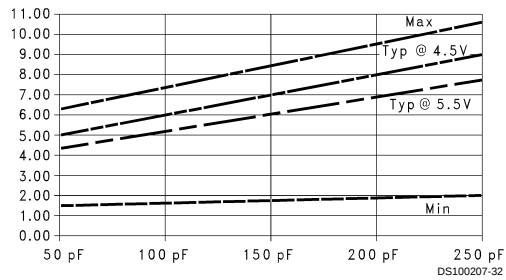
**$t_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching Clock to Output**



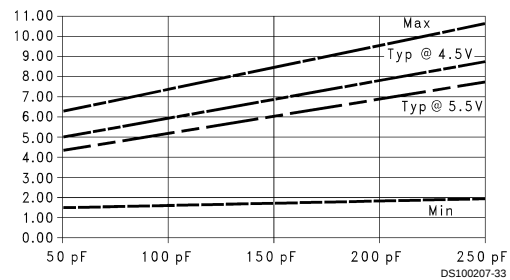
**$t_{PHL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching Clock to Output**



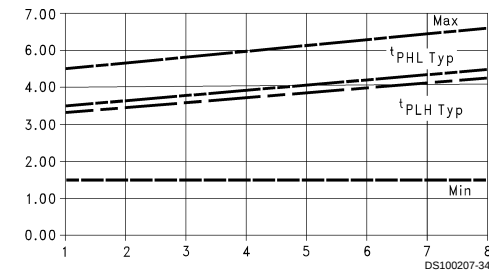
**$t_{PZH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching OE to Output**



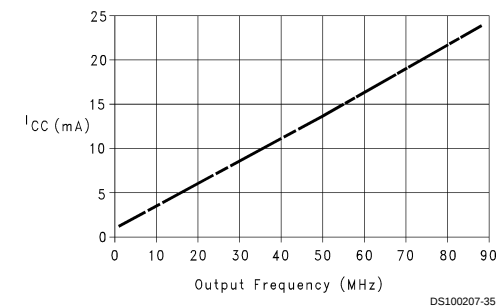
**$t_{PZL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching OE to Output**



**$t_{PLH}$  and  $t_{PHL}$  vs Number Outputs Switching  
 $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ ,  
Outputs in Phase Clock to Output**

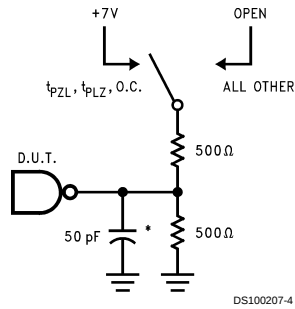


**Typical  $I_{CC}$  vs Output Switching Frequency  
 $C_L = 0\text{ pF}$ ,  $V_{CC} = V_{IH} = 5.5\text{V}$ , 1 Output  
Switching at 50% Duty Cycle Clock to Output**



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

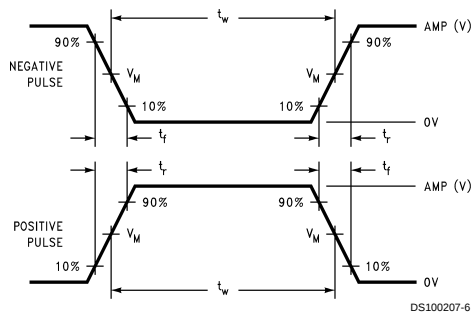
## AC Loading



DS100207-4

\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



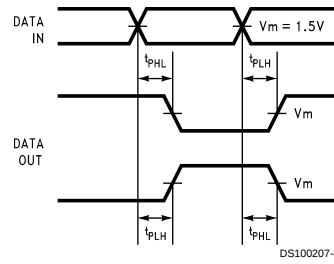
DS100207-6

FIGURE 2.  $V_M = 1.5V$

## Input Pulse Requirements

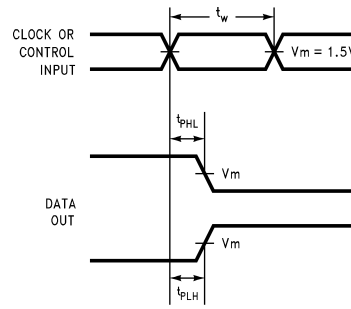
| Amplitude | Rep. Rate | $t_w$  | $t_r$  | $t_f$  |
|-----------|-----------|--------|--------|--------|
| 3.0V      | 1 MHz     | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements



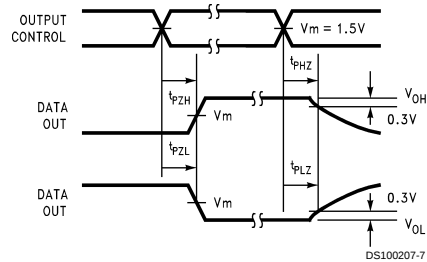
DS100207-8

FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



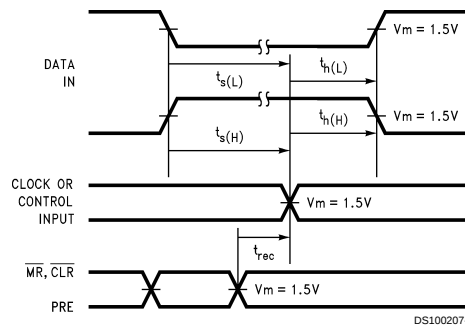
DS100207-5

FIGURE 5. Propagation Delay, Pulse Width Waveforms



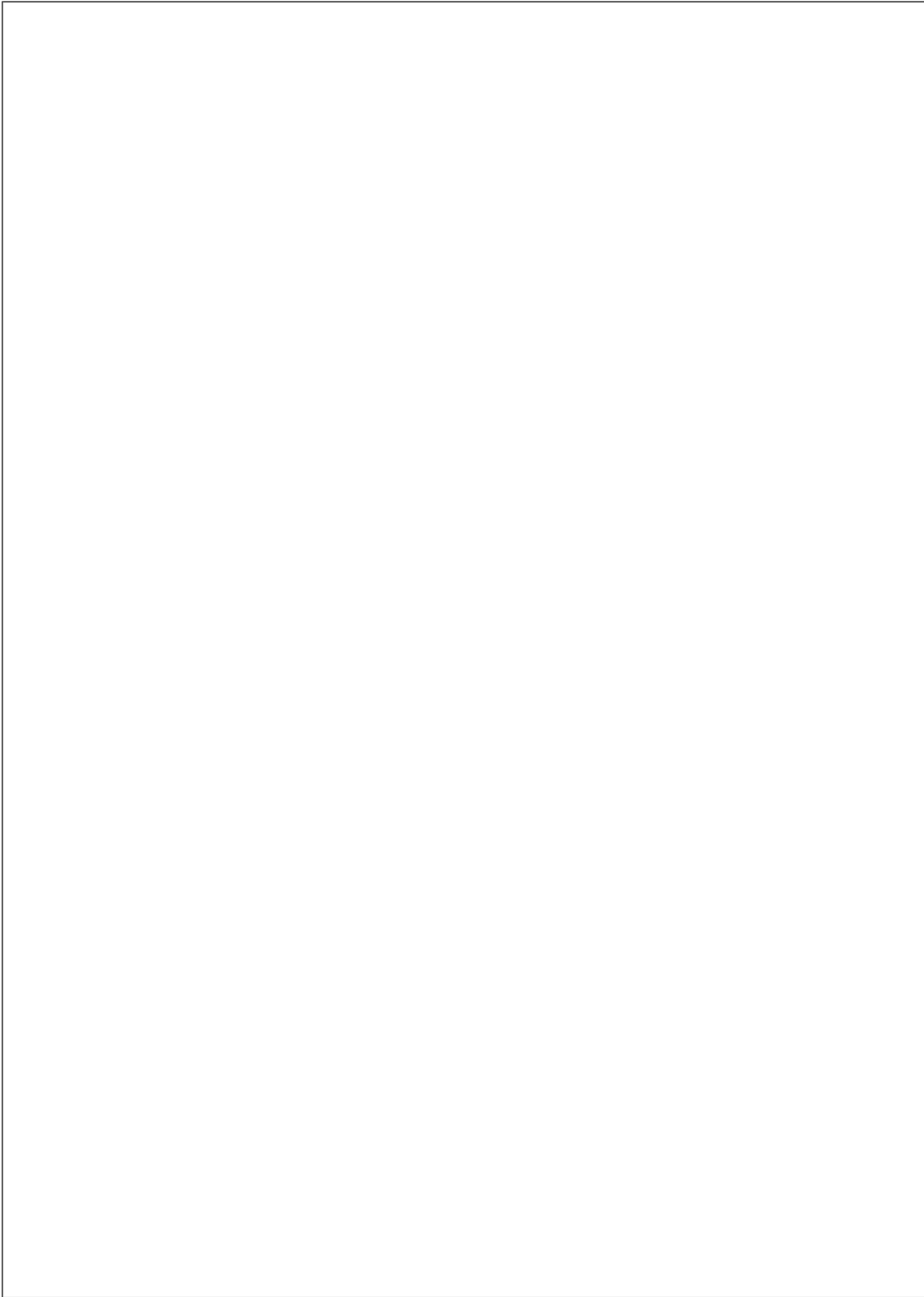
DS100207-7

FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

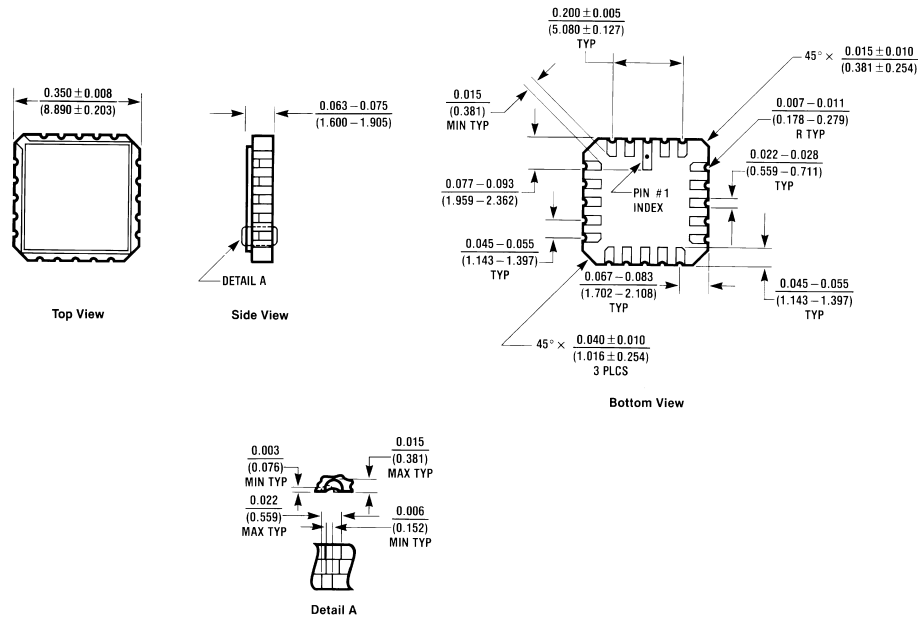


DS100207-9

FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

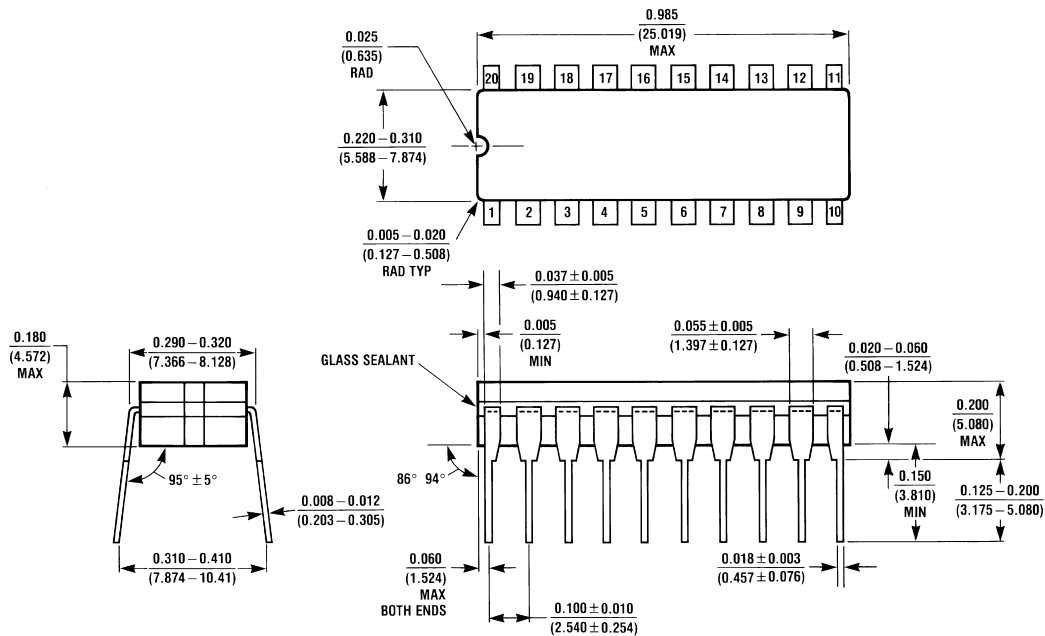


# Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

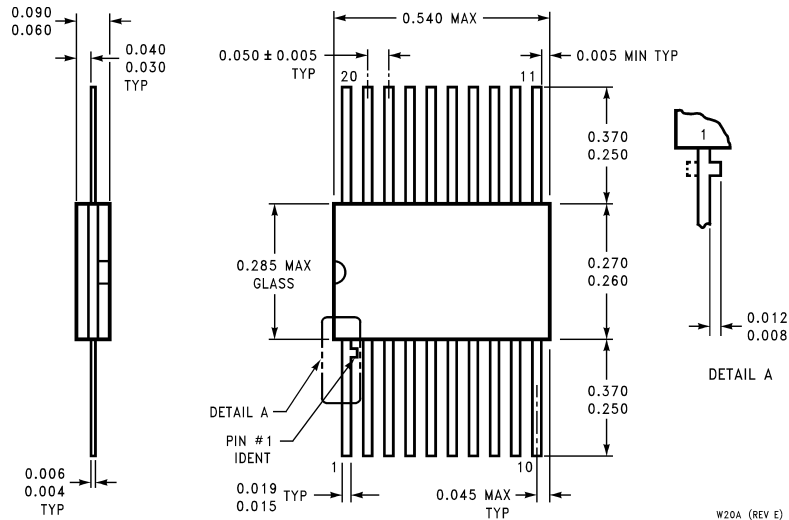
**20-Terminal Ceramic Chip Carrier (L)**  
**NS Package Number E20A**



J20A (REV M)

**20-Lead Ceramic Dual-In-Line (D)**  
**NS Package Number J20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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